MAXIM

CMOS 12-Bit Serial Input Multiplying D/A Converter

General Description

The MAX543 is a 12-bit current-output multiplying digital-to-analog converter (DAC) that is packaged in a space-saving 8-pin DIP or 16-pin surface mount SO. Its 3-wire serial interface saves additional circuit board space and also results in low power dissipation. When used with microprocessors (μP) with a serial port, the MAX543 minimizes the digital noise feed-through from its input pins to its output. The serial port can be used as a dedicated analog bus and kept inactive while the MAX543 is in use. Serial interfacing also reduces the complexity of opto- or transformer-isolated applications.

The MAX543 contains a 12-bit R-2R type DAC, a serial-in parallel-out shift register, a DAC register and control logic. On the rising edge of the clock (CLK) pulse the serial input (SRI) data is shifted into the MAX543. When all the data is clocked in, it is transferred into the DAC register by taking the LOAD input low.

The MAX543 is specified both with a single +5V and +15V power supply. With a +5V supply, the digital inputs are TTL and +5V CMOS compatible. High voltage CMOS compatibility is maintained with a +15V supply.

Maxim's MAX543 uses low tempco thin-film resistors laser trimmed to ±1/4 LSB linearity and better than ±1 LSB gain accuracy. The digital inputs are protected against electrostatic discharge (ESD) damage and can typically withstand over 5,000V of ESD voltages.

Applications

Automatic Calibration

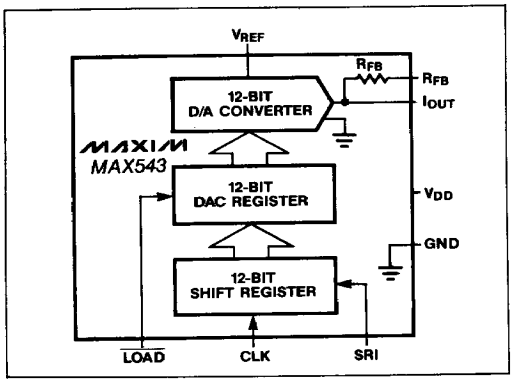
Motion Control Systems

μP Controlled Systems

Programmable Amplifiers/Attenuators

Digitally Controlled Filters

Functional Block Diagram



Features

- ◆ 12-Bit Accuracy in 8-Pin Mini-DIP
- ◆ Fast 3-Wire Serial Interface
- ◆ Low INL and DNL (±1/2 LSB Max)
- ◆ Gain Accuracy to ±1 LSB Max
- ◆ Low Gain Tempco (5ppm/°C Max)
- ◆ Operates with +5V or +15V Supplies
- ◆ TTL/CMOS Compatible
- ◆ ESD Protected

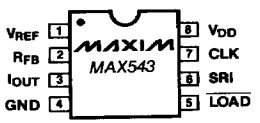
Ordering Information

PART	TEMP. RANGE	PACKAGE	LINEARITY
MAX543ACPA	0°C to +70°C	Plastic DIP	±1/2 LSB
MAX543BCPA	0°C to +70°C	Plastic DIP	±1 LSB
MAX543ACWE	0°C to +70°C	Wide SO	±1/2 LSB
MAX543BCWE	0°C to +70°C	Wide SO	±1 LSB
MAX543AEWE	-40°C to +85°C	Wide SO	±1/2 LSB
MAX543BEWE	-40°C to +85°C	Wide SO	±1 LSB
MAX543BC/D	0°C to +70°C	Dice	±1 LSB
MAX543AEJA	-40°C to +85°C	CERDIP	±1/2 LSB
MAX543BEJA	-40°C to +85°C	CERDIP	±1 LSB
MAX543AMJA	-55°C to +125°C	CERDIP	±1/2 LSB
MAX543BMJA	-55°C to +125°C	CERDIP	±1 LSB

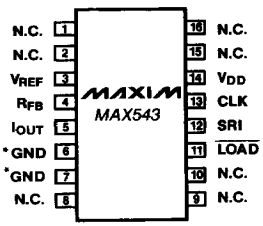
All DIP packages are 8 leads; all SO packages are 16 leads.

Pin Configurations

Top View



DIP



SO

* Leads 6 and 7 must be connected together as close to the package as possible.

CMOS 12-Bit Serial Input Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
V_{IOUT} to GND ..... -0.3V, V_{DD} + 0.3V
Power dissipation to +75°C (any package) 470mW
Derate above +75°C by ..... 6mW/°C

Operating Temperature Ranges
MAX543AC/BC ..... 0°C to 70°C
MAX543AE/BE ..... -40°C to +85°C
MAX543AM/BM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{IOUT} = GND = 0V; over specified temperature range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL			MAX543A MAX543B			±1/2 ±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits over temperature		MAX543A MAX543B			±1/2 ±1	LSB
Gain Error	FSE	Using internal R_{FB}	T_A = +25°C	MAX543A MAX543B			±1 ±2	LSB
			$T_A = T_{MIN}$ to T_{MAX}	All			±2	
Gain Tempco ΔGain/ΔTemp (Note 1)	TCFS	Using internal R_{FB}				±1	±5	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD} = ±5%.					±0.001	%/%
DYNAMIC PERFORMANCE (Note 1)								
Current Settling Time	t_S	To 1/2LSB. I_{OUT} load is 100Ω|| 13pF. DAC register alternately loaded with all 1s and all 0s.	T_A = +25°C			0.25	1	μs
Digital to Analog Glitch	Q	V_{REF}= 0V. I_{OUT} load is 100Ω||13pF. DAC register alternately loaded with all 1s and all 0s.				2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	V_{REF} = ±10Vp-p at 10kHz. DAC register loaded with all 0s.				0.4	1	mVp-p
Total Harmonic Distortion	THD	V_{REF} = $6V_{rms}$ at 1kHz. DAC register loaded with all 1s.				-85		dB
Output Noise Voltage Density	en	10Hz to 100kHz. Measured between R_{FB} and I_{OUT}.				13	15	nV/Hz
REFERENCE INPUT								
Input Resistance	RREF	V_{REF} pin to I_{OUT}			7	11	15	kΩ
Input Resistance Tempco	TCR					-200		ppm/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, +12V or +15V; V_{REF} = +10V; V_{IOUT} = GND = 0V; over specified temperature range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUT								
I_{OUT} Leakage Current	I_{LKG}	DAC register loaded with all 0s.	T_A = +25°C			±0.5	±5	nA
			T_A = T_{MIN} to T_{MAX}	MAX543AC/BC/AE/BE			±25	
				MAX543AM/BM			±100	
I_{OUT} Capacitance (Note 1)	C_{OUT}	DAC register loaded with all 0s.				55	80	pF
		DAC register loaded with all 1s.				85	110	
DIGITAL INPUTS								
Input High Voltage	V_{IH}		V_{DD} = +5V V_{DD} = +15V		2.4 13.5			V
Input Low Voltage	V_{IL}		V_{DD} = +5V V_{DD} = +15V				0.8 1.5	V
Input Leakage Current	I_{IN}	Digital Inputs at 0V or V_{DD}					±1	µA
Input Capacitance (Note 1)	C_{IN}	Digital Inputs at 0V or V_{DD}					8	pF
SWITCHING CHARACTERISTICS (Note 2)								
CLK Pulse Width High	t_{CH}				90			ns
CLK Pulse Width Low	t_{CL}				120			ns
SRI Data to CLK Setup	t_{DS}				40			ns
SRI Data to CLK Hold	t_{DH}				80			ns
$\overline{LOAD}$ Pulse Width	t_{LD}				120			ns
LSB CLK to $\overline{LOAD}$	t_{SL}				0			ns
$\overline{LOAD}$ High to CLK	t_{LC}				0			ns
POWER SUPPLY								
V_{DD} Range	V_{DD}		V_{DD} = +12V or +15V V_{DD} = +5V		+11.4 +4.75		+15.75 +5.25	V
I_{DD} Range	I_{DD}	All digital inputs at V_{IL} or V_{IH}					500	µA
		All digital inputs at 0V or V_{DD}				5	100	

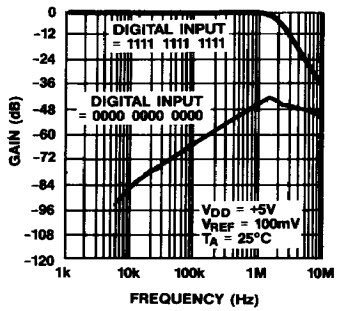
Note 1: Guaranteed by design and not subject to test.
Note 2: Sample tested at +25°C to ensure compliance.

9

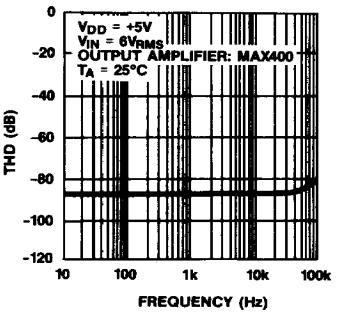
CMOS 12-Bit Serial Input Multiplying D/A Converter

Typical Operating Characteristics

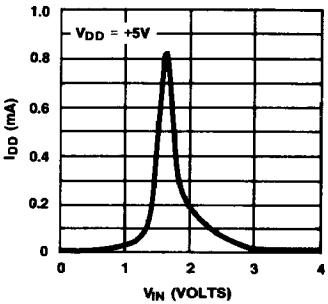
GAIN vs FREQUENCY (OUTPUT AMPLIFIER: MAX400)



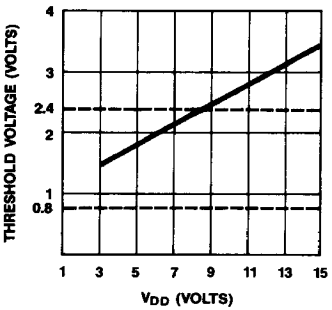
TOTAL HARMONIC DISTORTION vs FREQUENCY (MULTIPLYING MODE)



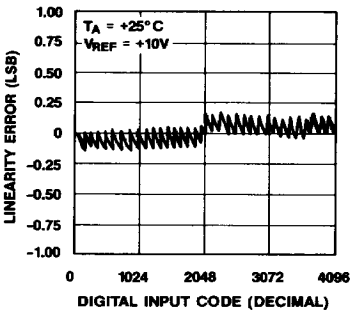
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



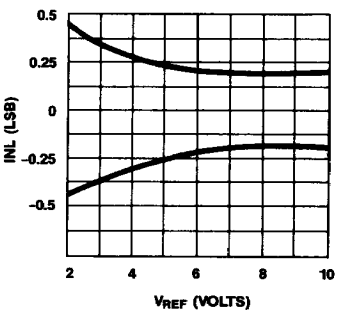
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



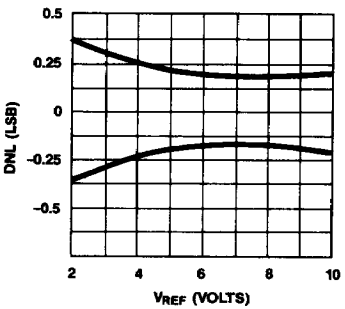
LINEARITY ERROR vs DIGITAL CODE



LINEARITY ERROR vs REFERENCE VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



CMOS 12-Bit Serial Input Multiplying D/A Converter

Detailed Description

D/A Converter

The MAX543 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binary weighted currents are switched to either I_{OUT} or GND depending on the status of each input data bit. Although the current at I_{OUT} and GND depends on the digital input code, the sum of the two output currents are always equal to the input current at V_{REF}.

The current output I_{OUT} can be converted into a voltage by adding an external output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT} pin output capacitance, C_{OUT}, is code dependent and is typically 55pF with all switches to GND and 85pF with all switches to I_{OUT}.

Digital Circuit

Figure 2 shows the timing diagram for the MAX543. The MSB is always loaded first on the rising edge of clock. When all the data is shifted into the MAX543, the DAC register is loaded by taking the LOAD signal low. The DAC register is transparent when LOAD is low and latched when LOAD is high. If the LOAD signal is taken low before the LSB bit is fully shifted into the shift register, the DAC output can produce a "glitch". If this is undesirable, the LOAD signal can be delayed 30ns after the rising edge of the LSB clock edge to avoid this condition.

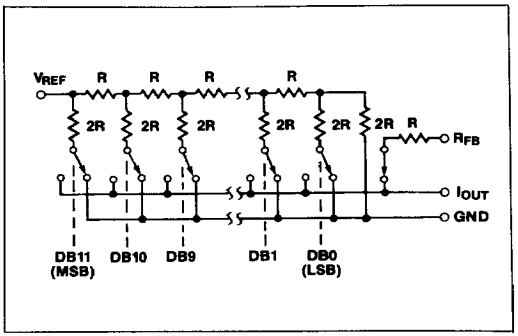


Figure 1. Simplified D/A Circuit of MAX543

The input buffer inverters of the MAX543 act as level shifters converting TTL levels into CMOS logic levels. These input buffers are TTL and +5V-CMOS compatible (0.8V and 2.4V) at V_{DD} = +5V. For V_{DD} = +15V the input buffers are CMOS compatible (1.5V and 13.5V). At this supply voltage the input buffers are in their linear region when the input voltages are between 1V and 6V. Therefore to minimize high supply currents, the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and GND) as possible.

Circuit Configurations

Unipolar Operation

Basic application of the MAX543 is shown in Figure 3. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.

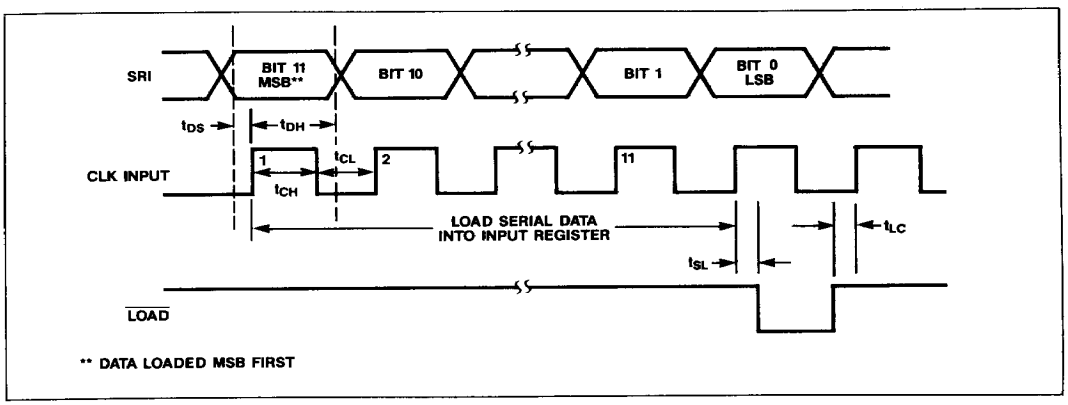


Figure 2. Write Cycle Timing Diagram

CMOS 12-Bit Serial Input Multiplying D/A Converter

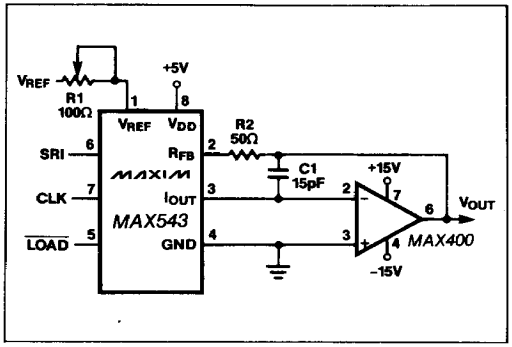


Figure 3. Unipolar Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0

In many applications gain adjustment will not be necessary since the gain accuracy of the part is sufficient, or the gain is trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. When trimming is used, and the DAC is operated over a wide temperature range, then low tempco (< 300ppm/°C) resistors should be used for R1 and R2.

The capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the output of the DAC.

Bipolar Operation

Figure 4 shows the MAX543 operating in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors (R3, R4 and R5) are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In

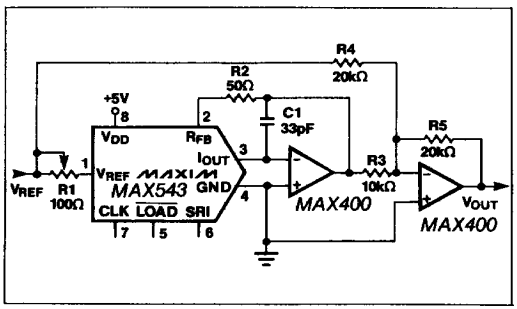


Figure 4. Bipolar Operation

Table 2. Offset Binary Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 3. 2's Complement Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	0
1111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR instruction to make the MAX543 work with 2's complement coding. Table 3 shows the code relationships to output voltage for the 2's complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using parts with a guaranteed maximum ±1 LSB gain error. In these cases, the gain can be trimmed at the reference source and resistors R1 and R2 in Figure 4 omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

Single Supply Operation (Voltage Mode)

The MAX543 can be conveniently used in single supply (voltage mode) operation with I_{OUT} biased at any voltage between GND and V_{DD}. I_{OUT} must not be allowed to go 0.3V lower than the GND or 0.3V higher than V_{DD}. Otherwise, internal diodes would turn on causing a high current flow from the supply which could damage the device.

Figure 5 shows the MAX543 connected as a voltage output DAC. I_{OUT} is connected to the reference voltage source and GND is grounded. The DAC output, now appears at the V_{REF} pin which has a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the response time of the circuit depends on the behavior of the reference source with changing load conditions.

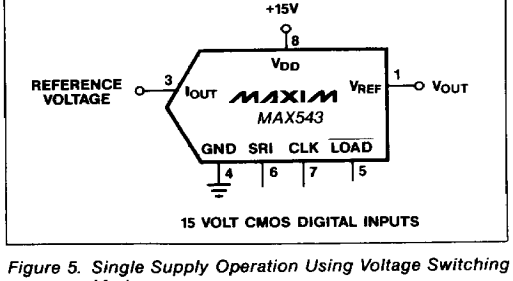


Figure 5. Single Supply Operation Using Voltage Switching Mode

Two advantages of the voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode.

MAX543 Opto-Isolated Application

Figure 6A shows the MAX543 interface to optocouplers for isolated barrier applications. Three optocouplers (OC1 thru OC3) carry the serial data and clocking signals across the isolation barrier. Isolated power sources, V^+ and V^-, supply the MAX543, the output amplifier and optocouplers. If data word updates are infrequent, and large analog output transitions can be tolerated while serial data is being clocked in, then parts count can be reduced by eliminating optocoupler OC3 and tying LOAD (pin 5) of the MAX543 low.

Using type 6N136 optocouplers this circuit accepts serial data at a maximum clock rate of 100kHz, or 130μs per data word. The SERIAL DATA and LOAD signals should change coincident with the falling edge of CLOCK, as shown in the timing diagram (Figure 6B). A positive CLOCK cycle is masked during the time that LOAD is low.

The MAX543 will also work with +5V isolated supplies using the optocoupler circuit of Figure 6A. The values of R1 through R3 should be changed to 3kΩ to maintain switching speed with the lower value of V^+.

Current drawn from V^- for the MAX543 and optocoupler is 3.5mA at 100kHz clock rate when all data bits are set to zero. V^+ current drops to zero (excluding reference and op amp current) when no new data is being loaded and CLOCK, SERIAL DATA, and LOAD are static high.

Microprocessor Interfacing

Interfacing to the 8085

Figure 7 shows the MAX543 interfacing to the 8085 microprocessor. The SOD line from the 8085 is used to send serial data to the DAC. This data is clocked into the MAX543 by executing memory write instructions. The CLK input for the DAC can be generated by decoding address 8000 and the WR signal. The data is transferred into the DAC register with a memory write instruction to address A000 which brings LOAD low. The data for the MAX543 is stored in the right-justified format in registers H and L of the 8085.

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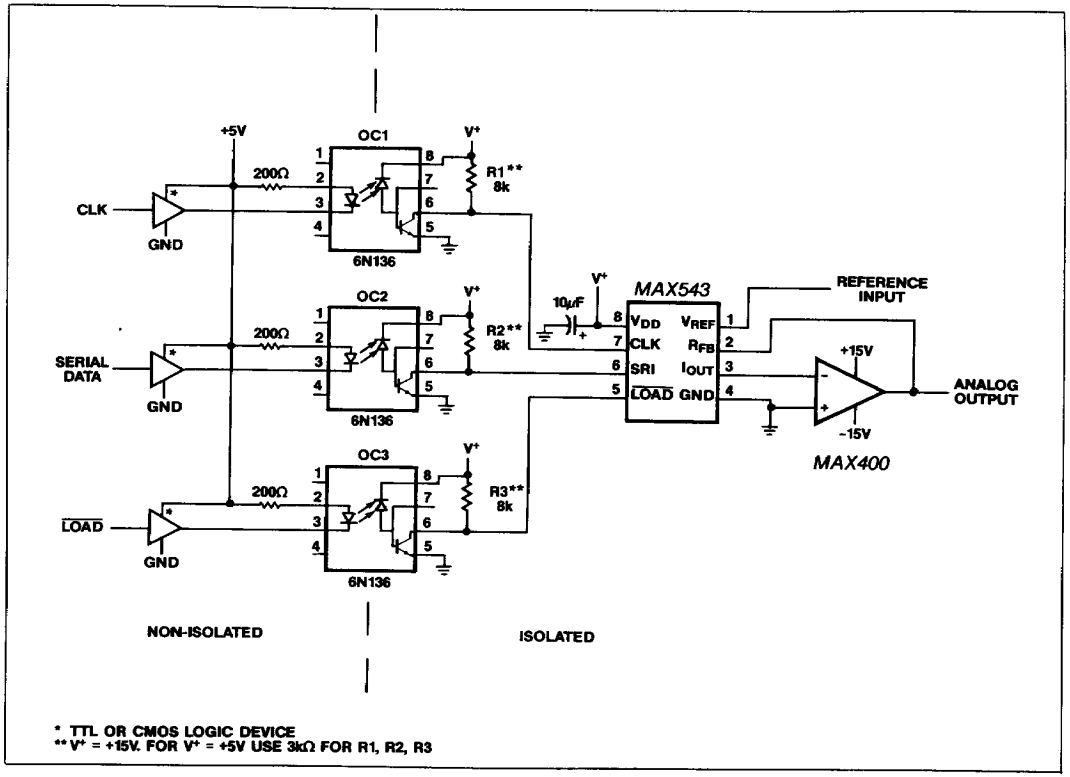

Figure 6A. MAX543 Opto-coupled Application

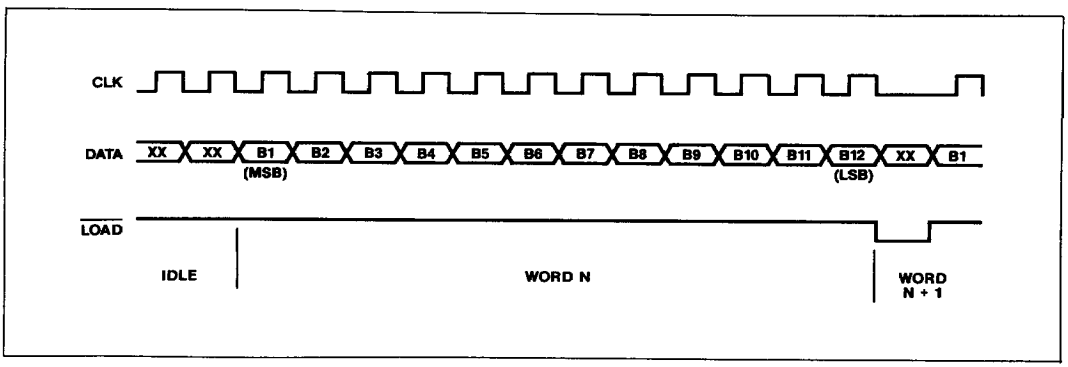

Figure 6B. MAX543 Opto-Isolated Timing

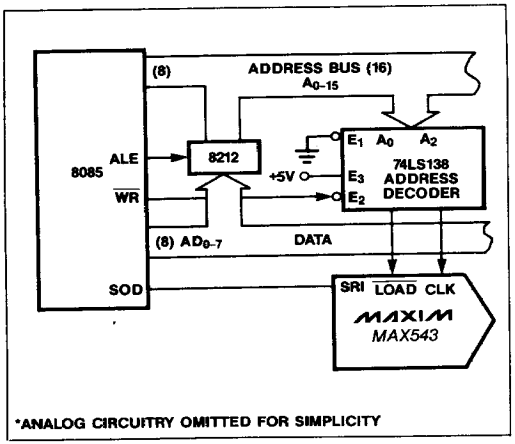

Figure 7. MAX543 - 8085 Interface

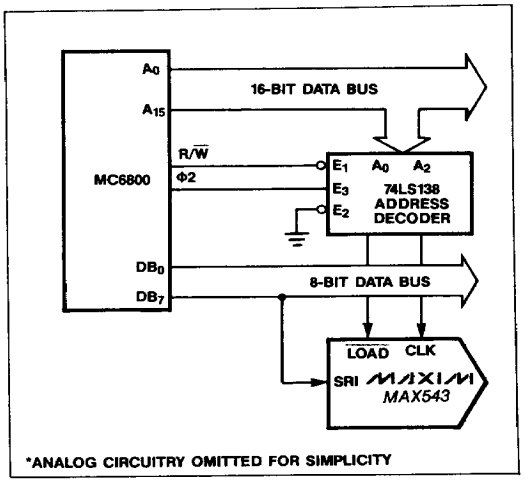

Figure 8. MAX543 - MC6800 Interface

Interfacing to the MC6800

Figure 8 shows the MAX543 interfacing to the MC6800 microprocessor. The data is transferred into the MAX543 by executing successive memory WRITE instructions while changing the data between WRITEs to construct the serial data to the DAC.

The DB7 data line is used for the SRI signal. The lower half of the memory location 0000 holds the four MSB data bits, and the 0001 location holds the eight LSB data bits. The memory address 2000, R/W, and 02 are decoded to generate the CLK signal for the DAC with each memory WRITE. Similarly, a memory WRITE to address 4000 transfers data into the DAC register by bringing the MAX543's LOAD input low.

Application Information

Output Amplifier Offset

For best linearity, I_{OUT} and GND should be terminated at exactly 0V. In most applications I_{OUT} is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_O)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will, therefore, degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10LSB.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should, therefore, be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to I_{OUT}. This normally is a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and I_{OUT} pins.

The DAC output follows the digital inputs when the LOAD pin is low. In this mode invalid outputs and voltage glitches can appear at the DAC output. Keeping the LOAD input high until all the data is shifted into the MAX543 eliminates this problem.

CMOS 12-Bit Serial Input Multiplying D/A Converter

Compensation

A compensation capacitor, C1, may be required when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used but typically ranges from 10pF to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at I_{OUT} as low as possible.

Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected across the DAC V_{DD} and GND as close to the pins as possible.

The MAX543 has high impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

Chip Topography