



PBSS4021SP

20 V, 6.3 A PNP/PNP low V_{CEsat} (BISS) transistor

Rev. 2 — 11 October 2010

Product data sheet

1. Product profile

1.1 General description

PNP/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT96-1 (SO8) medium power Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/PNP complement	NPN/PNP complement
	Nexperia	Name		
PBSS4021SP	SOT96-1	SO8	PBSS4021SN	PBSS4021SPN

1.2 Features and benefits

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Loadswitch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

1.4 Quick reference data

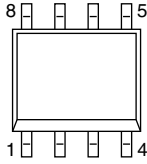
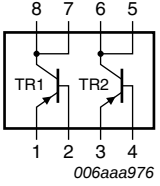
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-20	V
I_C	collector current		-	-	-6.3	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-15	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -5$ A; $I_B = -0.5$ A [1]	-	36	54	m Ω

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		 006aaa976
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4021SP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4021SP	4021SP

5. Limiting values

Table 6. Limiting values

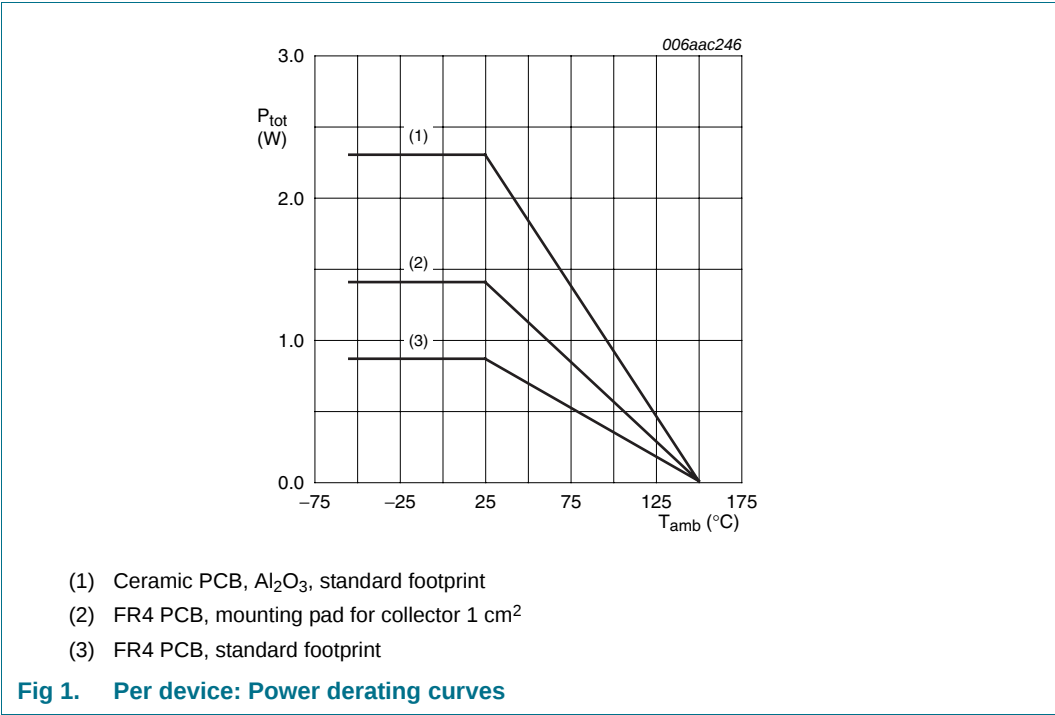
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{CBO}	collector-base voltage	open emitter	-	−20	V
V _{CEO}	collector-emitter voltage	open base	-	−20	V
V _{EBO}	emitter-base voltage	open collector	-	−5	V
I _C	collector current		-	−6.3	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	−15	A
I _B	base current		-	−1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] -	0.73	W
			[2] -	1	W
			[3] -	1.7	W

Table 6. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] -	0.86	W
			[2] -	1.4	W
			[3] -	2.3	W
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	+150	°C
T _{stg}	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] -	-	170	K/W
			[2] -	-	125	K/W
			[3] -	-	75	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point		-	-	40	K/W
Per device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] -	-	145	K/W
			[2] -	-	90	K/W
			[3] -	-	55	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

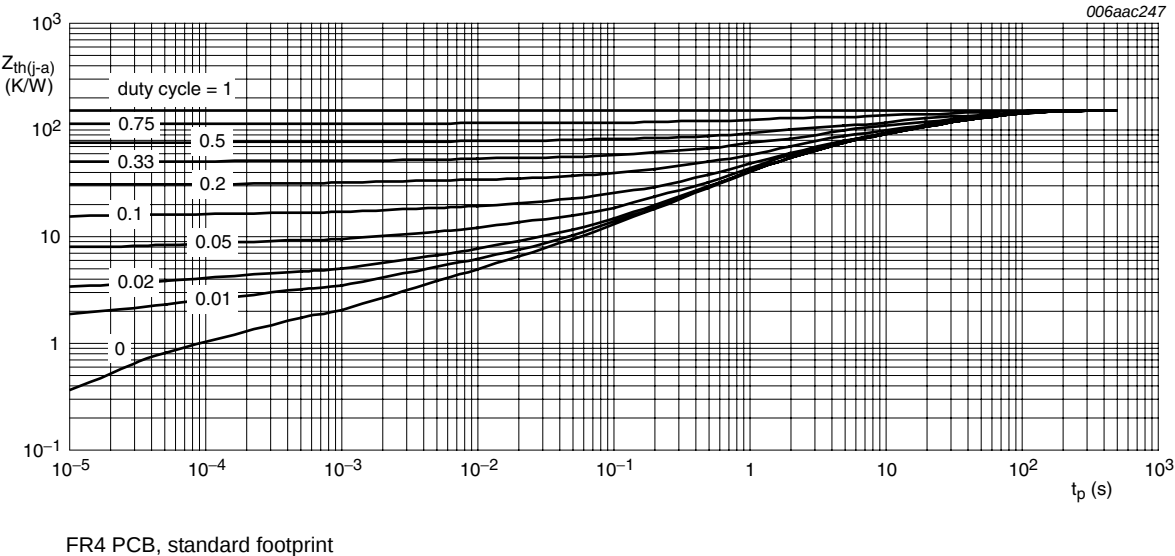
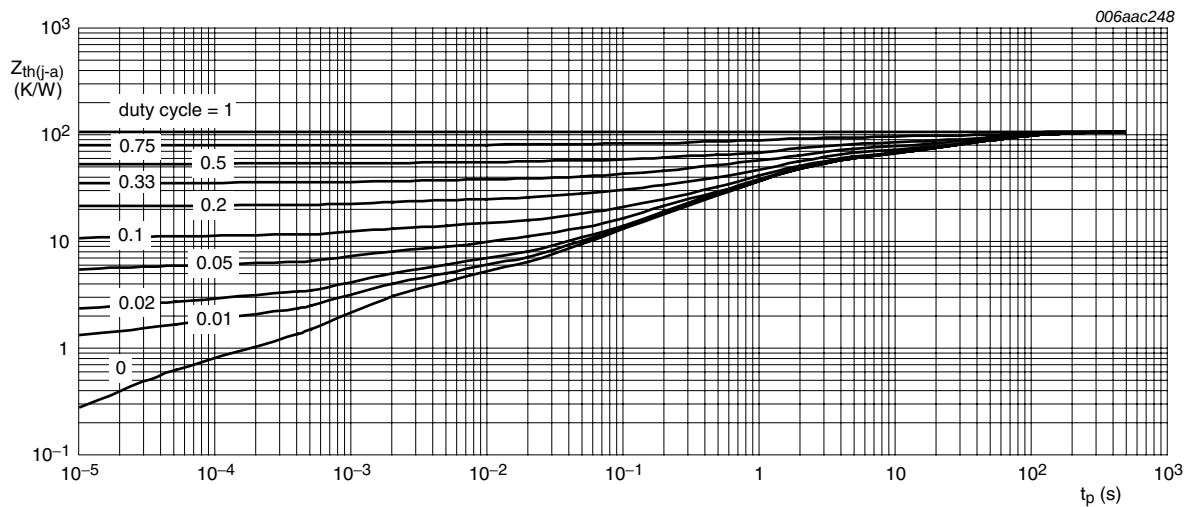
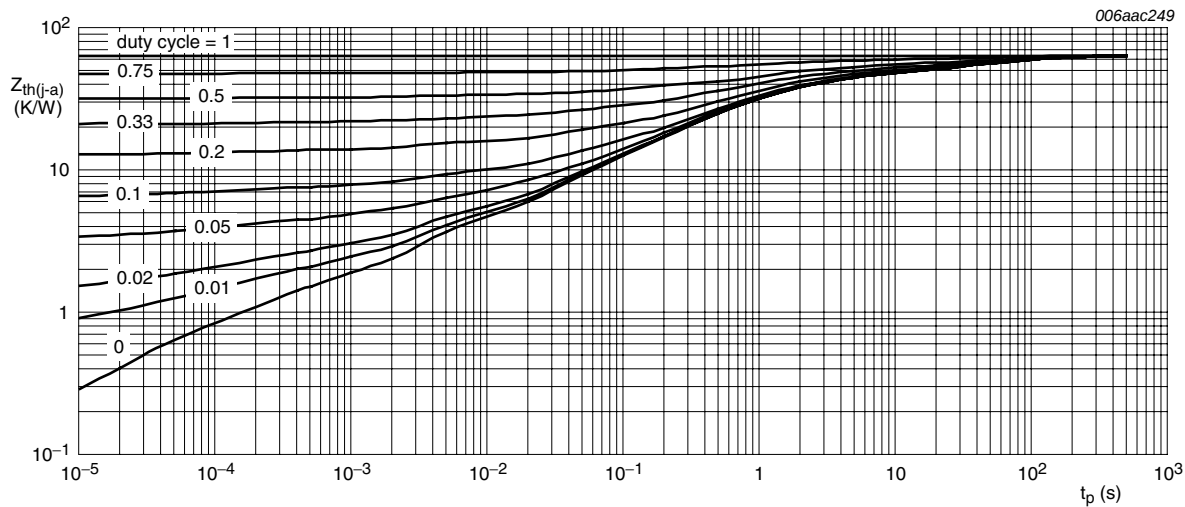


Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm²

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

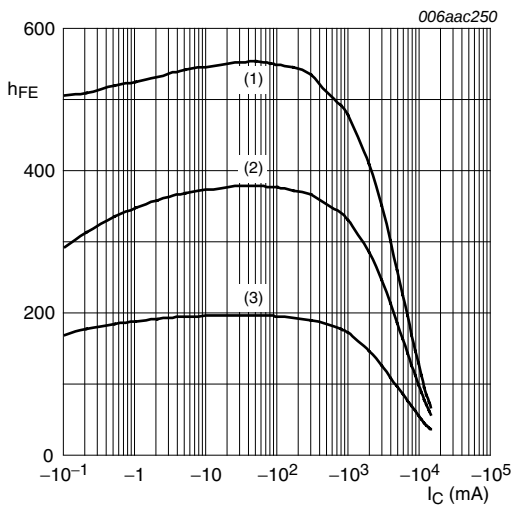
7. Characteristics

Table 8. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

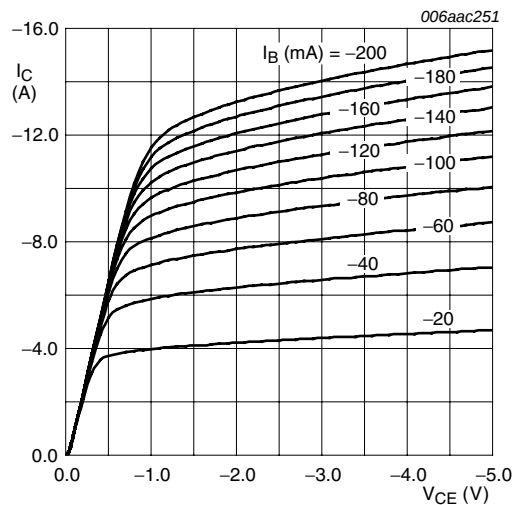
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
I _{CBO}	collector-base cut-off current	V _{CB} = −20 V; I _E = 0 A	-	-	−100	nA	
		V _{CB} = −20 V; I _E = 0 A; T _j = 150 °C	-	-	−50	μA	
I _{CES}	collector-emitter cut-off current	V _{CE} = −16 V; V _{BE} = 0 V	-	-	−100	nA	
I _{EBO}	emitter-base cut-off current	V _{EB} = −5 V; I _C = 0 A	-	-	−100	nA	
h _{FE}	DC current gain	V _{CE} = −2 V	[1]				
		I _C = −500 mA	250	400	-		
		I _C = −1 A	250	400	-		
		I _C = −2 A	200	350	-		
		I _C = −4 A	150	300	-		
		I _C = −7 A	80	200	-		
V _{CEsat}	collector-emitter saturation voltage		[1]				
		I _C = −1 A; I _B = −50 mA	-	−45	−68	mV	
		I _C = −1 A; I _B = −10 mA	-	−70	−115	mV	
		I _C = −2 A; I _B = −40 mA	-	−100	−150	mV	
		I _C = −4 A; I _B = −200 mA	-	−150	−225	mV	
		I _C = −4 A; I _B = −40 mA	-	−250	−375	mV	
	I _C = −6.5 A; I _B = −325 mA	-	−235	−350	mV		
R _{CEsat}	collector-emitter saturation resistance	I _C = −5 A; I _B = −500 mA	[1]	-	36	54	mΩ
V _{BEsat}	base-emitter saturation voltage		[1]				
		I _C = −1 A; I _B = −100 mA	-	−0.85	−1	V	
		I _C = −4 A; I _B = −400 mA	-	−1	−1.2	V	
V _{BEon}	base-emitter turn-on voltage	V _{CE} = −2 V; I _C = −2 A	[1]	-	−0.76	−0.85	V
t _d	delay time	V _{CC} = −12.5 V; I _C = −1 A;	-	40	-	ns	
t _r	rise time	I _{Bon} = −0.05 A; I _{Boff} = 0.05 A	-	55	-	ns	
t _{on}	turn-on time		-	95	-	ns	
t _s	storage time		-	340	-	ns	
t _f	fall time		-	85	-	ns	
t _{off}	turn-off time		-	425	-	ns	
f _T	transition frequency	V _{CE} = −10 V; I _C = −100 mA; f = 100 MHz	-	105	-	MHz	
C _c	collector capacitance	V _{CB} = −10 V; I _E = i _e = 0 A; f = 1 MHz	-	95	-	pF	

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.



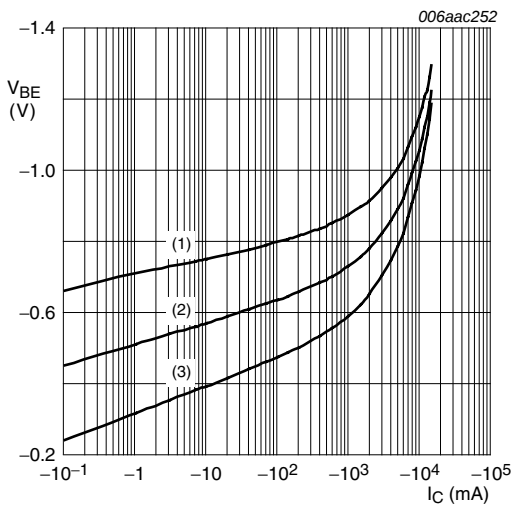
$V_{CE} = -2\text{ V}$
(1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 5. DC current gain as a function of collector current; typical values



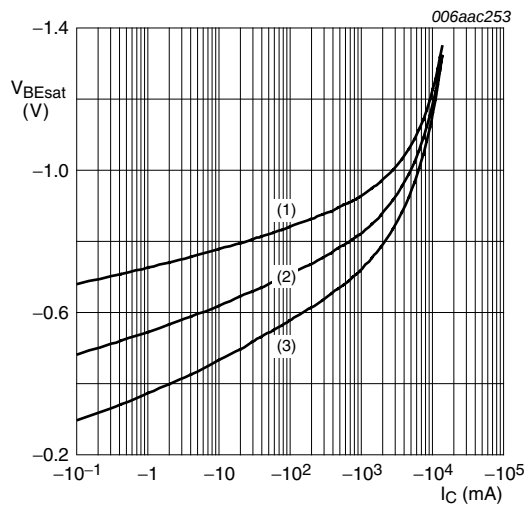
$T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 6. Collector current as a function of collector-emitter voltage; typical values



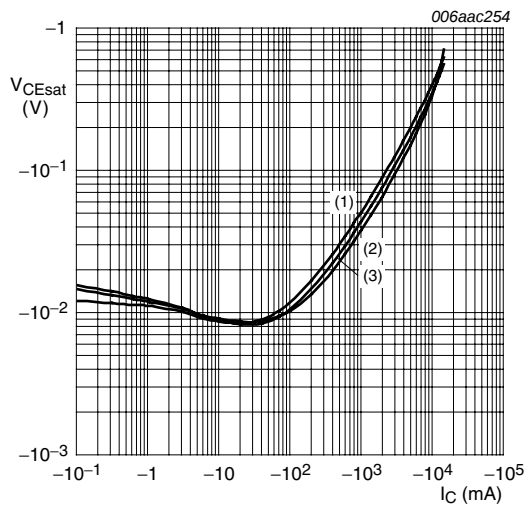
$V_{CE} = -2\text{ V}$
(1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 7. Base-emitter voltage as a function of collector current; typical values



$I_C/I_B = 20$
(1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

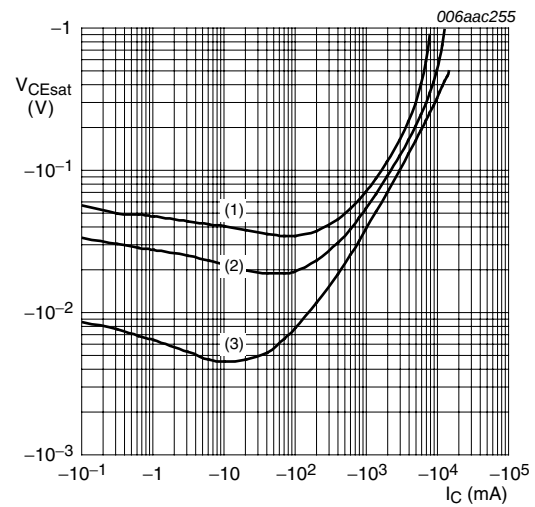
Fig 8. Base-emitter saturation voltage as a function of collector current; typical values



$$I_C/I_B = 20$$

- (1) $T_{amb} = 100\text{ °C}$
- (2) $T_{amb} = 25\text{ °C}$
- (3) $T_{amb} = -55\text{ °C}$

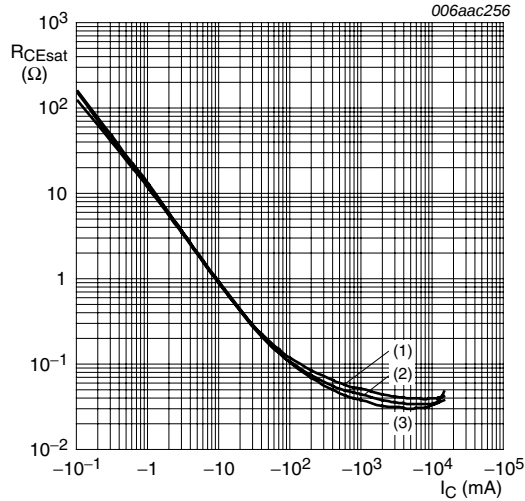
Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



$$T_{amb} = 25\text{ °C}$$

- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

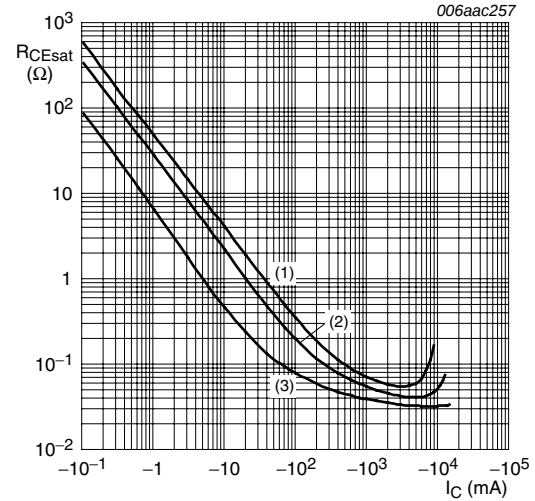
Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



$$I_C/I_B = 20$$

- (1) $T_{amb} = 100\text{ °C}$
- (2) $T_{amb} = 25\text{ °C}$
- (3) $T_{amb} = -55\text{ °C}$

Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values



$$T_{amb} = 25\text{ °C}$$

- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

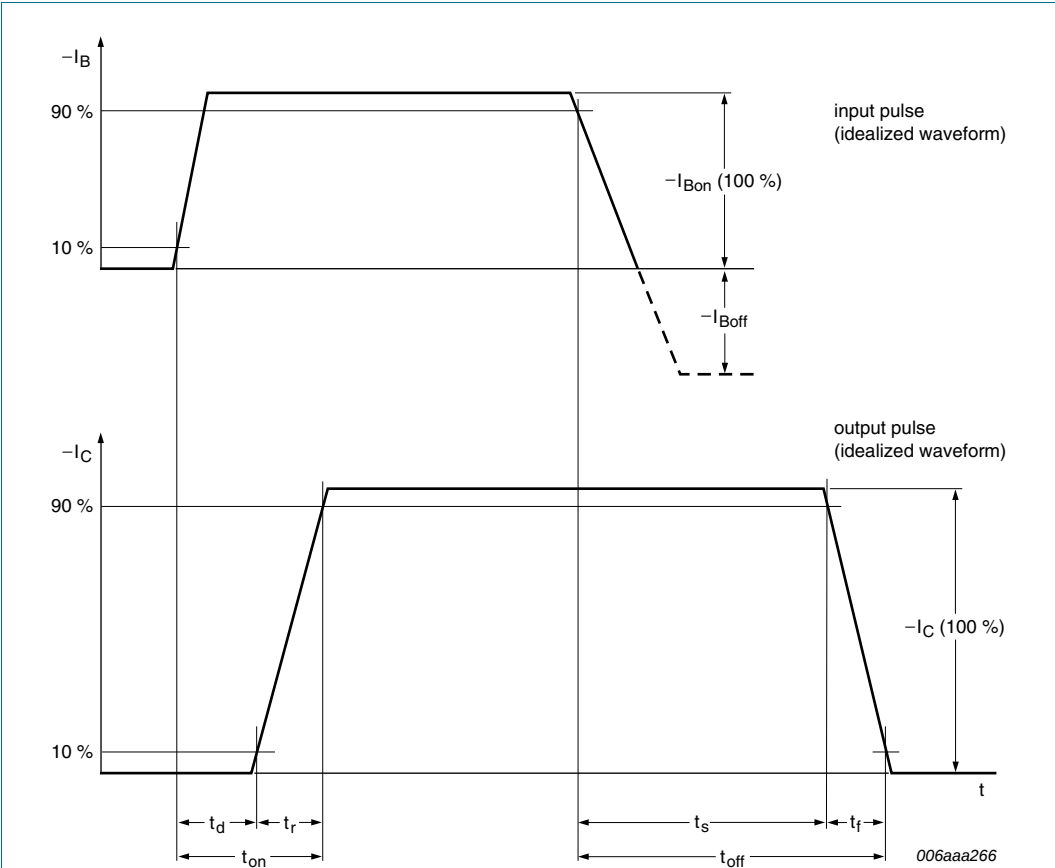
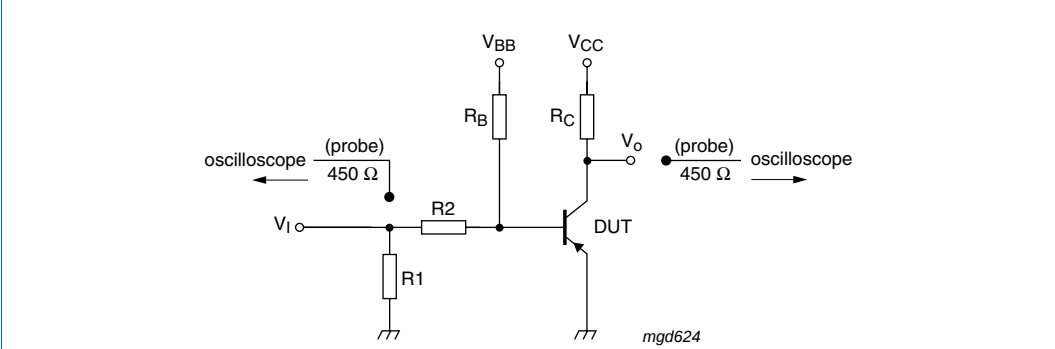


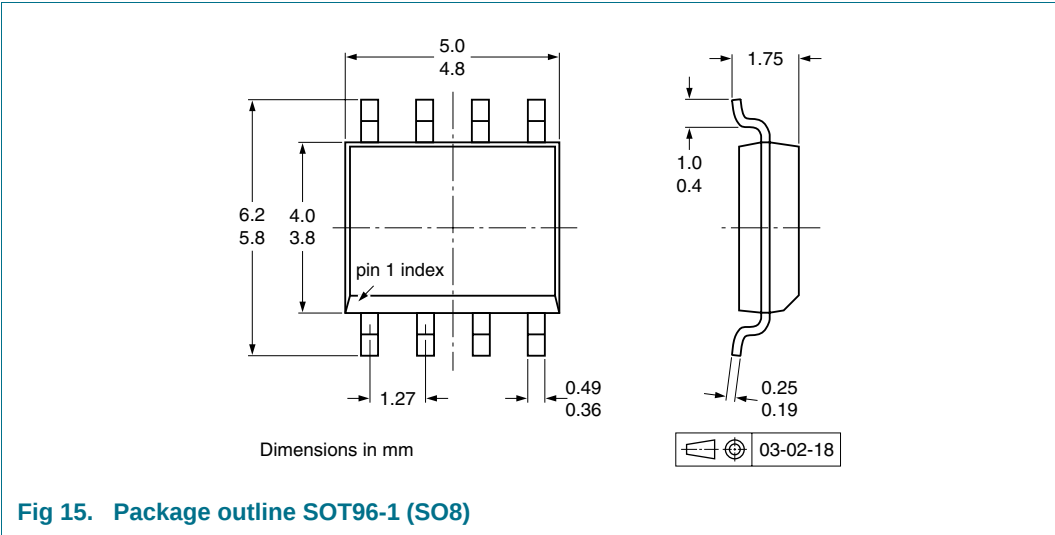
Fig 13. BISS transistor switching time definition



$V_{CC} = -12.5\text{ V}$; $I_C = -1\text{ A}$; $I_{Bon} = -0.05\text{ A}$; $I_{Boff} = 0.05\text{ A}$

Fig 14. Test circuit for switching times

9. Package outline



10. Packing information

Table 9. Packing methods
The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS4021SP	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering

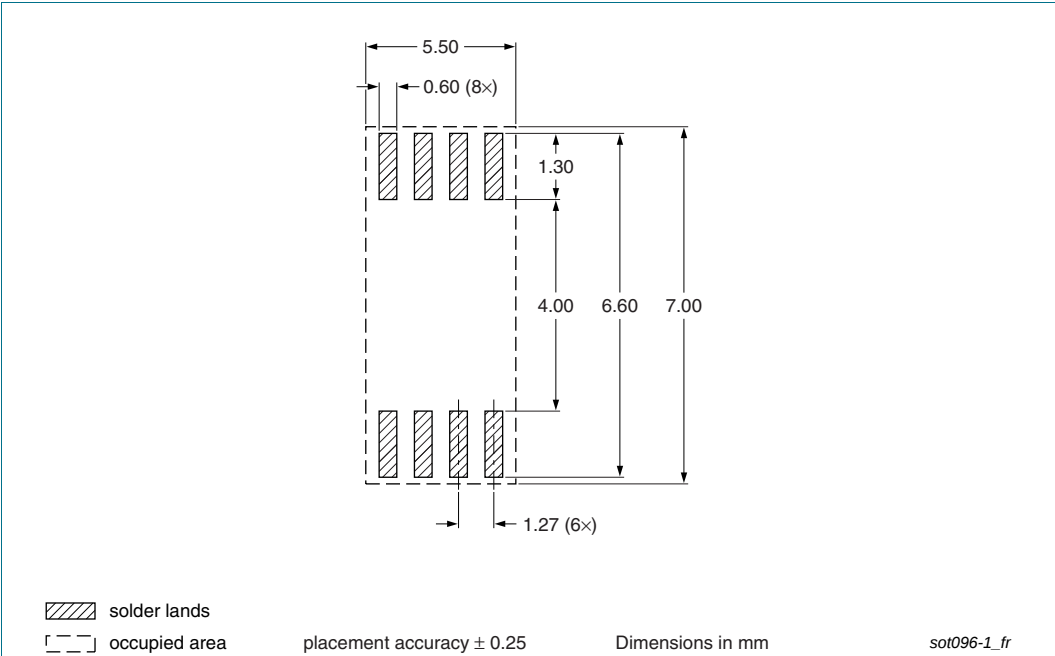


Fig 16. Reflow soldering footprint SOT96-1 (SO8)

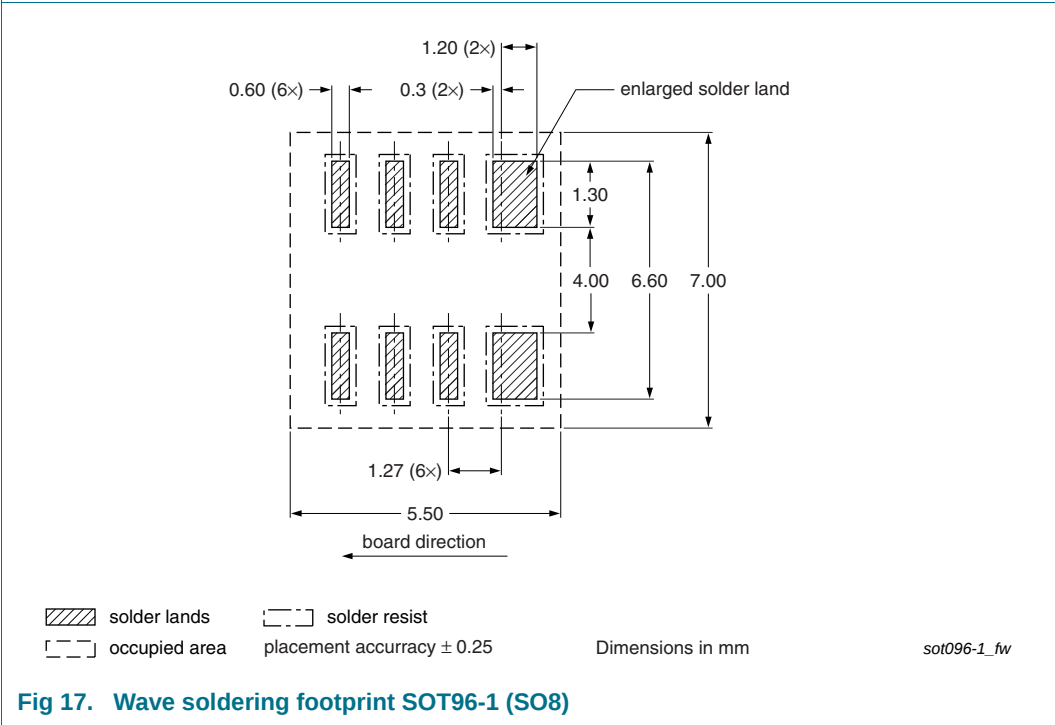


Fig 17. Wave soldering footprint SOT96-1 (SO8)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4021SP v.2	20101011	Product data sheet	-	PBSS4021SP v.1
Modifications:	• Figure 1 “Per device: Power derating curves” : updated.			
PBSS4021SP v.1	20100714	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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