

Signetics

Integrated Circuits TTL

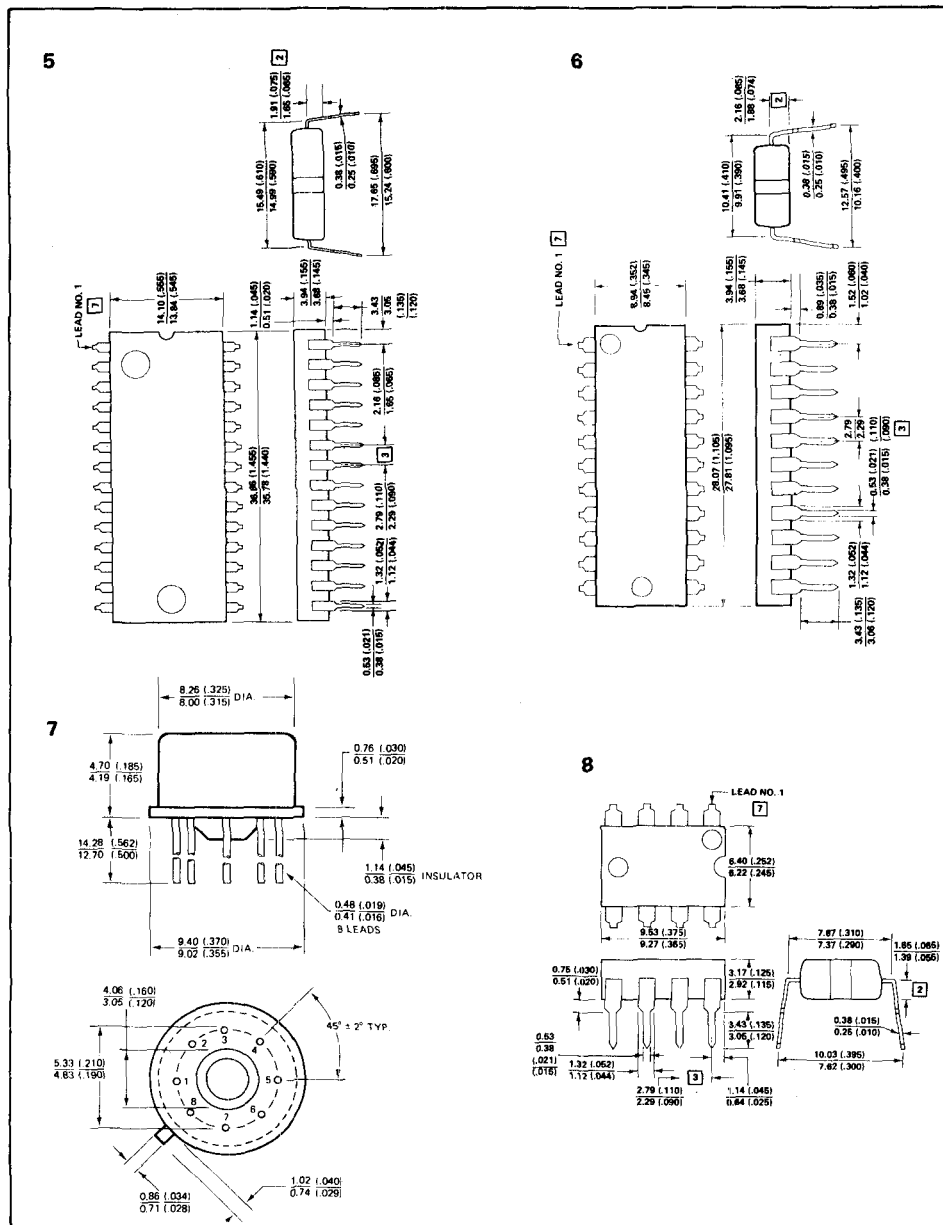
TYPE NO	DESCRIPTION	STOCK NO.	OUTLINE DRWG. NO.	CONNECTION DIAG. NO.
N7476N	Dual J-K Master-Slave F/F	55234X	2	B55
N7480N	Gated Full Adder	55235H	1	B56
N7483N	4-Bit Binary Full Adder	55236F	2	B57
N7483AN	4-Bit Binary Full Adder	55344R	2	B57
N7485N	4-Bit Magnitude Comparator	55237D	2	B59
N7486N	Quad 2-Input Exclusive OR Gate	55238B	1	B60
N7490N	Decade Counter	55239X	1	B61
N7491N	8-Bit Shift Register	55240C	1	B62
N7492N	Divide-By-Twelve Counter	55241A	1	B63
N7493N	4-Bit Binary Counter	55242X	1	B64
N7494N	4-Bit Shift Register (PISO)	55243H	2	B65
N7495N	4-Bit Left-Right Shift Register	55244F	1	B66
N7496N	5-Bit Shift Register	55245D	2	B67
N74100N	4-Bit Bistable Latch (Dual)	55246B	3	B68
N74107N	Dual J-K Master-Slave F/F	55247X	1	B69
N74109N	Dual J-K Positive Edge Triggered F/F	55248R	2	B70
N74116N	Dual 4-Bit Latch with clear	55249G	3	B71
N74121N	Monostable Multivibrator	55250X	1	B72
N74122N	Retriggerable Monostable Multivibrator	55251H	1	B73
N74123N	Retriggerable Monostable Multivibrator	55252F	2	B74
N74125N	Quad Bus Buffer Gate w/Tri-state outputs	55253D	1	B75
N74126N	Quad Bus Buffer Gate w/Tri-state outputs	55254B	1	B76
N74128N	Quad 2-Input NOR Buffer	55255X	1	B77
N74132N	Quad Schmitt Trigger	55256R	1	B78
N74145N	BCD-to-Decimal Decoder/Drive with O/C	55257G	2	B79
N74147N	10-Line to 4-Line Priority Encoder	55258E	2	B80
N74148N	8-Line to 3-Line Priority Encoder	55259C	2	B81
N74150N	16-Line to 1-Line Mux	55260F	2	B82
N74151N	8-Line to 1-Line Mux	55261D	2	B83
N74153N	Dual 4-Line to 1-Line Mux	55262B	2	B84
N74154N	4-Line to 16-Line Decoder/Demux	55263X	3	B85
N74155N	Dual 2-Line to 4-Line Decoder/Demux	55264R	2	B86
N74156N	2-Line to 4-Line Decoder/Demux	55265G	2	B86
N74157N	Quad 2-Input Data Selector (non-inu.)	55266E	2	B88
N74158N	Quad 2-Input Data Selector (inv.)	55267C	2	B89
N74160N	Synchronous 4-Bit Decode Counter	55268A	2	B90
N74161N	Synchronous 4-Bit Binary Counter	55269X	2	B90
N74162N	Synchronous 4-Bit Decode Counter	55270B	2	B90
N74163N	Synchronous 4-Bit Binary Counter	55271X	2	B90
N74164N	8-Bit Parallel Out Serial Shift Register	55272R	1	B94
N74165N	Parallel-Load 8-Bit Shift Register	55273G	2	B95
N74166N	8-Bit Shift Register	55274E	2	B96
N74170N	4 x 4 Register File	55275C	2	B97
N74173N	Quad D-Type F/F (Tri-State) (8T10)	55276A	2	B98
N74174N	Hex D-Type F/F with Clear	55277X	2	B99
N74175N	Quad D-Type Edge-Triggered F/F	55278H	2	B100
N71176N	Presetable Decade Counter/Latch (8270)	55279F	1	B101
N74177N	Presetable Binary Counter/Latch (8271)	55280R	1	B101
N74178N	4-Bit Parallel Access Shift Reg (8280)	55281G	2	B103
N74179N	4-Bit Parallel Shift Reg (8281)	55282E	2	B104
N74180N	8-Bit Odd/Even Parity Checker	55283C	1	B105
N74181N	4-Bit Arithmetic Logic Unit	55284A	3	B106
N74182N	Look-Ahead Carry Generator	55285X	2	B107
N74190N	Synchronous Up/Down Counter (BCD)	55286H	2	B108
N74191N	Synchronous Up/Down Counter (Binary)	55287F	2	B109
N74192N	Synchronous Decade Up/Down Counter	55288D	2	B110
N74193N	Synchronous 4-Bit Binary Up/Down Counter	55289B	2	B110
N74194N	4-Bit Bidirectional Universal Sh ft Reg.	55290E	2	B112
N74195N	4-Bit Parallel Access Shift Reg.	55291C	2	B113
N74196N	Presetable Decade Counter/Latch (8290)	55292A	1	B114
N74197N	Presetable Binary Counter/Latch (8291)	55293X	1	B114
N74198N	8-Bit Shift Register	55294H	3	B116
N74199N	8-Bit Shift Register	55295F	3	B117
N74221N	Dual Monostable Multivibrator	55296D	2	B118
N74279N	Quad S-R Latch	55297B	1	B119
N74298N	Quad 2-Input Mux with Storage	55300X	2	B122

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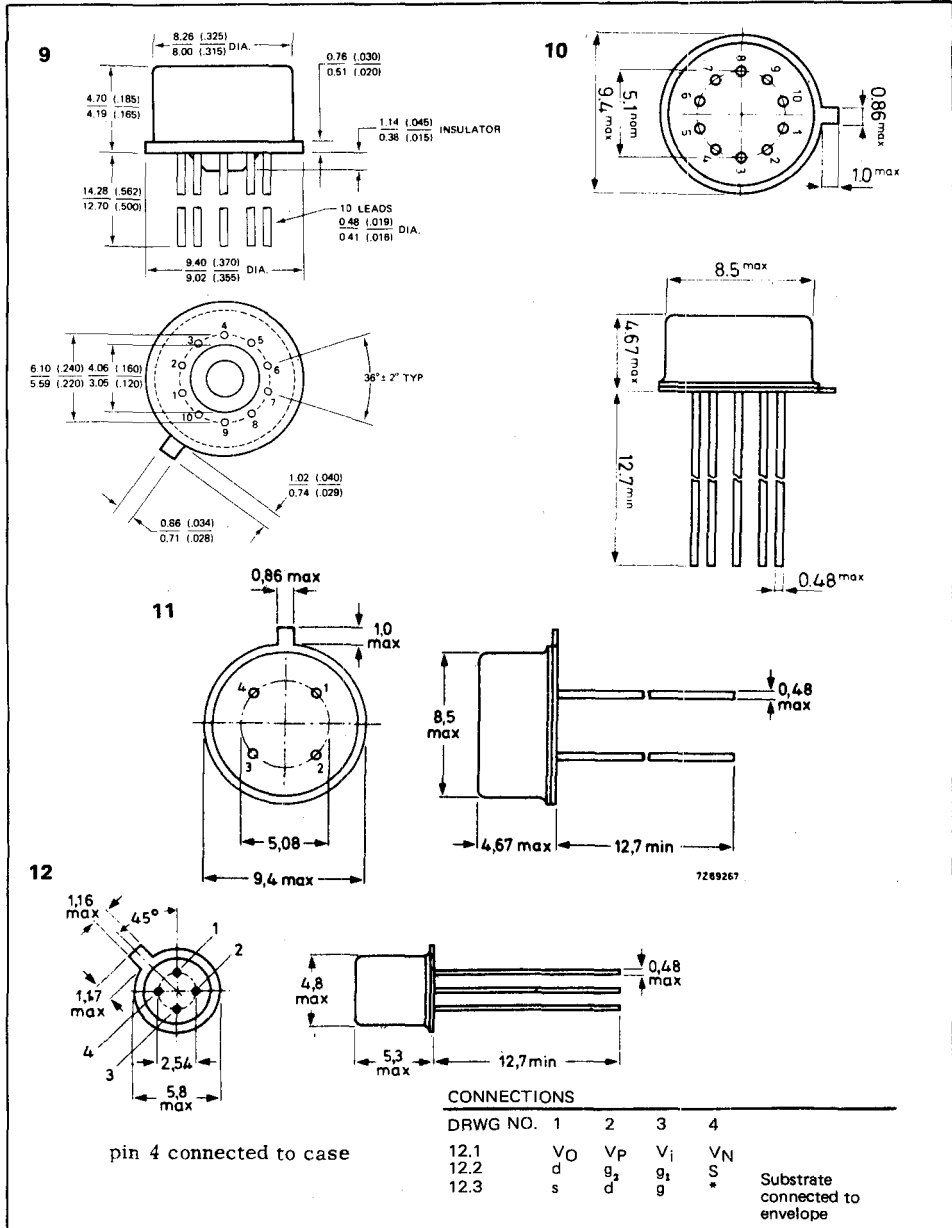
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Outline Drawings



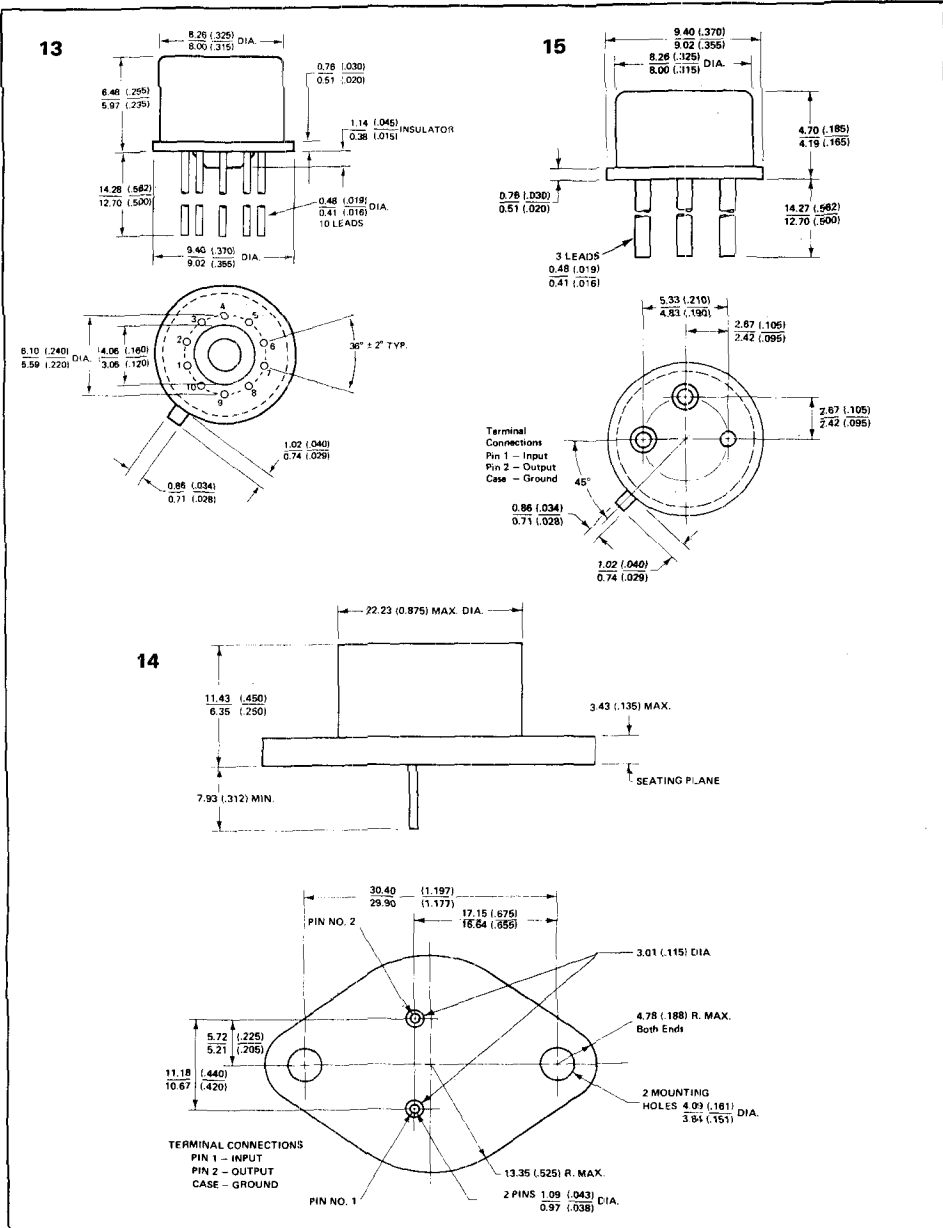
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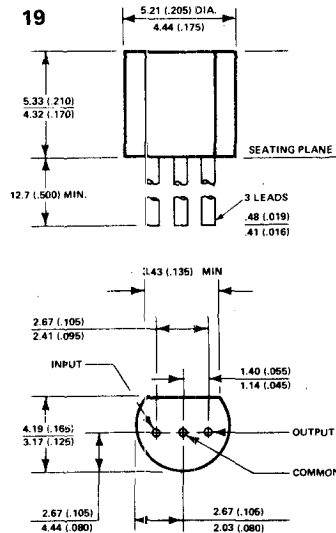
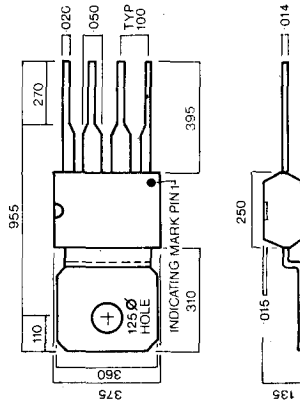
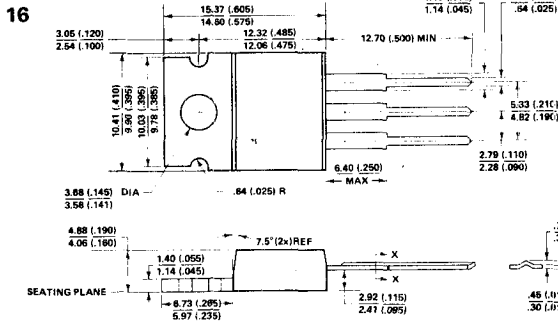
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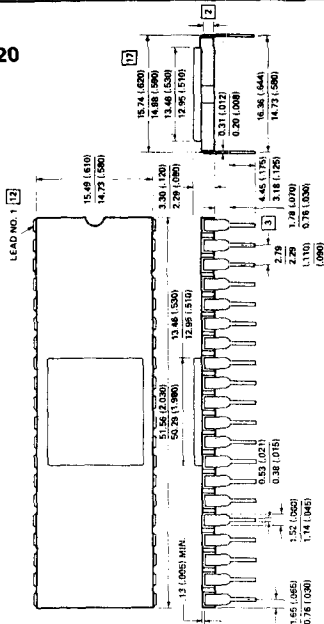




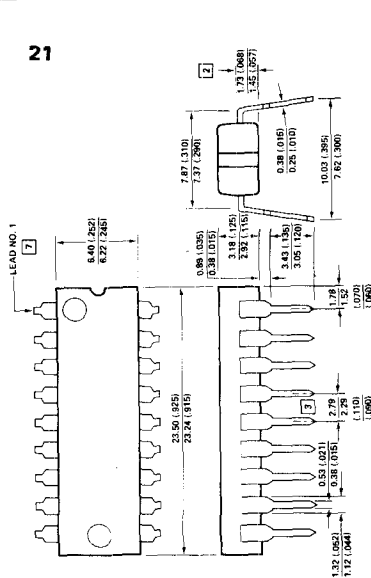
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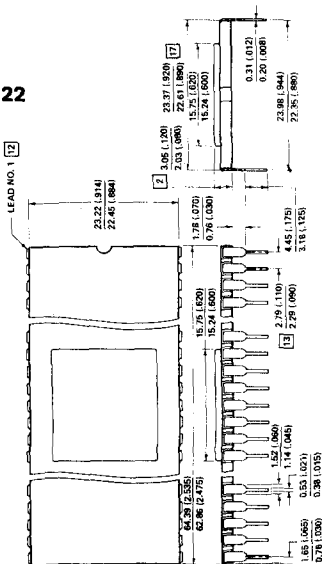
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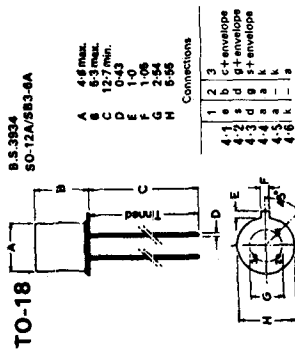
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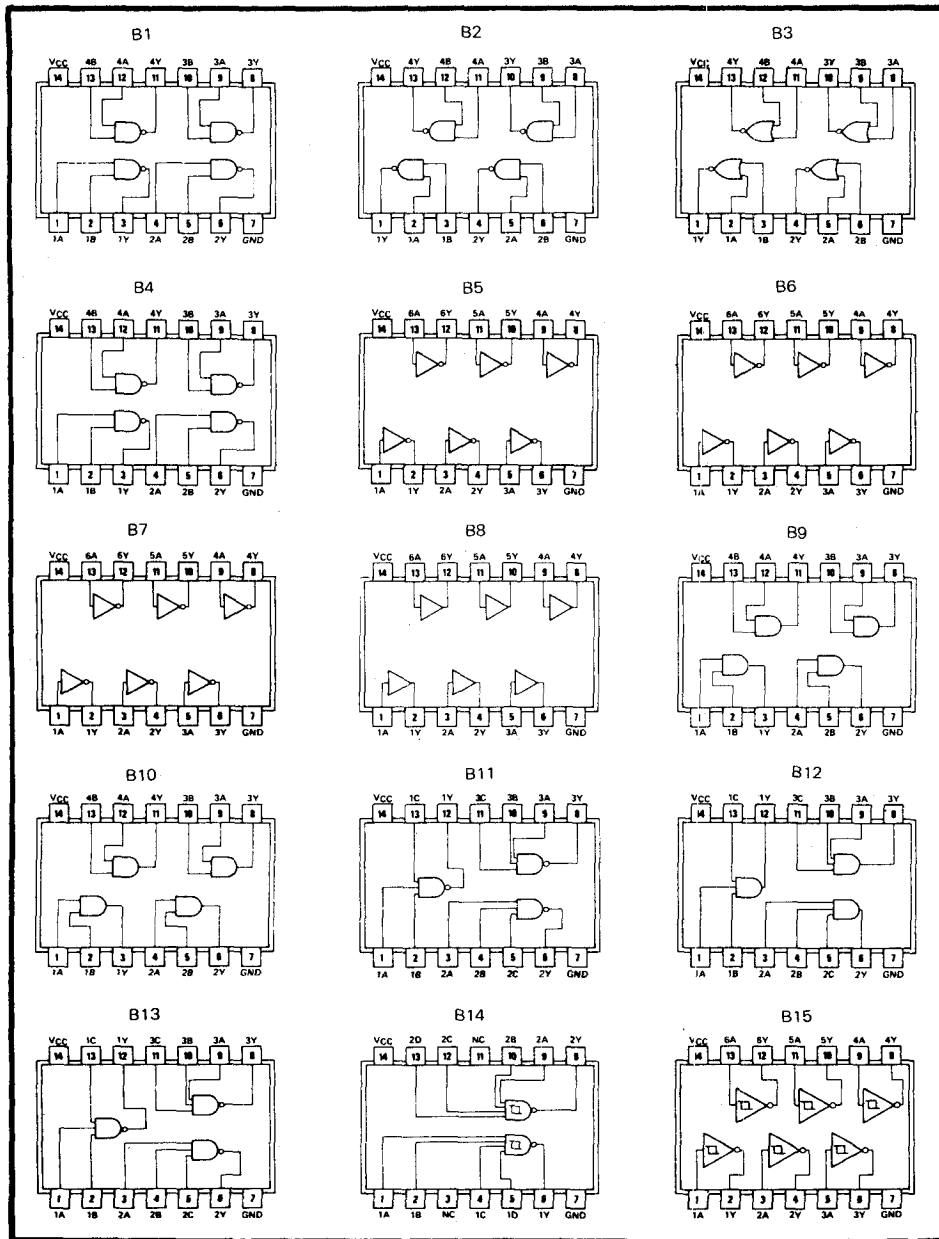


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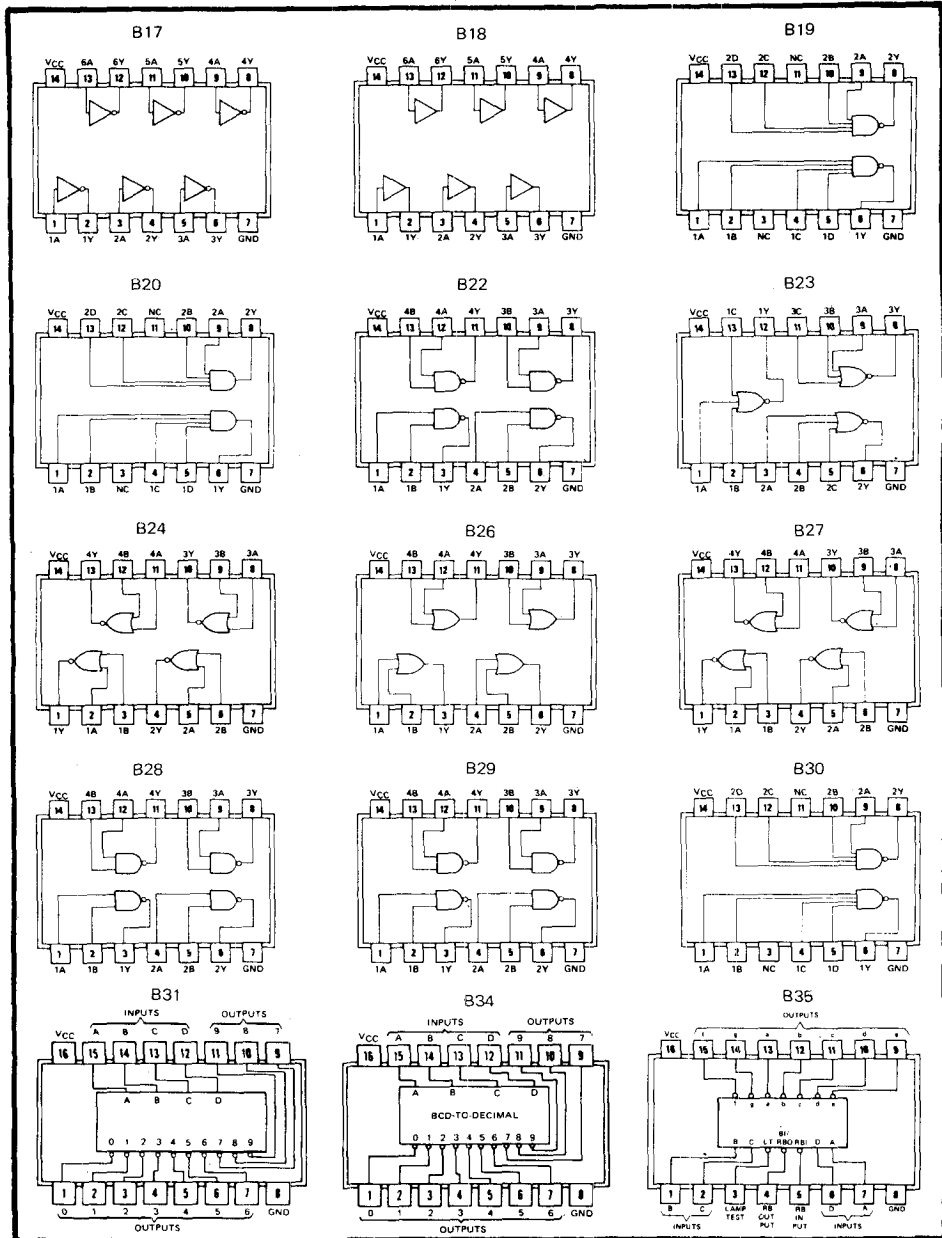


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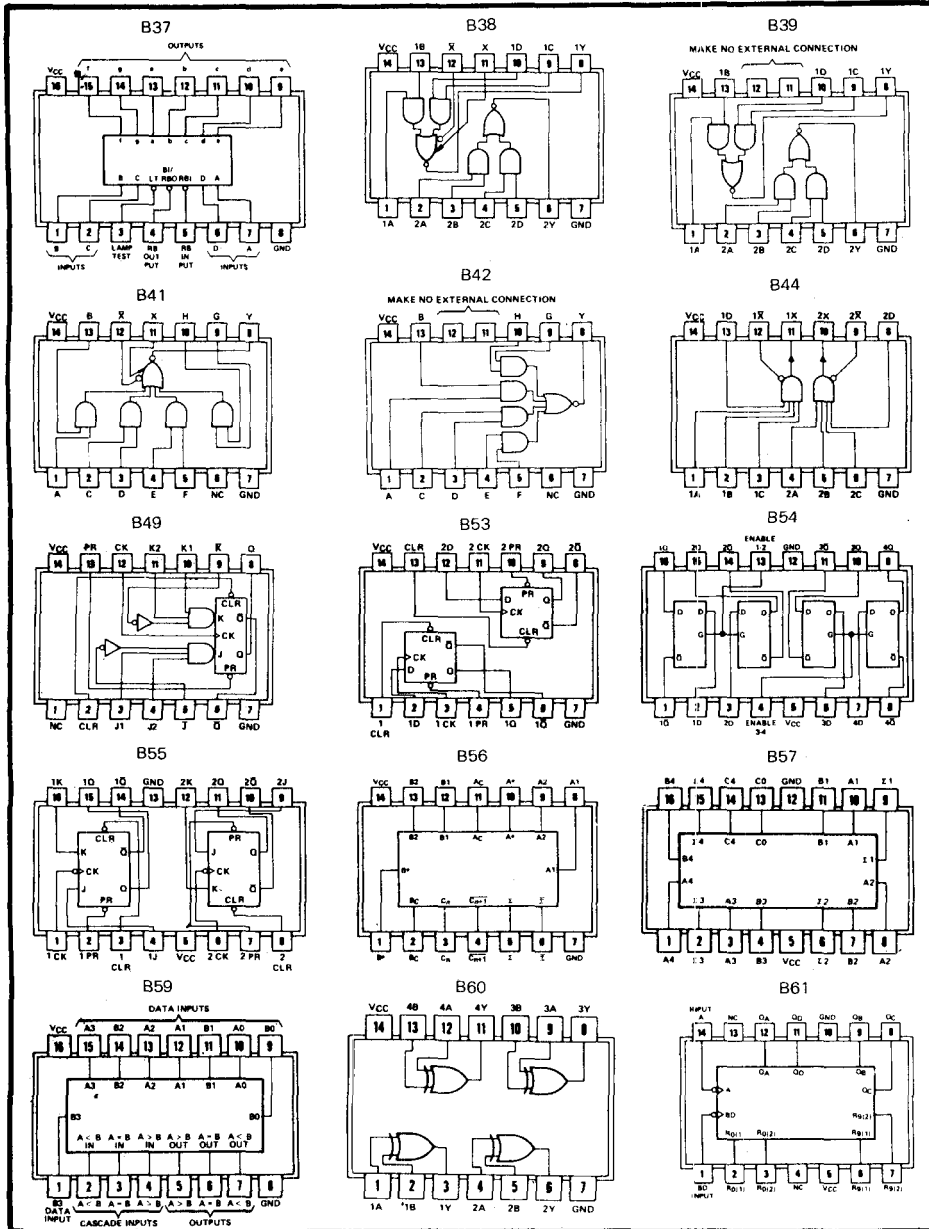
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Connection Diagram



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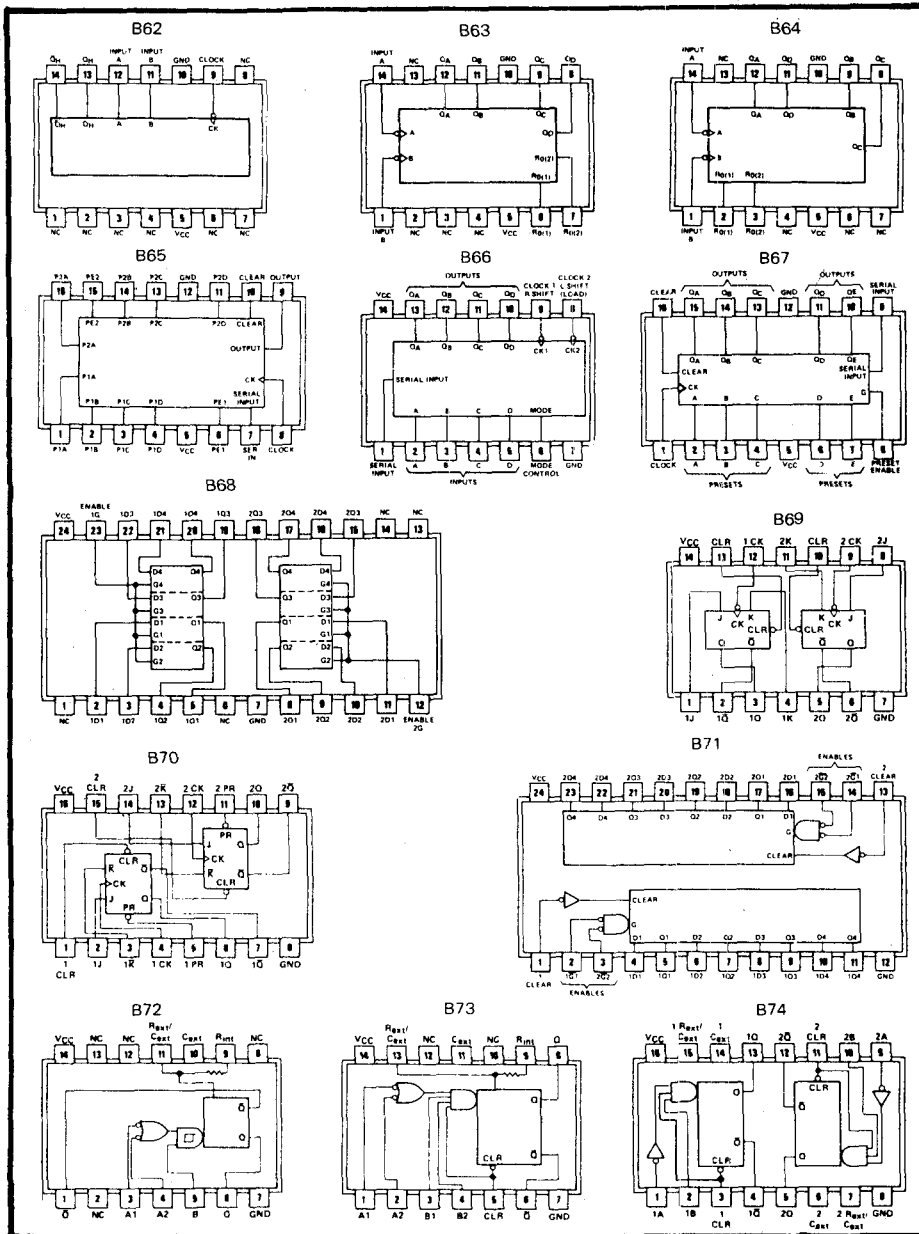
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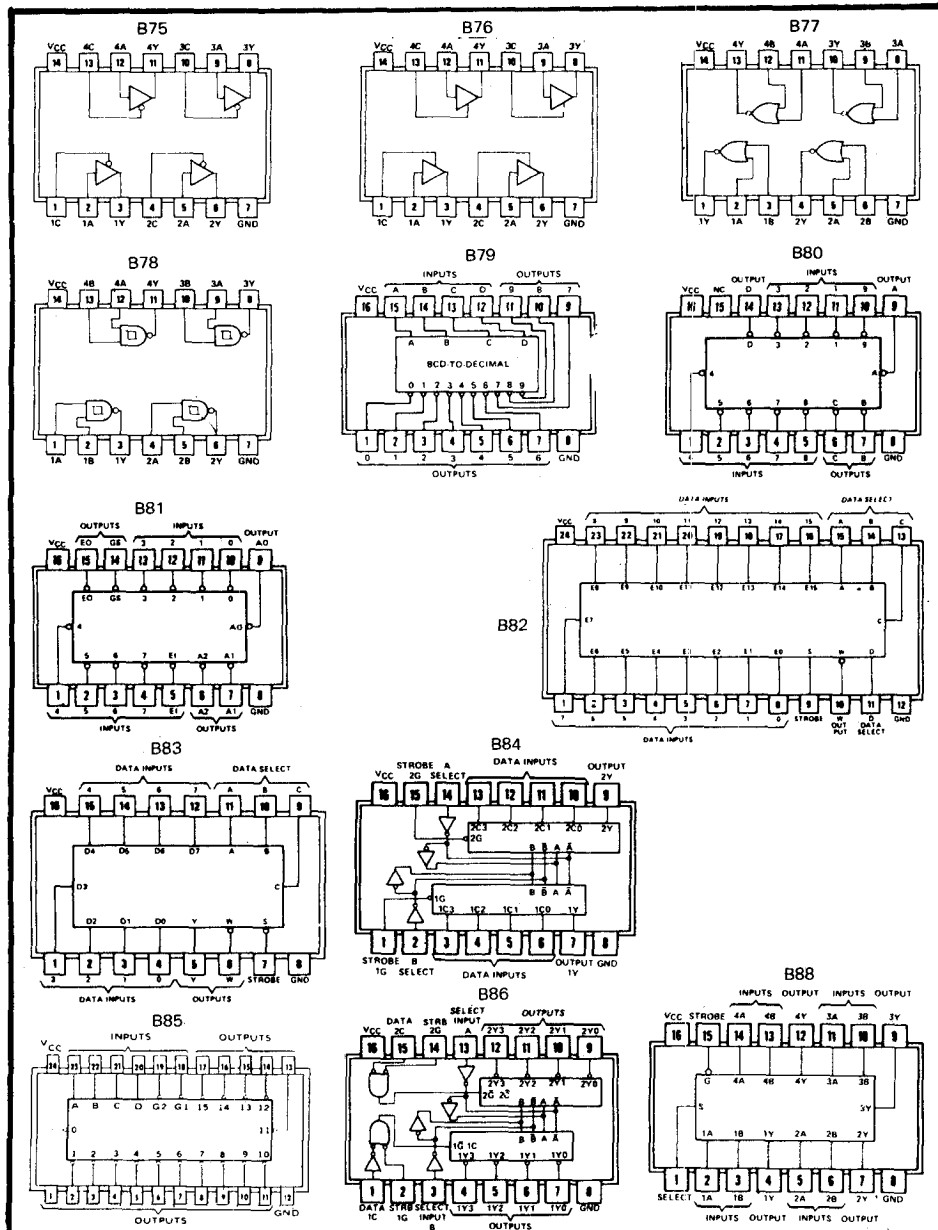


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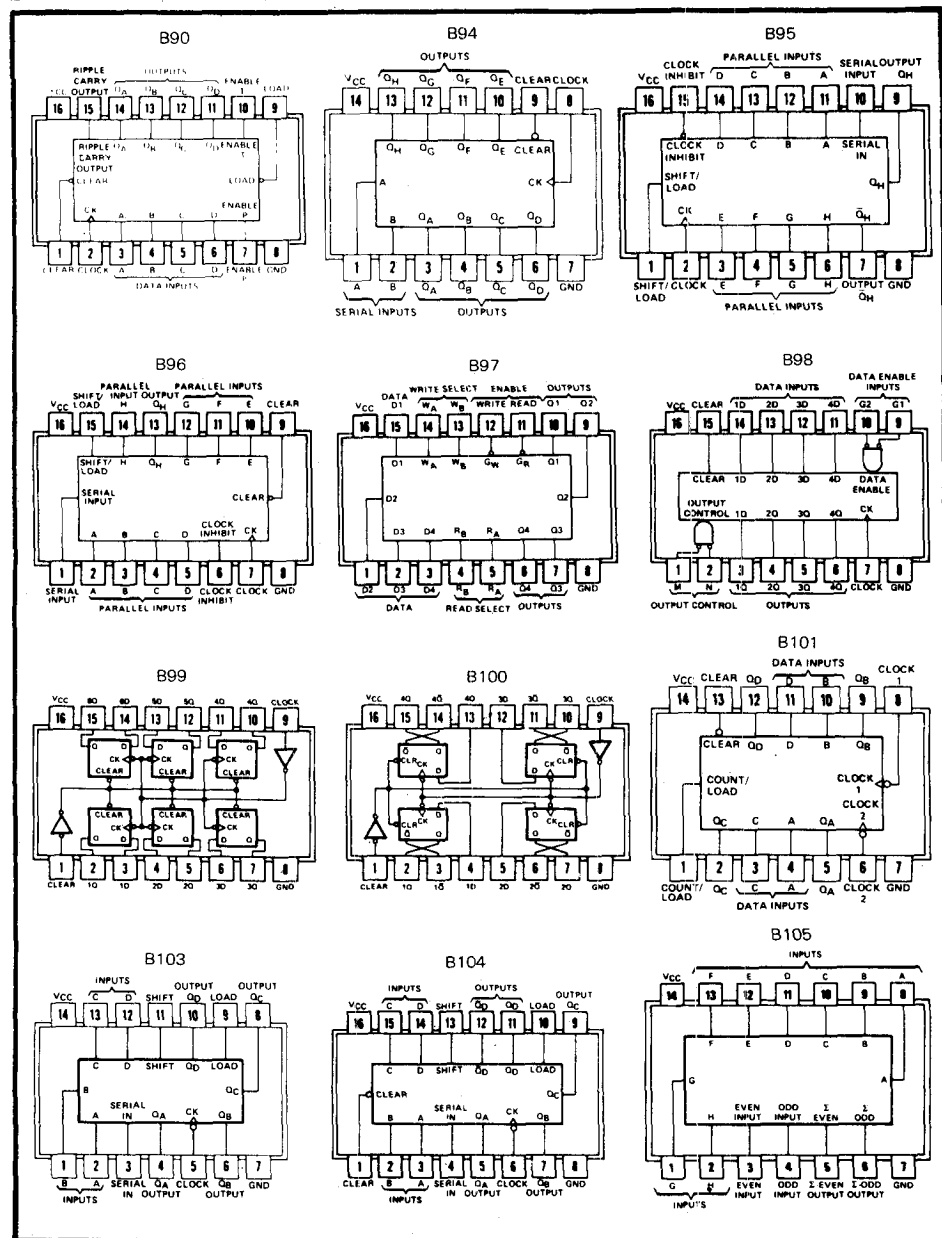
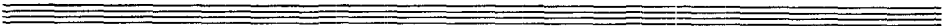
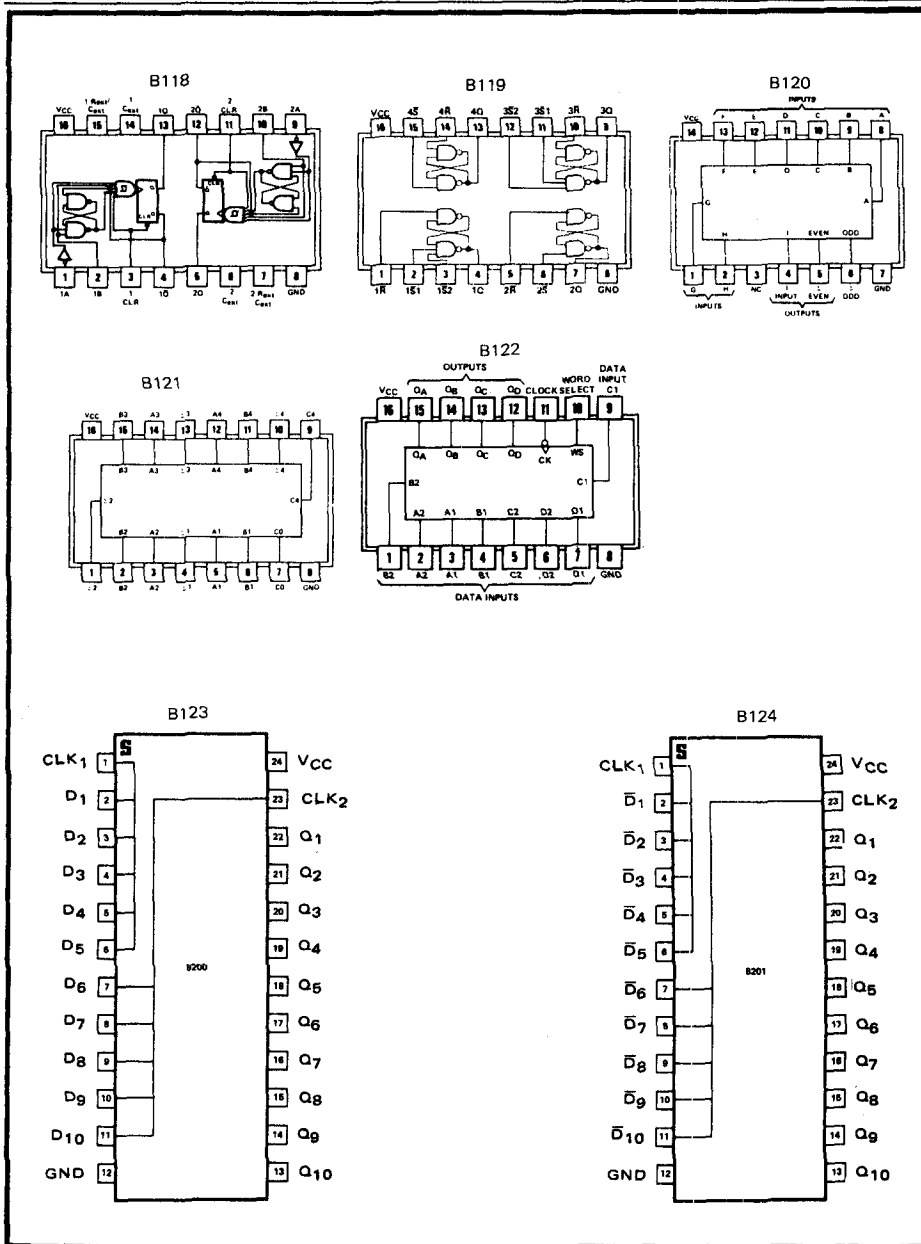


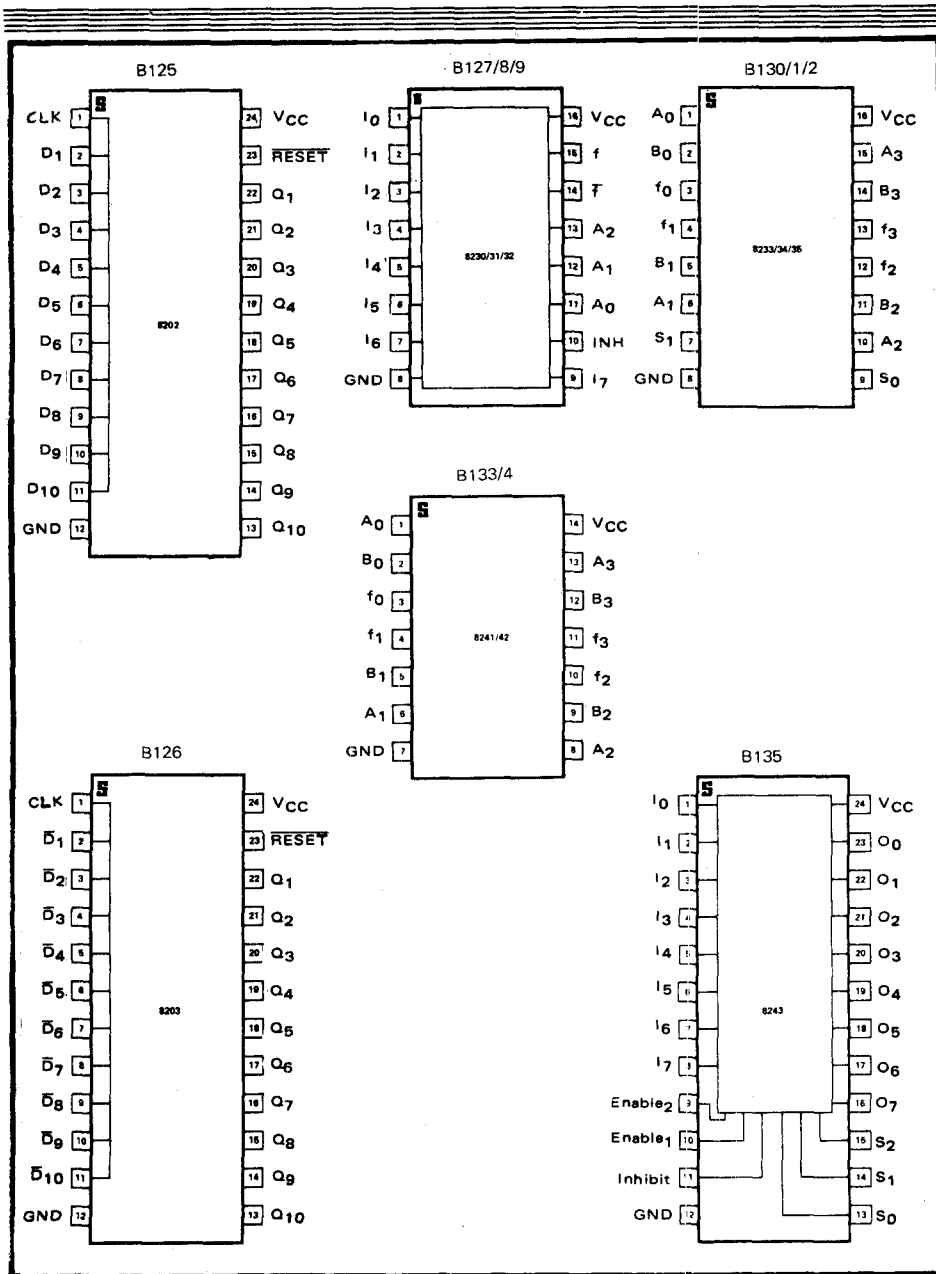
Figure 1: Schematic representation of the experimental design. The figure shows a timeline of the experiment. It starts with a 'Pretest' phase, followed by a 'Main Experiment' phase. The Main Experiment is divided into two parts: 'Part 1' and 'Part 2'. Part 1 involves a 'Pretest' and a 'Main Experiment' with 'Condition 1' and 'Condition 2'. Part 2 involves a 'Pretest' and a 'Main Experiment' with 'Condition 1' and 'Condition 2'. The timeline ends with a 'Posttest' phase.

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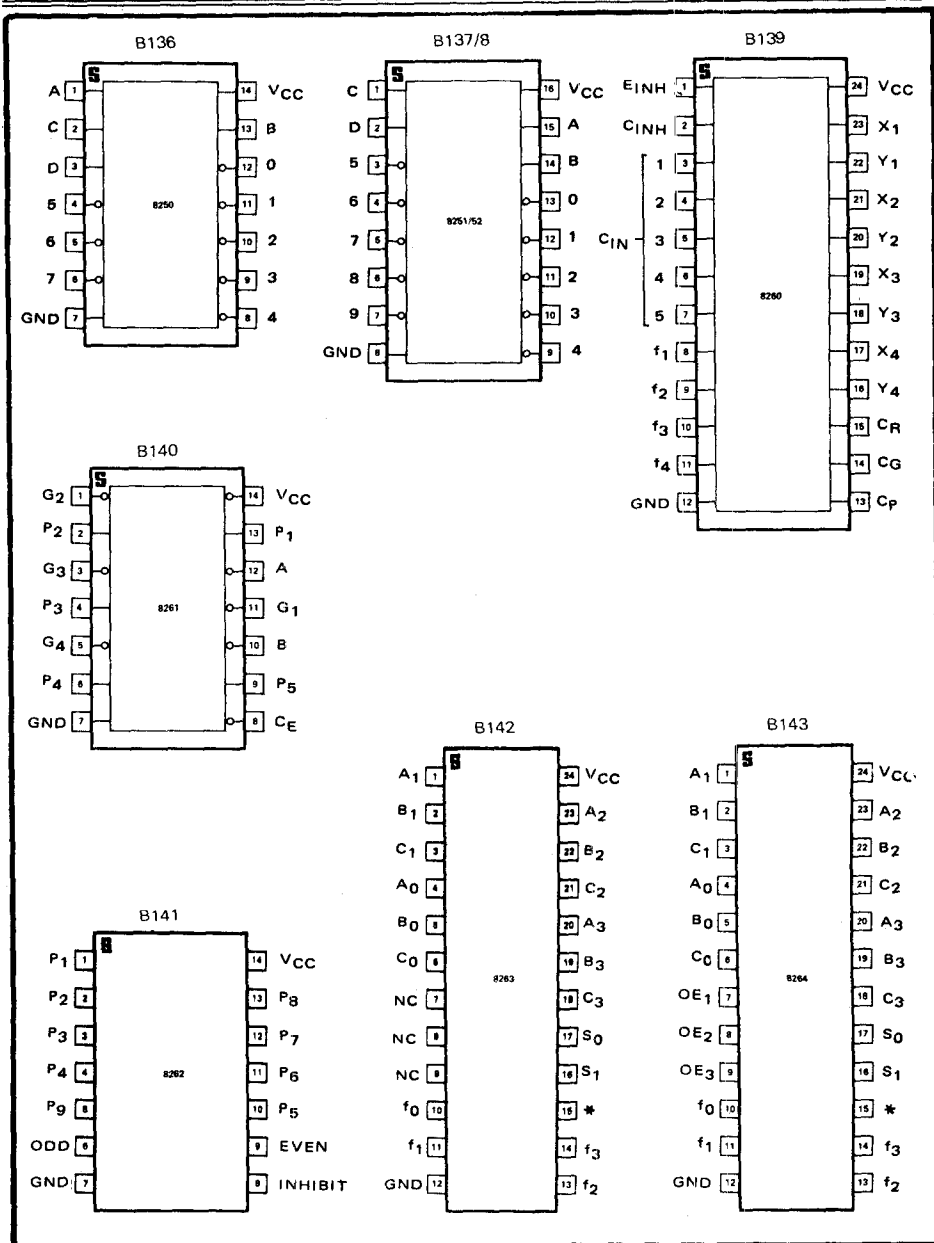
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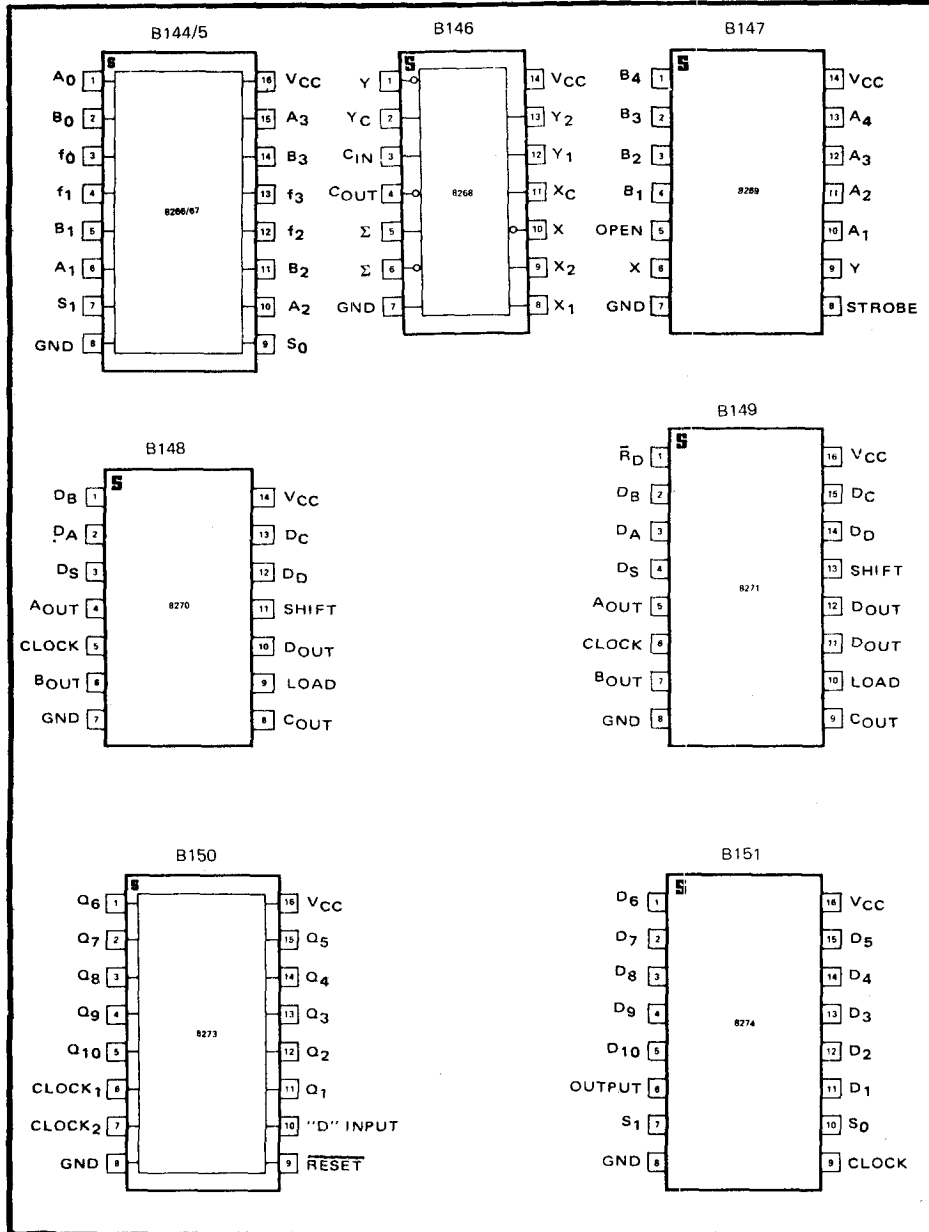
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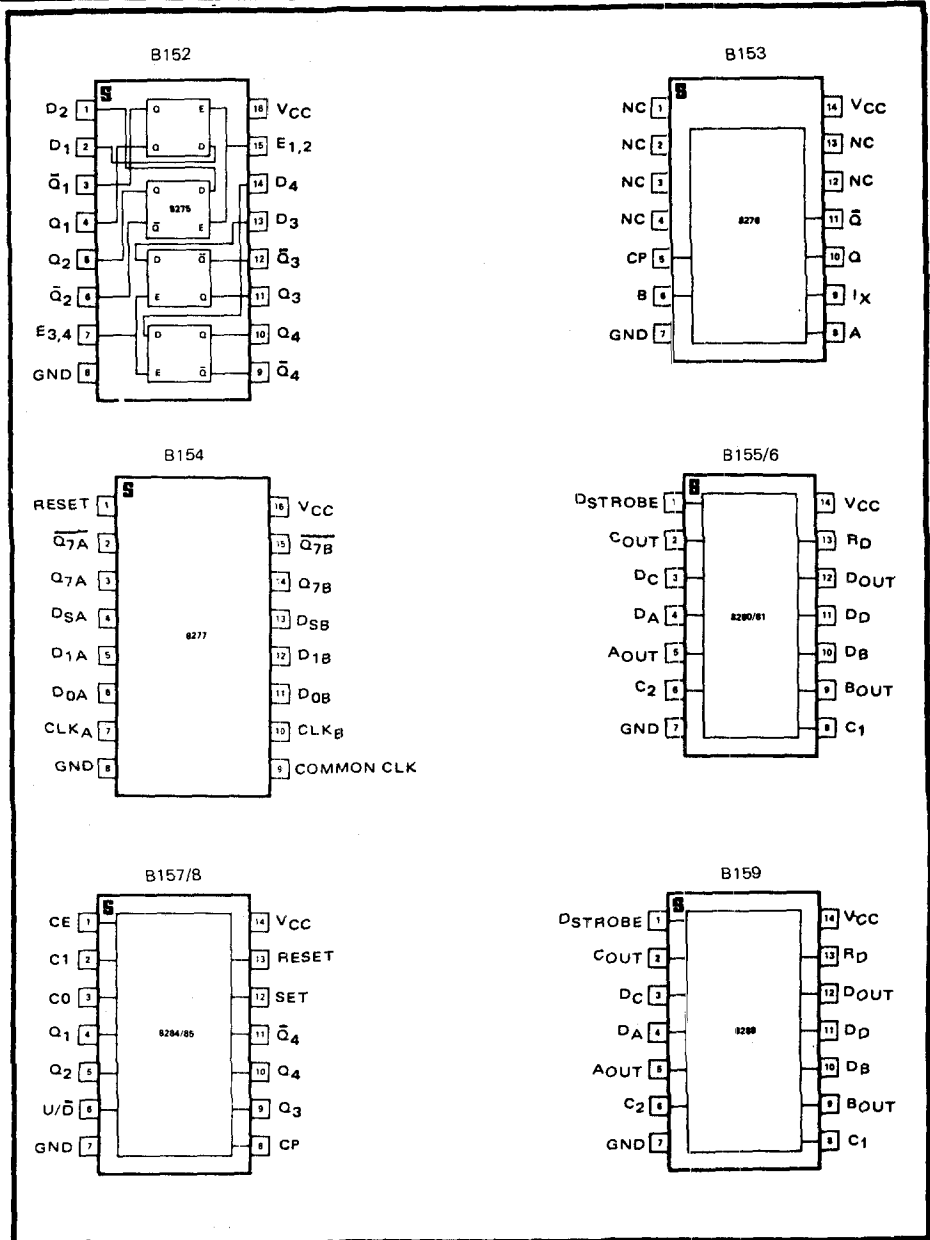
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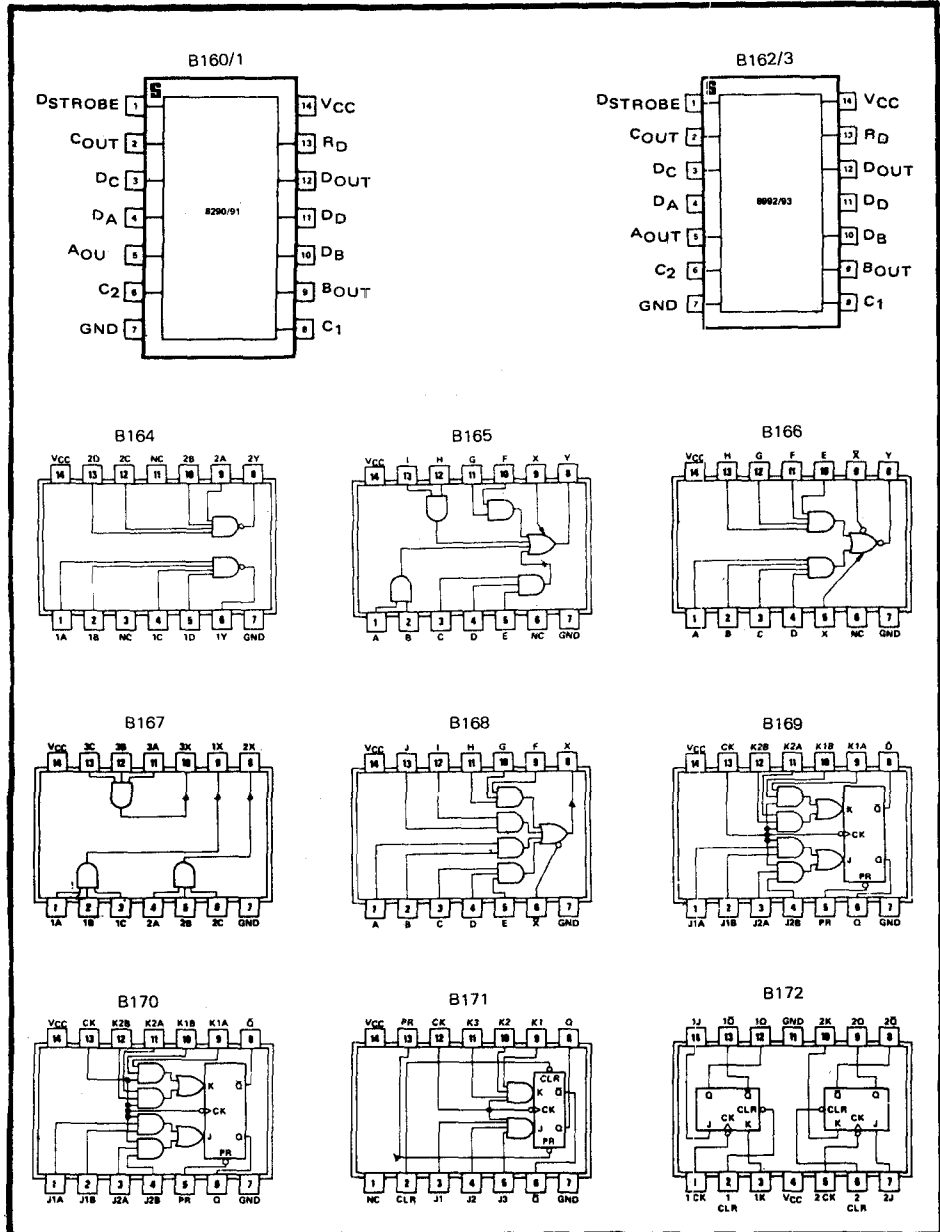
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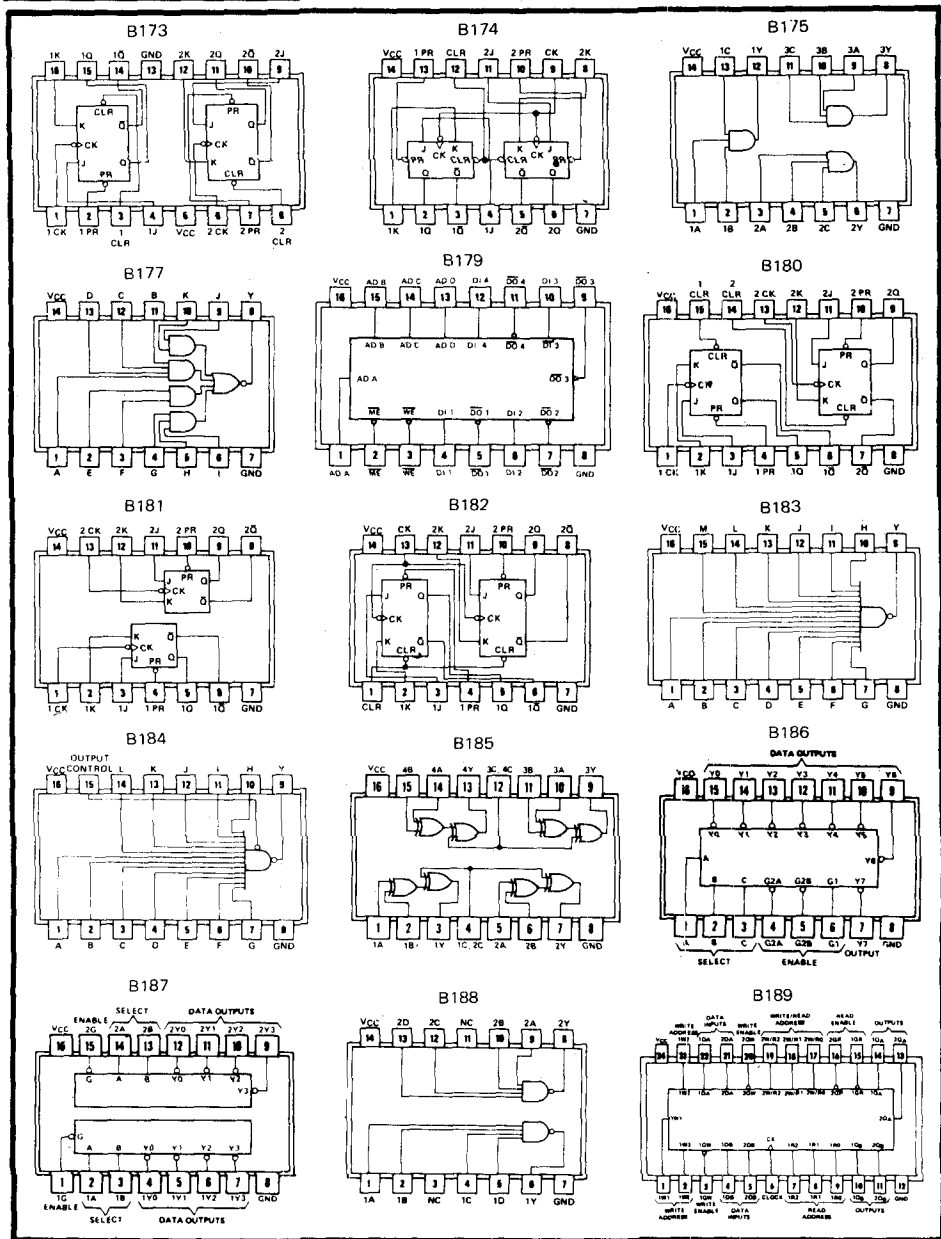


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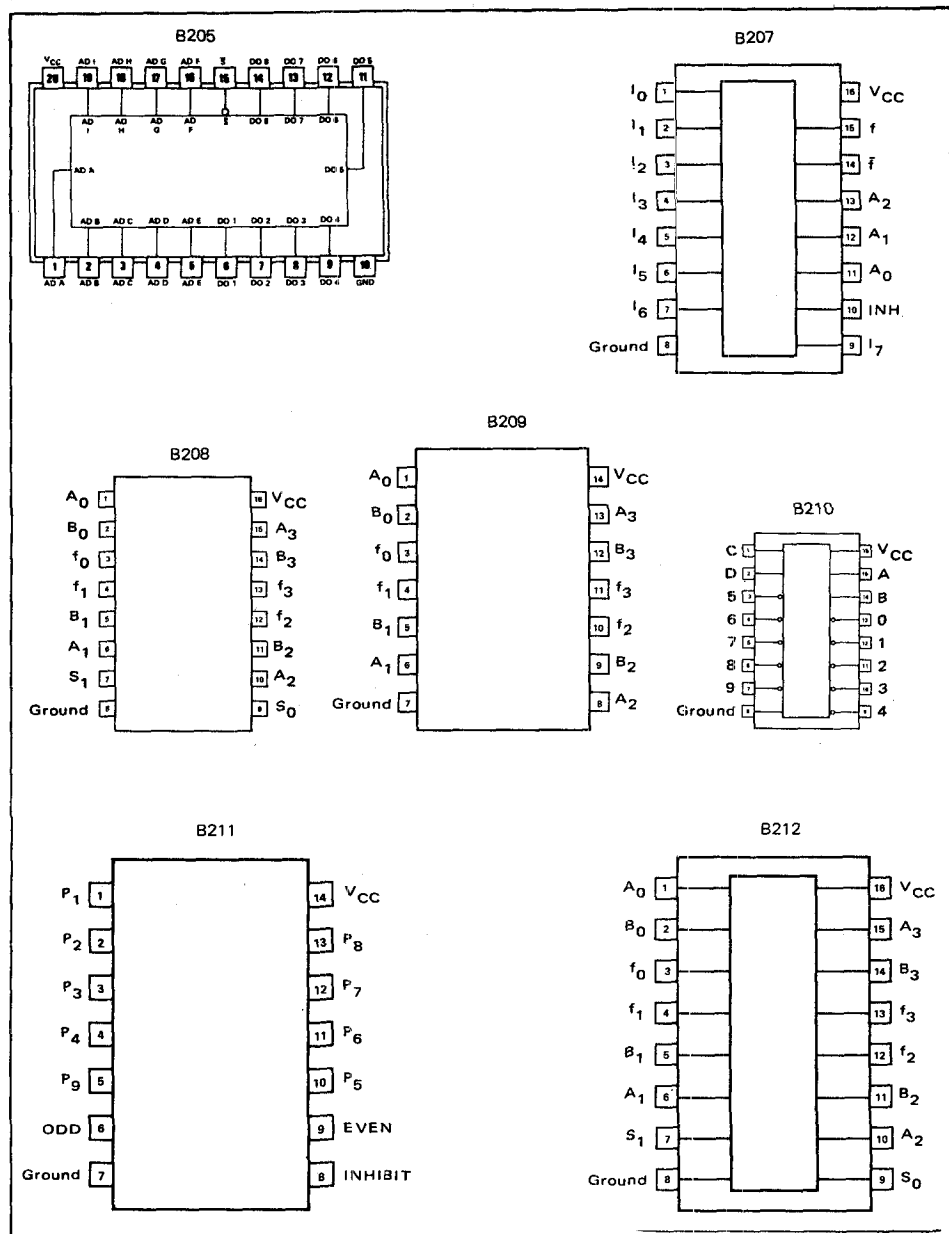
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1. The first step is to identify the problem. This involves understanding the current situation and what needs to be achieved.

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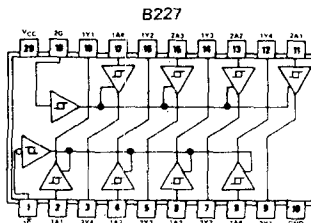
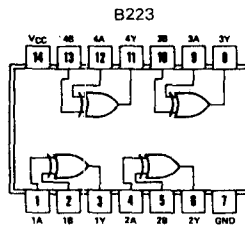
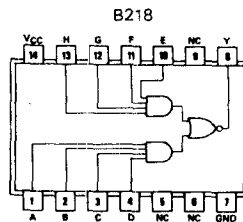
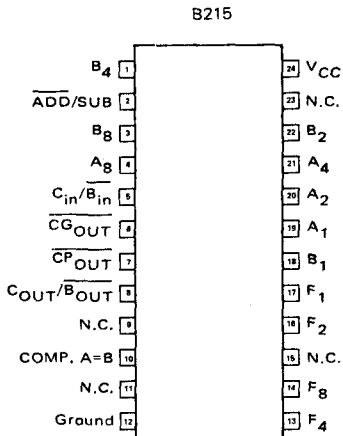
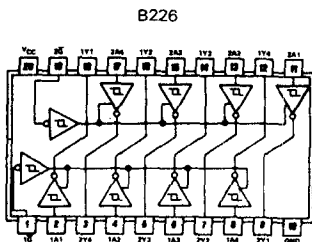
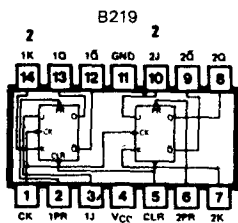
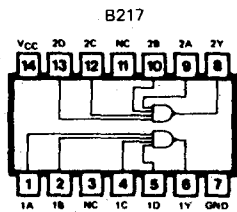
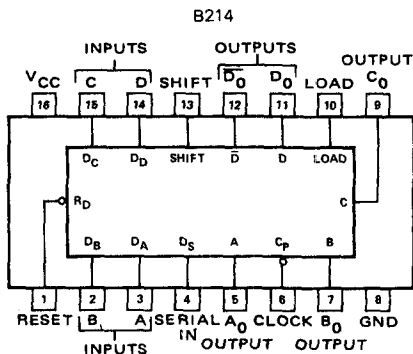
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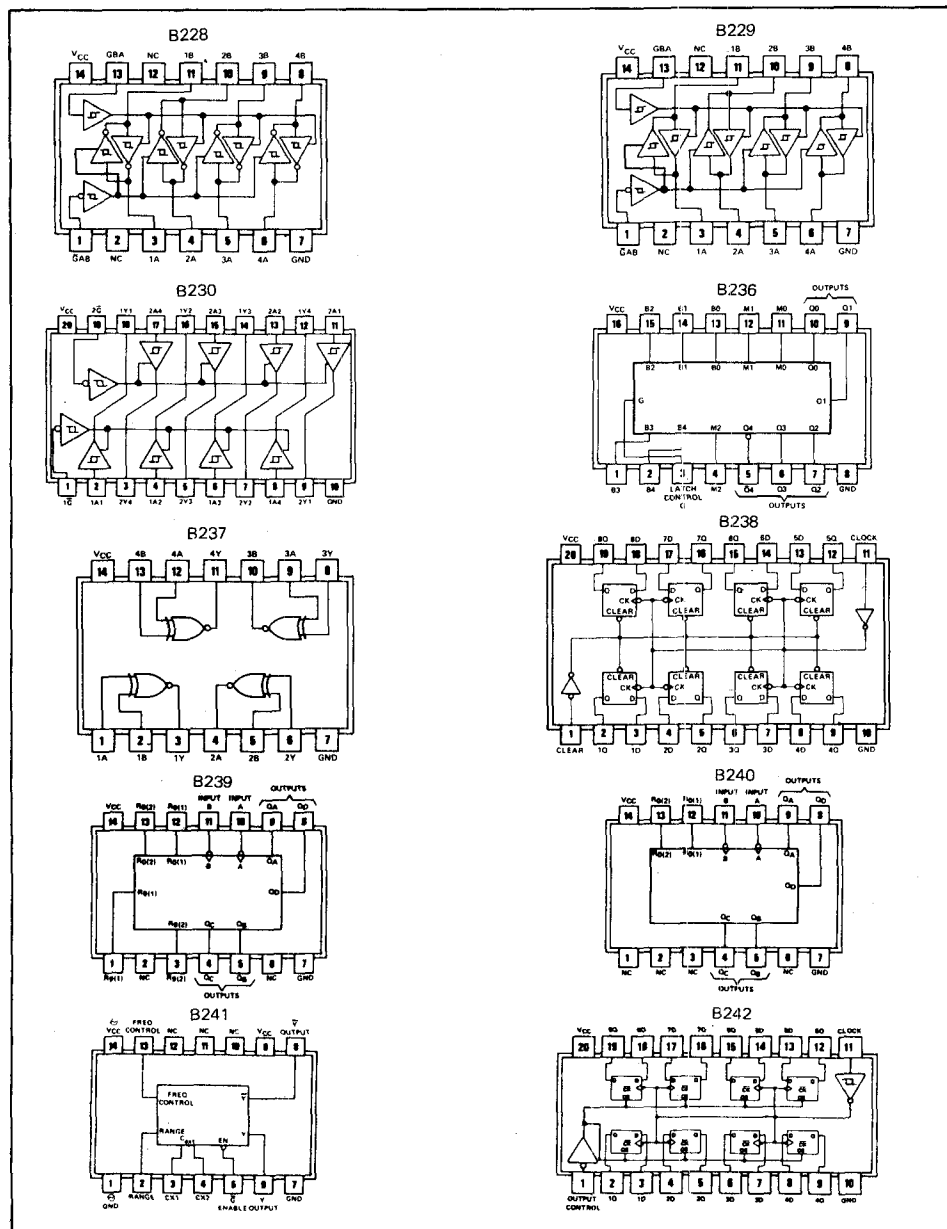


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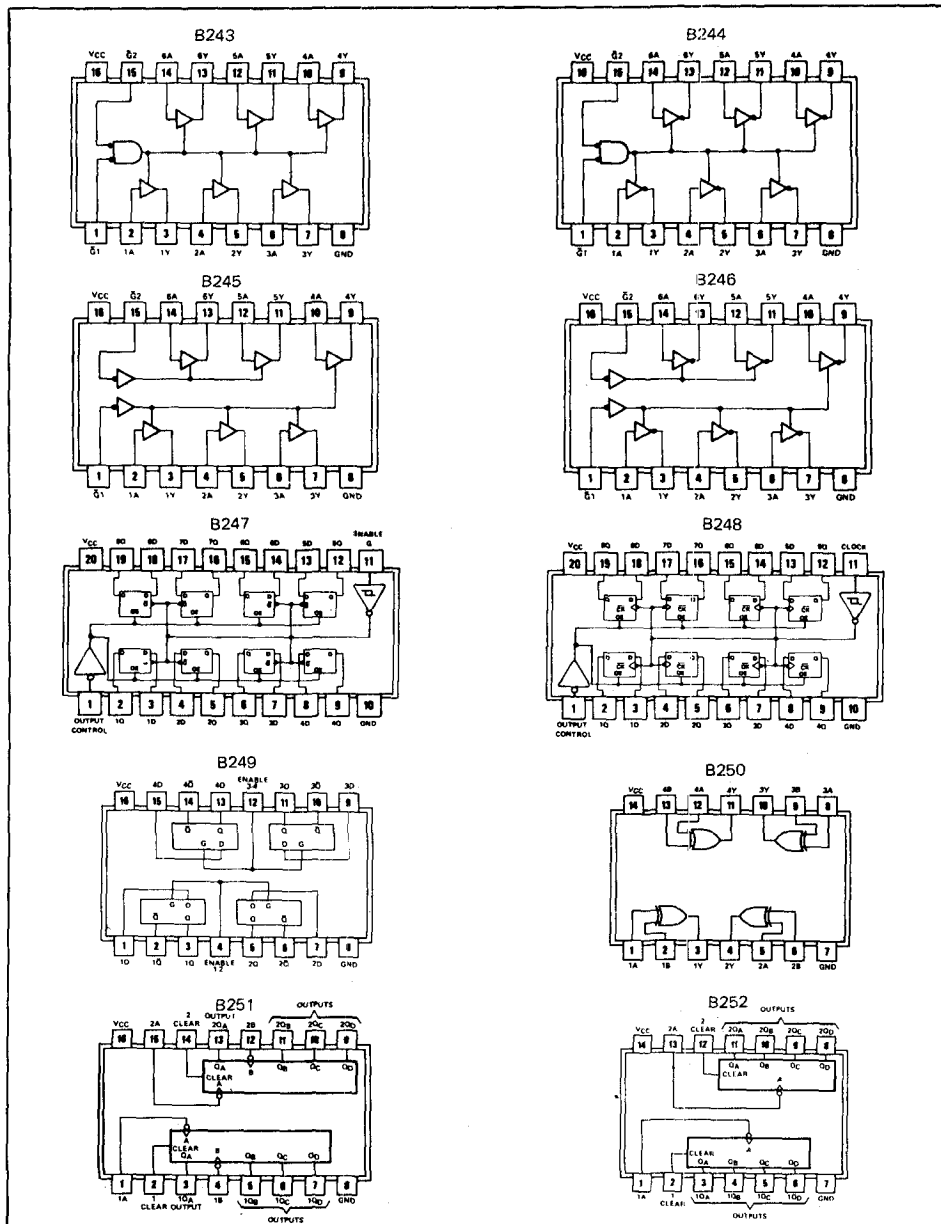


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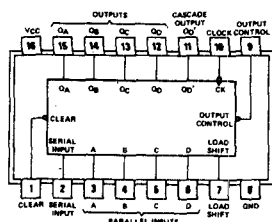
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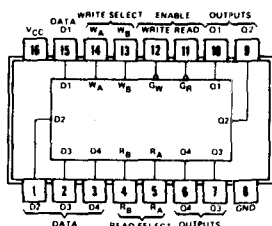
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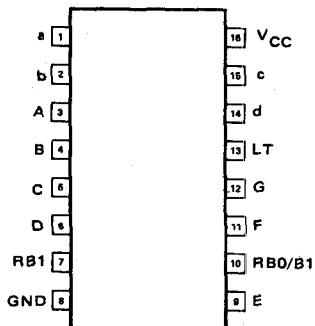
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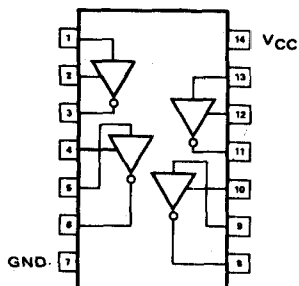
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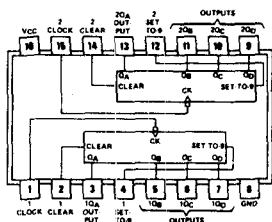
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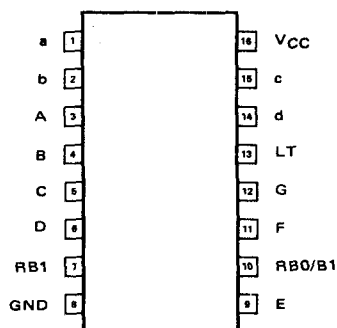
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