



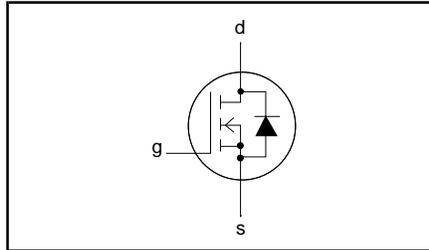
N-channel TrenchMOS™ transistor

PSMN057-200P

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

| |
|-------------------------------------|
| $V_{DSS} = 200\text{ V}$ |
| $I_D = 39\text{ A}$ |
| $R_{DS(ON)} \leq 57\text{ m}\Omega$ |

GENERAL DESCRIPTION

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

Applications:-

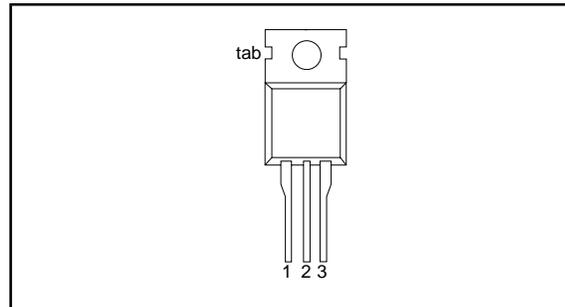
- d.c. to d.c. converters
- switched mode power supplies

The PSMN060-200P is supplied in the SOT78 (TO220AB) conventional leaded package.

PINNING

SOT78 (TO220AB)

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | gate |
| 2 | drain |
| 3 | source |
| tab | drain |



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--|--|------|----------|------------------|
| V_{DSS} | Drain-source voltage | $T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$ | - | 200 | V |
| V_{DGR} | Drain-gate voltage | $T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 200 | V |
| V_{GS} | Gate-source voltage | | - | ± 20 | V |
| I_D | Continuous drain current | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 39 | A |
| | | $T_{mb} = 100\text{ }^\circ\text{C}$ | - | 27.5 | A |
| I_{DM} | Pulsed drain current | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 156 | A |
| P_D | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 250 | W |
| T_j, T_{stg} | Operating junction and storage temperature | | - 55 | 175 | $^\circ\text{C}$ |

SiliconMAX

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------|----------------------------------|--|------|------|------|
| E_{AS} | Non-repetitive avalanche energy | Unclamped inductive load, $I_{AS} = 35$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 50$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; | - | 300 | mJ |
| I_{AS} | Non-repetitive avalanche current | | - | 35 | A |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|----------------|--|-------------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | | - | 0.6 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | in free air | 60 | - | K/W |

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|----------------------------------|---|-----------------|---------------|---------------|--------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$ | 200 178 | - - | - - | V V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$ | 2.0 1.0 - | 3.0 - - | 4.0 - 6 | V V V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 17$ A $T_j = 175^\circ\text{C}$ | - - | 41 - | 57 165 | m Ω m Ω |
| I_{GSS} | Gate source leakage current | $V_{GS} = \pm 10$ V; $V_{DS} = 0$ V | - | 2 | 100 | nA |
| I_{DSS} | Zero gate voltage drain current | $V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 175^\circ\text{C}$ | - | 0.03 | 10 500 | μ A μ A |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 39$ A; $V_{DD} = 160$ V; $V_{GS} = 10$ V | - | 96 | - | nC |
| Q_{gs} | Gate-source charge | | - | 13 | - | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 37 | 50 | nC |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD} = 100$ V; $R_D = 2.7$ Ω ; $V_{GS} = 10$ V; $R_G = 5.6$ Ω Resistive load | - | 18 | - | ns |
| t_r | Turn-on rise time | | - | 58 | - | ns |
| $t_{d\ off}$ | Turn-off delay time | | - | 105 | - | ns |
| t_f | Turn-off fall time | | - | 78 | - | ns |
| L_d | Internal drain inductance | Measured from tab to centre of die | - | 3.5 | - | nH |
| L_d | Internal drain inductance | Measured from drain lead to centre of die | - | 4.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz | - | 3750 | - | pF |
| C_{oss} | Output capacitance | | - | 385 | - | pF |
| C_{rss} | Feedback capacitance | | - | 180 | - | pF |



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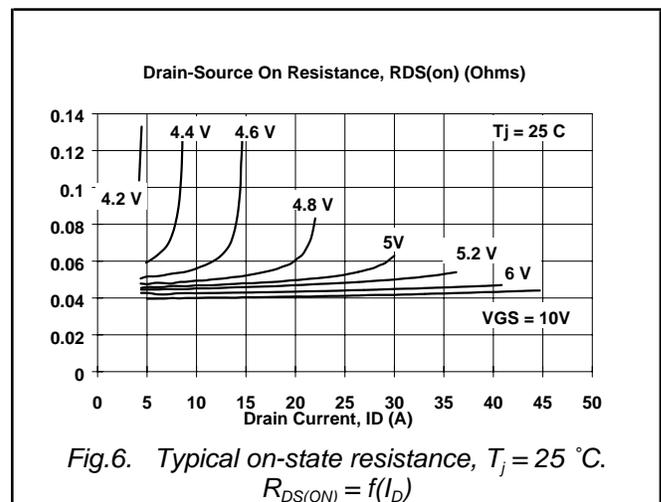
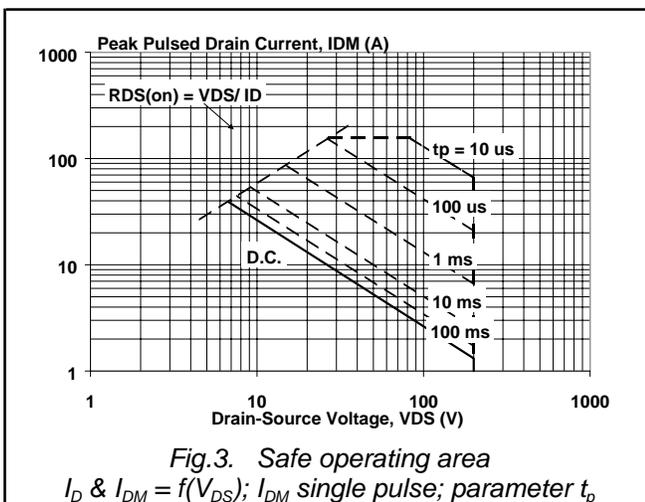
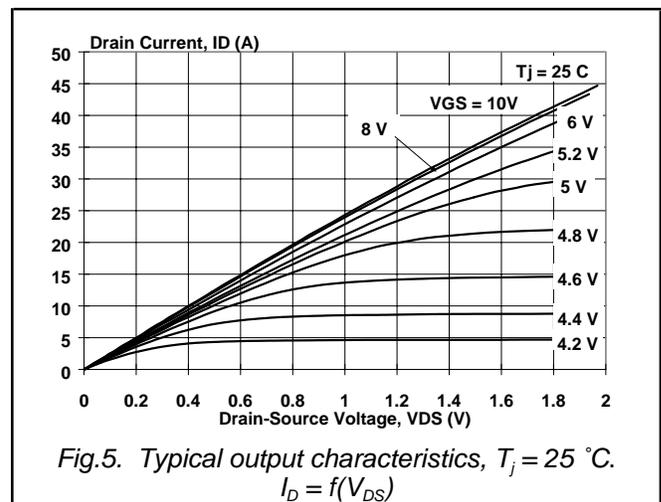
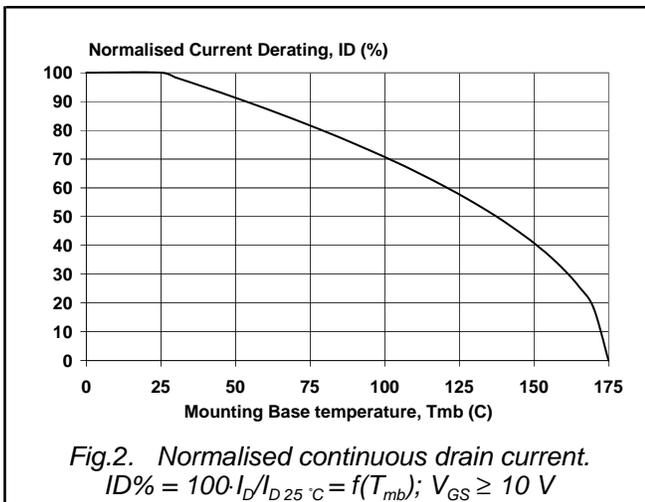
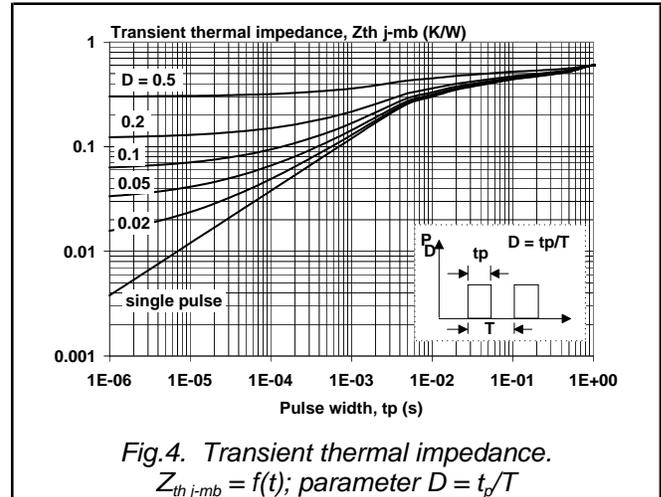
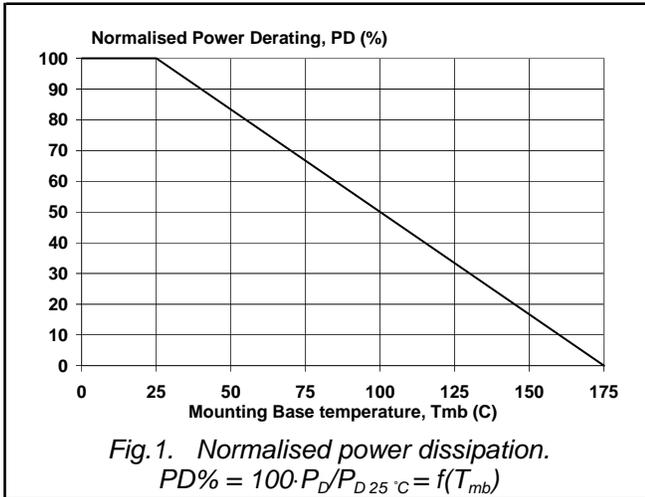
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|--|---|------|------|------|------|
| I_S | Continuous source current (body diode) | | - | - | 39 | A |
| I_{SM} | Pulsed source current (body diode) | | - | - | 156 | A |
| V_{SD} | Diode forward voltage | $I_F = 25\text{ A}; V_{GS} = 0\text{ V}$ | - | 0.85 | 1.2 | V |
| t_{rr} | Reverse recovery time | $I_F = 20\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ | - | 133 | - | ns |
| Q_{rr} | Reverse recovery charge | $V_{GS} = 0\text{ V}; V_R = 30\text{ V}$ | - | 895 | - | nC |



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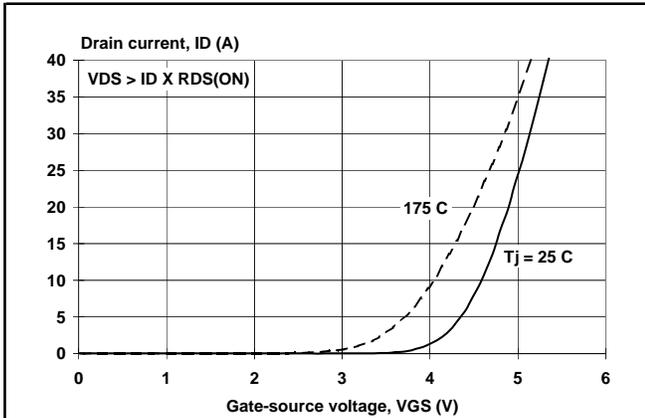


Fig. 7. Typical transfer characteristics.

$$I_D = f(V_{GS})$$

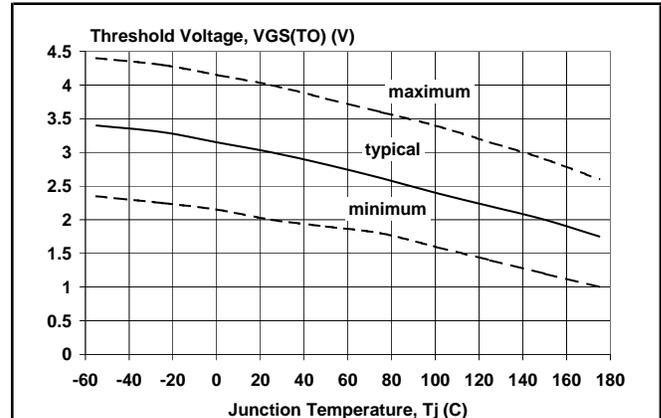


Fig. 10. Gate threshold voltage.

$$V_{GS(T0)} = f(T_j); \text{ conditions: } I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

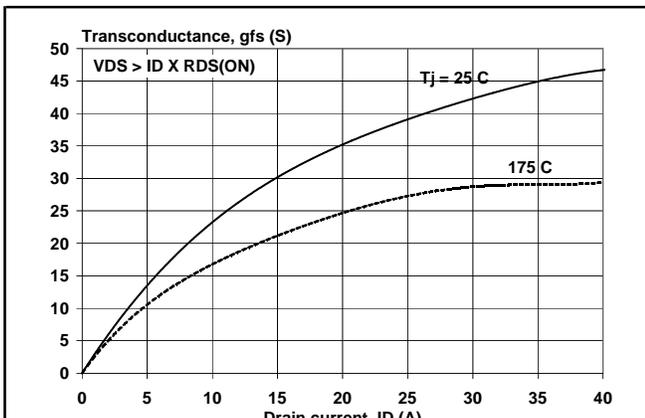


Fig. 8. Typical transconductance, $T_j = 25^\circ\text{C}$.

$$g_{fs} = f(I_D)$$

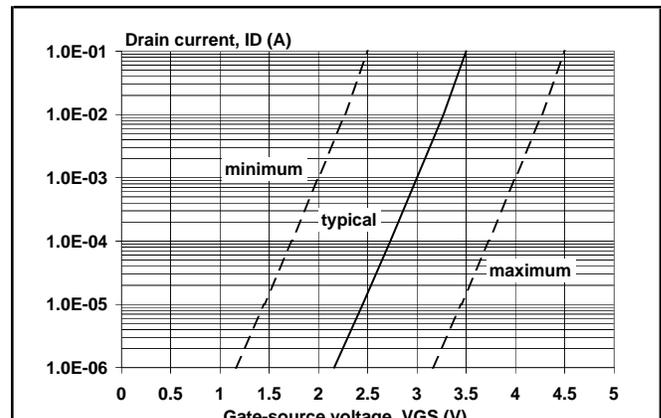


Fig. 11. Sub-threshold drain current.

$$I_D = f(V_{GS}); \text{ conditions: } T_j = 25^\circ\text{C}$$

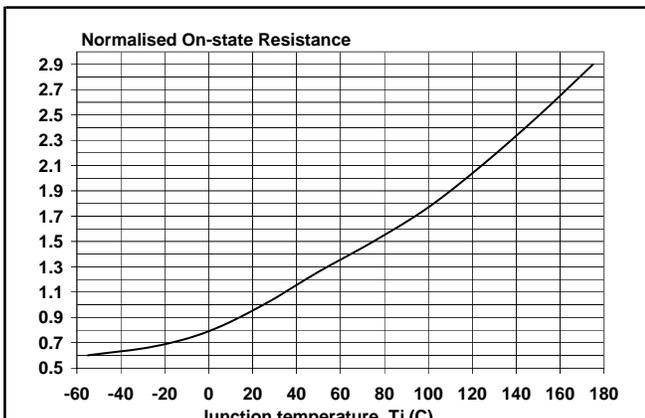


Fig. 9. Normalised drain-source on-state resistance.

$$R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$$

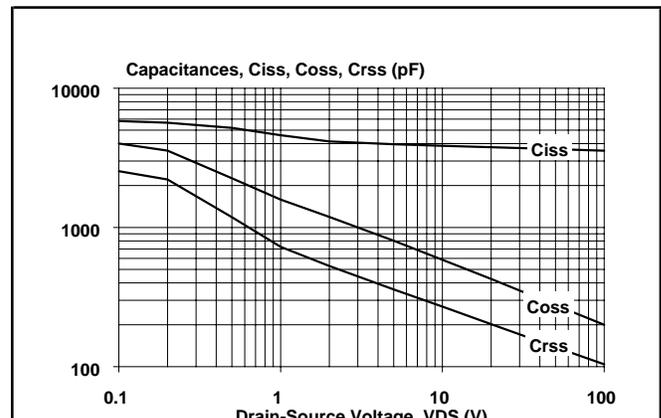


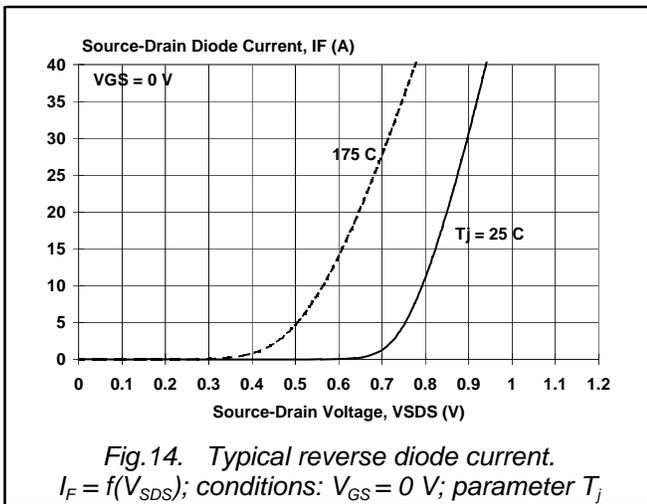
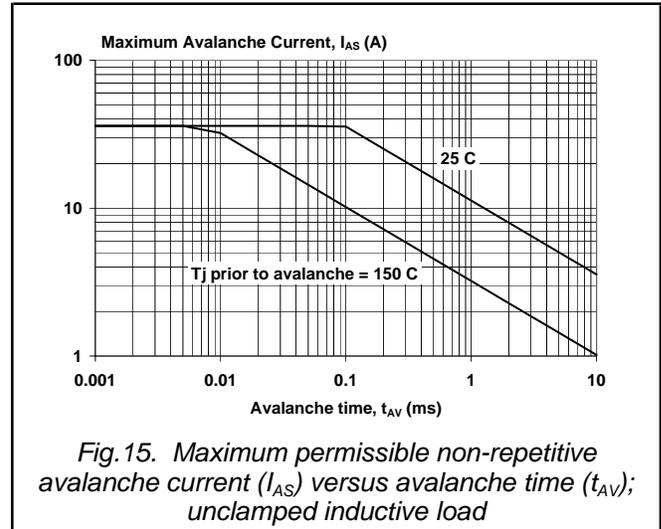
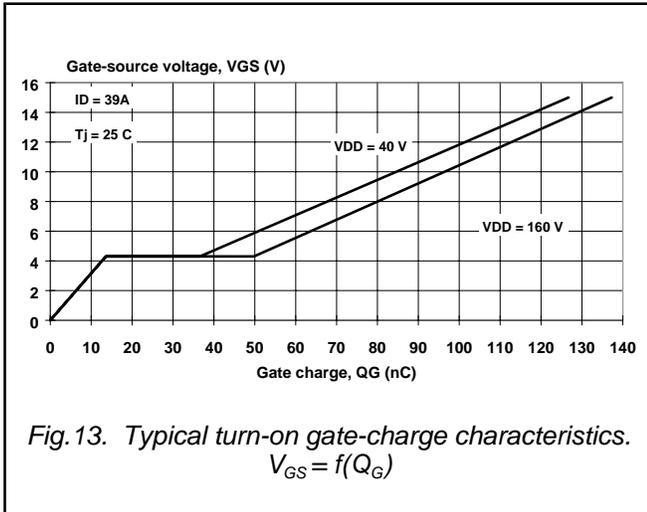
Fig. 12. Typical capacitances, $C_{iss}, C_{oss}, C_{rss}$.

$$C = f(V_{DS}); \text{ conditions: } V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



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MECHANICAL DATA

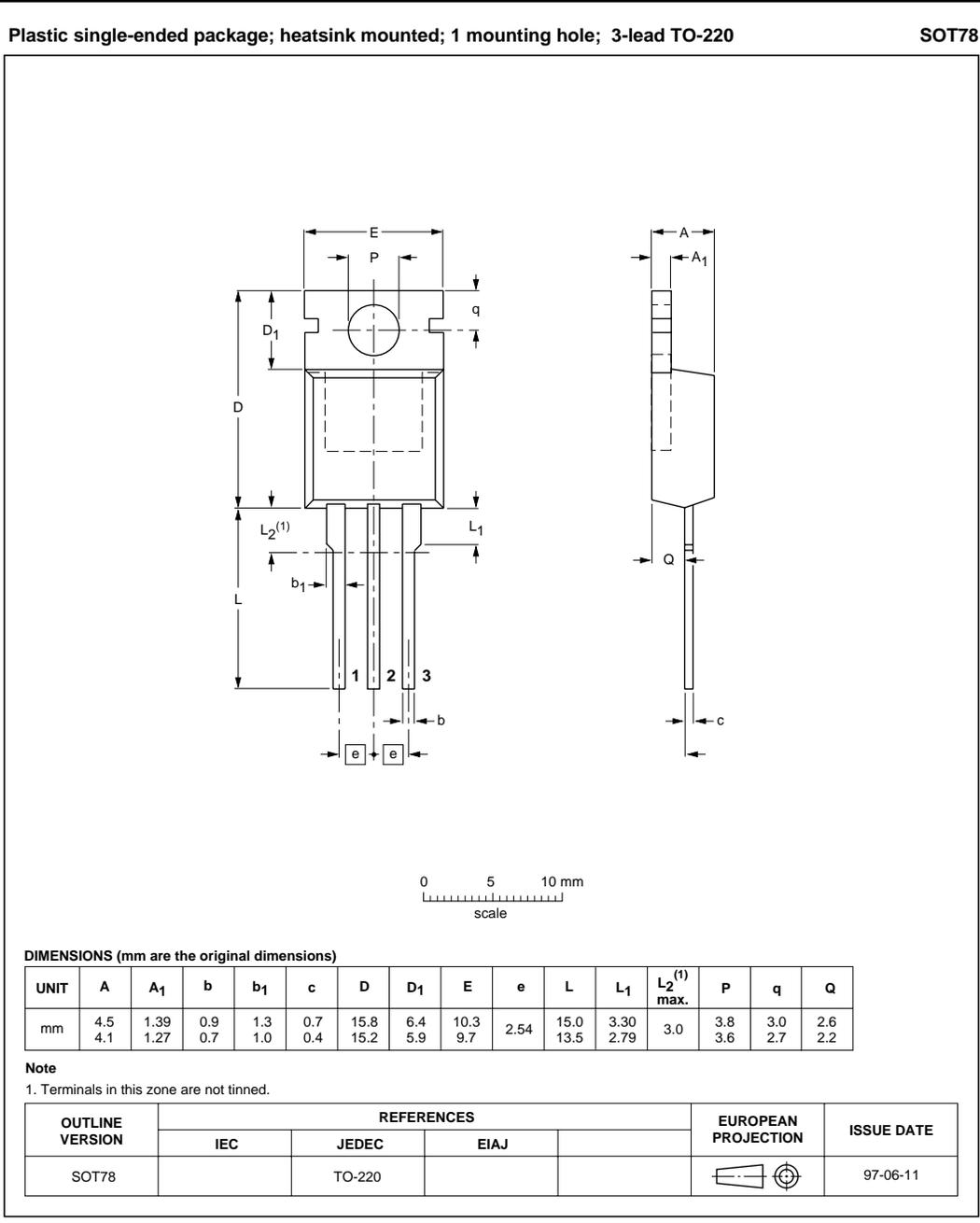


Fig. 16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".



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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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