

November 2002 Revised August 2003

FSA66

Low Voltage UHS Single SPST Normally Open Analog Switch

General Description

The FSA66 is a ultra high-speed (UHS) CMOS compatible single-pole/single-throw (SPST) analog switch. The LOW On Resistance of the switch allows input to be connected to output with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 1-bit switch with a switch enable (OE) signal. When OE is HIGH, the switch is on and Port A is connected to Port B. When OE is LOW, the switch is open and a high-impedance state exists between the two ports.

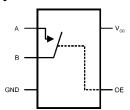
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- Broad V_{CC} Operating Range 1.65V–5.5V
- Rail-to-Rail signal handling
- \blacksquare 5 Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control input compatible with CMOS input levels
- >250 MHz -3dB bandwidth

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
FSA66M5X	MA05B	7Z66	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
FSA66P5X	MAA05A	Z66	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
FSA66L6X	MAC06	EE	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Analog Symbol



Pin Descriptions

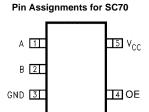
Pin Names	Description
OE	Switch Enable Input
A	Bus A I/O
В	Bus B I/O
NC	No Connect

Function Table

OE	B ₀	Function		
L	HIGH-Z State	Disconnect		
Н	A_0	Connect		

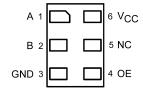
MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams



(Top View)

Pad Assignment for MicroPak



(Top Through View)

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions (Note 3)

Supply Voltage (V _{CC})	-0.5V to $+7.0V$
DC Switch Voltage (V _S)	$-0.5V$ to V_{CC} +0.5V
DC Input Voltage (V _{IN}) (Note 2)	-0.5V to $+7.0V$
DC Input Diode Current	
$(I_{IK}) V_{IN} < 0V$	−50 mA

 $\begin{array}{lll} (I_{\text{IK}}) \ V_{\text{IN}} < 0V & -50 \ \text{mA} \\ \text{DC Output } (I_{\text{OUT}}) \ \text{Sink Current} & 128 \ \text{mA} \\ \text{DC } V_{\text{CC}} / \text{GND Current } (I_{\text{CC}} / I_{\text{GND}}) & \pm 100 \ \text{mA} \\ \end{array}$

Storage Temperature Range $(T_{STG}) \hspace{1.5cm} -65^{\circ}C \hspace{1mm} to \hspace{1mm} +150^{\circ}C$

Junction Lead Temperature

under Bias (T_J) Junction Lead Temperature (T_L)

(Soldering, 10 Seconds)
Power Dissipation (P_D) @ +85°C

 SOT23-5
 200 mW

 SC70-5
 150 mW

Input Rise and Fall Time (t_r, t_f)

 $\label{eq:control} \begin{array}{lll} \mbox{Control Input; $V_{CC}=2.3$V-3.6V} & 0 \mbox{ ns/V to 10 ns} \\ \mbox{Control Input; $V_{CC}=4.5-5.5$V} & 0 \mbox{ ns/V to 5 ns} \\ \mbox{Switch I/O} & 0 \mbox{ ns/V to DC} \end{array}$

 $-40^{\circ}C$ to $+85^{\circ}C$

Operating Temperature (T_A) Thermal Resistance (θ_{JA})

+150°C

+260°C

 SOT23-5
 300°C/Watt

 SC70-5
 425°C/Watt

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

		V _{CC}	T _A =	–40°C to ⊦	-85°C	$T_A = +25^{\circ}C$				
Symbol	Parameter	(V)	Min	Typ (Note 5)	Max	Min	Тур	Max	Units	Conditions
V _{IH}	HIGH Level	1.65 to 1.95	0.75 V _{CC}						V	
	Input Voltage	2.3 to 5.5	0.7 V _{CC}							
V _{IL}	LOW Level	1.65 to 1.95			0.25 V _{CC}				V	
	Input Voltage	2.3 to 5.5			0.3 V _{CC}				· ·	
I _{IN}	Control Input Leakage Current	0 to 5.5		±0.05	±1.0				μА	$0 \le V_{IN} \le 5.5V$
I _{OFF}	OFF Leakage Current	1.65 to 5.5		±0.05	±10.0				μА	$0 \le A, B \le V_{CC}$
R _{ON}	Switch On Resistance			3	7					$V_{IN} = 0V, I_{IN} = 30 \text{ mA}$
	(Note 4)	4.5		5	12					$V_{IN} = 2.4V, I_{IN} = 15 \text{ mA}$
				7	15					$V_{IN} = 4.5V$, $I_{IN} = 30 \text{ mA}$
		3.0		4	9					$V_{IN} = 0V$, $I_{IN} = 24$ mA
		3.0		10	20				Ω	$V_{IN} = 3V$, $I_{IN} = 24$ mA
		2.3		5	12					$V_{IN} = 0V$, $I_{IN} = 8$ mA
		2.5		13	30					$V_{IN} = 2.3V$, $I_{IN} = 8 \text{ mA}$
		1.8		7	28					$V_{IN} = 0V$, $I_{IN} = 4$ mA
		1.0		25	60					$V_{IN} = 1.8V$, $I_{IN} = 4 \text{ mA}$
R _{flat}	On Resistance Flatness	5.0					6			$I_A = -30$ mA, $0 \le V_{Bn} \le V_{CC}$
	(Note 4)(Note 6)(Note 7)	3.3					12		Ω	$I_A = -24 \text{ mA}, \ 0 \le V_{Bn} \le V_{CC}$
		2.5					28		32	$I_A = -8 \text{ mA}, \ 0 \le V_{Bn} \le V_{CC}$
		1.8					125			$I_A = -4 \text{ mA}, \ 0 \le V_{Bn} \le V_{CC}$
I _{CC}	Quiescent Supply Current	1.65 to 5.5		0.05	10				μА	$V_{IN} = V_{CC}$ or GND
		1.00 10 0.0		0.00	.0			μΛ	$I_{OUT} = 0$	

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: All typical values are at the specified $V_{CC},$ and $T_A=25^{\circ}C.$

Note 6: Parameter is characterized but not tested in production.

Note 7: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

AC Electrical Characteristics

Symbol	Parameter	V	$T_{A} = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ V_{CC} $C_{L} = 50 \text{ pF, RU} = \text{RD} = 500\Omega$			Units	Conditions	Figure
Symbol	raianietei	(V)	Min Typ Max (Note 8)		Onits	Conditions	Number	
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus	1.65 to 1.95			4.3			
	(Note 9)	2.3-2.7			1.2	ns	V _{IN} = OPEN	Figures
		3.0-3.6			0.8	ns		1, 2
		4.5-5.5			0.3	ns		
t _{PZL} , t _{PZH}	Output Enable Time	1.65 to 1.95	1.5	7.0	14.2			
		2.3-2.7	1.5	3.3	7.0	ns	$V_{IN} = 2 \times V_{CC}$ for t_{PZL}	Figures 1, 2
		3.0-3.6	1.5	2.4	5.5	ns	$V_{IN} = 0V$ for t_{PZH}	
		4.5-5.5	1.5	2.0	4.5	ns		
t _{PLZ} , t _{PHZ}	Output Disable Time	1.65 to 1.95	1.5	9.2	18.2			Figures
		2.3-2.7	1.5	5.3	9.0	ns	V_{IN} = 2 x V_{CC} for t_{PLZ}	
		3.0-3.6	1.5	4.0	7.0	ns	$V_{IN} = 0V$ for t_{PHZ}	1, 2
		4.5-5.5	1.5	2.7	5.0	ns		
Q	Charge Injection (Note 10)	1.65-5.5		0.05		pC	$C_L = 0.1 \text{ nF}, V_{GEN} = 0V,$ $R_{GEN} = 0\Omega, f = 1 \text{ MHz}$	Figure 3
OIRR	Off Isolation (Note 11)	1.65-5.5		-50		dB	$R_L = 50 \Omega$, $C_L = 5 pF$, f = 10 MHz	Figure 4
BW	-3dB Bandwidth	1.65-5.5		>250		MHz	$R_L = 50 \Omega$	Figure 5
THD	Total Harmonic Distortion						$R_L = 600\Omega$	
	(Note 8)	5		.011		%	0.5 V _{P-P} f = 600 Hz to 20 KHz	

Note 8: All typical values are at the specified V_{CC} , and $T_A = 25^{\circ}C$.

Note 9: This parameter is guaranteed by design but is not tested. The switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

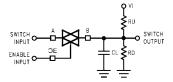
Note 10: Guaranteed by design.

Note 11: Off Isolation = $20 \log_{10} [V_A/V_{BN}]$.

Capacitance

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	2		pF	V _{CC} = 0V
C _{I/O}	Input/Output Capacitance	6		pF	V _{CC} = 5.0V

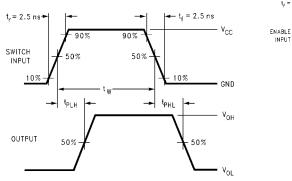
AC Loading and Waveforms



Input driven by 50Ω source terminated in 50Ω C_L includes load and stray capacitance.

Input PRR = 1.0 MHz; $t_{\rm W}$ = 500 ns

FIGURE 1. AC Test Circuit



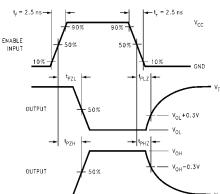
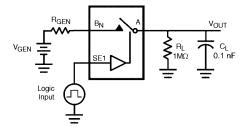


FIGURE 2. AC Waveforms



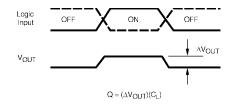
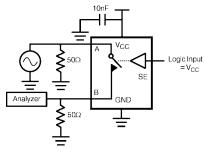
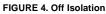


FIGURE 3. Charge Injection Test





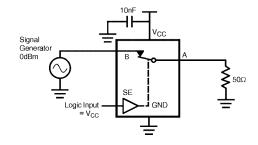


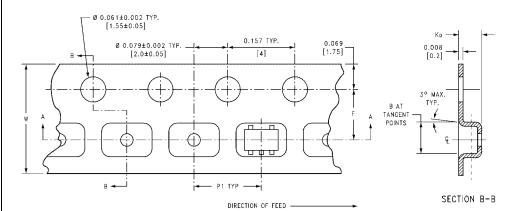
FIGURE 5. Bandwidth

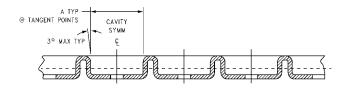
Tape and Reel Specification

TAPE FORMAT FOR SOT23, SC70

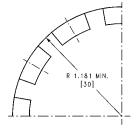
Package Tape		Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
M5X, P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)





SECTION A-A



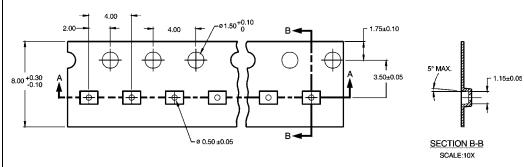
BEND RADIUS NOT TO SCALE

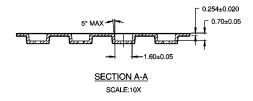
Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-5	8 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
	0 111111	(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)
SOT23-5	8 mm	0.130	0.130	0.138 ± 0.002	0.055 ± 0.004	0.157	0.315 ± 0.012
		(3.3)	(3.3)	(3.5 ± 0.05)	(1.4 ± 0.11)	(4)	(8 ± 0.3)

Tape and Reel Specification (Continued) TAPE FORMAT FOR MicroPak Package Tape Number

Package	Таре	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

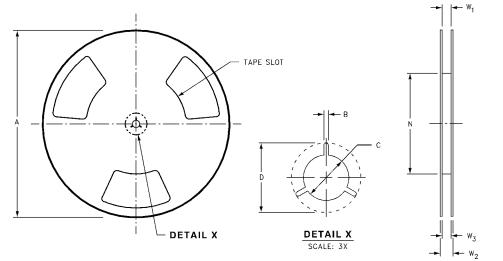
TAPE DIMENSIONS inches (millimeters)



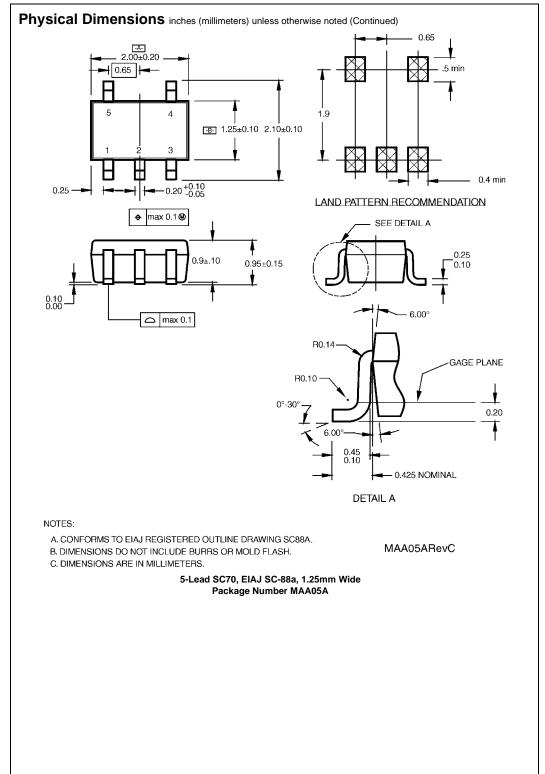


Tape and Reel Specification (Continued)

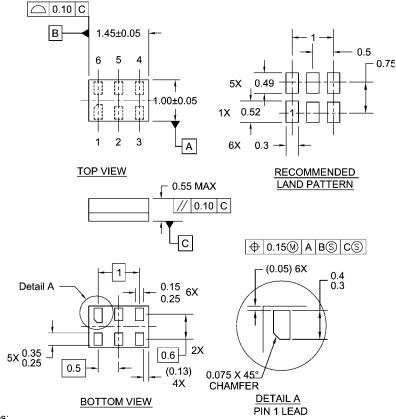
REEL DIMENSIONS inches (millimeters)



Tape Size	Α	В	C	D	N	W1	W2	W3
0	7.0	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
8 mm	(177.8)	(1.50)	(13.00)	(20.20)	(55.00)	(8.40 + 1.50/-0.00)	(14.40)	(W1 + 2.00/-1.00)



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com