



FAN6747WL

Highly Integrated Green-Mode PWM Controller

Features

- High-Voltage Startup
- AC-Line Brownout Protection by HV Pin
- Constant Output Power Limit by HV Pin (Full AC-Line Range)
- Built-in 8ms Soft-Start Function
- Two-Level Over-Current Protection (OCP) with 215 ms Debounce
- Short-Circuit Protection (SCP) with 15ms Debounce as Output Short
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- Low Startup Current: 30 μ A
- Low Operating Current: 1.7 mA
- Over-Temperature Protection (OTP) with External Negative-Temperature-Coefficient (NTC) Thermistor
- PWM Frequency Decreasing at Green-Mode
- V_{DD} Over-Voltage Protection (OVP)
- Internal Latch Circuit for OVP, OTP, SCP, and OCP

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- SMPS with Peak-Current Output, such as for Printers, Scanners, Motor Drivers
- AC/DC NB Adapters
- Open-Frame SMPS

Description

The highly integrated FAN6747WL PWM controller provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green-Mode function provides off-time modulation to decrease the switching frequency with load condition.

Under zero-load condition, the power supply enters Burst Mode and burst frequency can be low to reduce power. Green Mode enables the power supply to meet international power conservation requirements.

The FAN6747WL is specially designed for SMPS with peak-current output. It incorporates a cycle-by-cycle current limiting and two-level Over-Current-Protection (OCP) that can handle peak load with a debounce time. Once the current is over the threshold level, it triggers the first counter 15 ms and checks if V_{DD} is below 10 V; if it is, the PWM latches off for SCP. If V_{DD} is higher than 10 V; it keeps counting to 215 ms, then the PWM latches off for OCP.

FAN6747WL also integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation helps achieve stable peak-current control. To keep constant output power limit over universal AC input range, the current limit and OCP threshold voltage are adjusted according to AC line voltage detected by the HV pin. The gate output is clamped at 13.5 V to protect the external MOSFET from over-voltage damage.

Other protection functions include AC-line brownout protection with hysteresis and V_{DD} over-voltage protection. For over-temperature protection, an external NTC thermistor is applied to sense the ambient temperature. When OCP, OVP, SCP, or OTP is activated, an internal circuit latches off the controller. The latch is reset when V_{DD} drops to V_{DD-LH} .

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6747WLMY	-40 to +105°C	8-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .15-Inch Narrow Body	Tape & Reel

Application Diagram

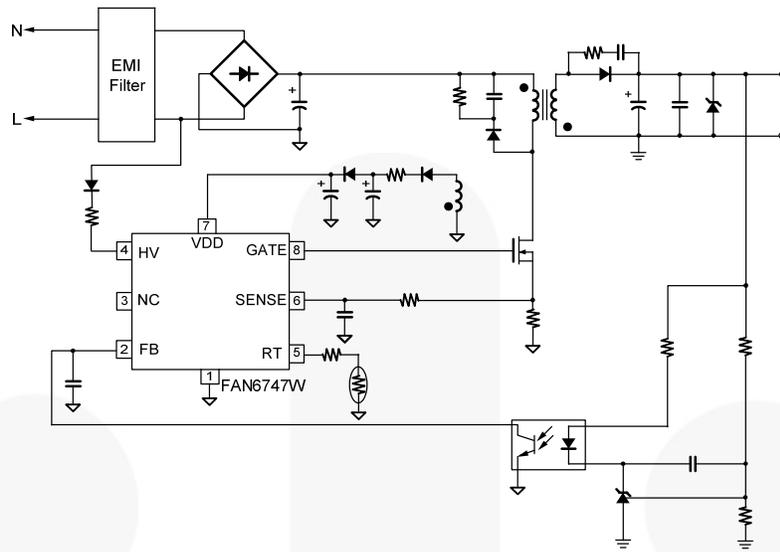


Figure 1. Typical Application

Internal Block Diagram

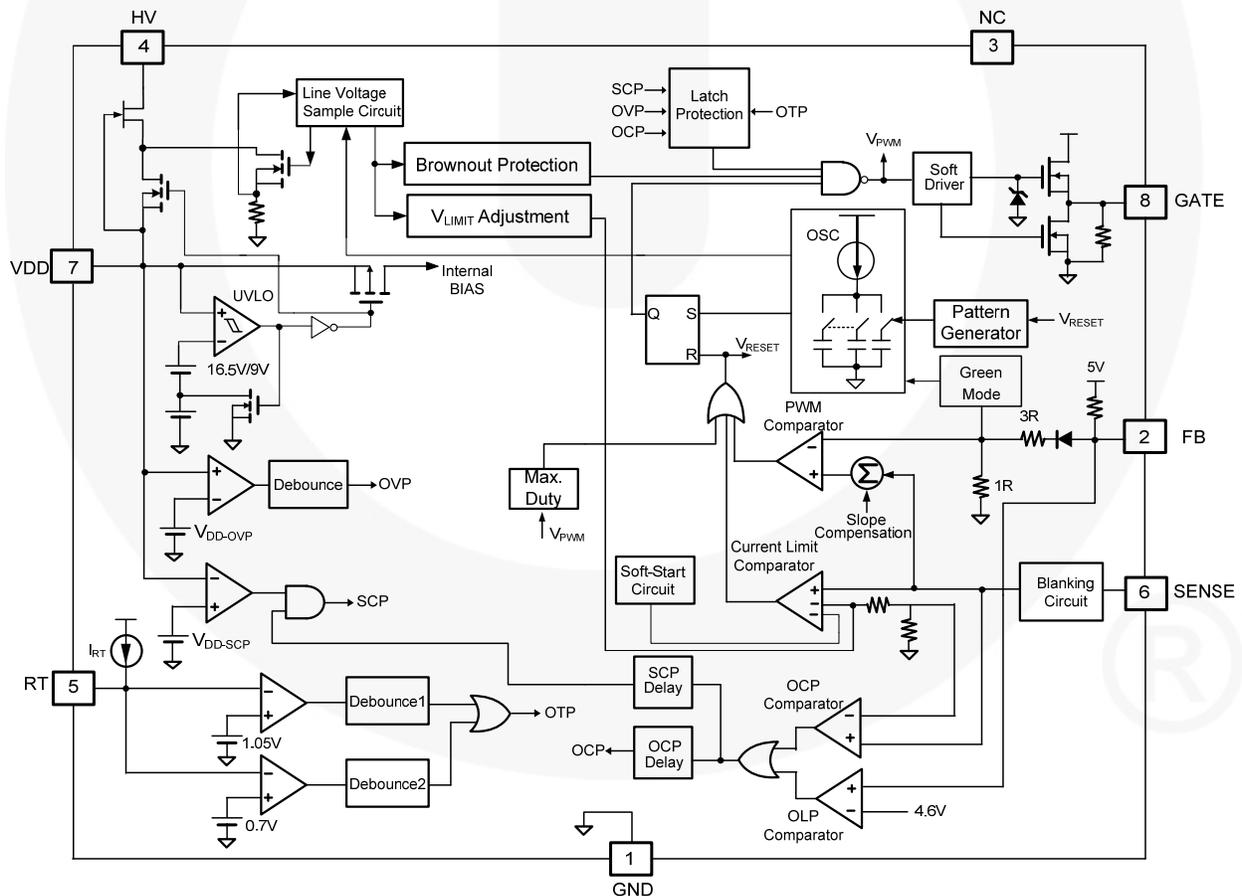
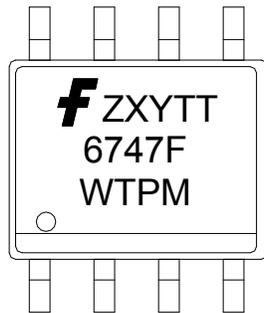


Figure 2. Functional Block Diagram

Marking Information



- F**: Fairchild Logo
- Z**: Plant Code
- X**: Year Code
- Y**: Week Code
- TT**: Die Run Code
- F**: L = OCP latch
- T**: Package Type (N = DIP, M = SOP)
- P**: Y = Green Compound
- M**: Manufacturing Flow Code

Figure 3. Top Mark

Pin Configuration

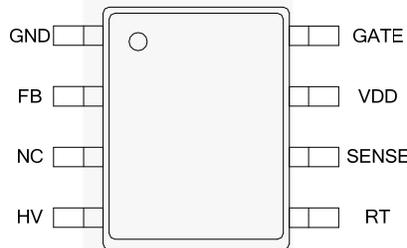


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	GND	Ground. This pin is used for the ground potential of all the pins. A 0.1 μ F decoupling capacitor placed between VDD and GND is recommended.
2	FB	Feedback. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined from this pin and the current-sense signal from Pin 6.
3	NC	No Connection
4	HV	High-Voltage Startup. This pin is connected to the line input via diodes and resistors to meet brownout and high/low line compensation. Once the voltage of the HV pin is lower than the brownout voltage, PWM output is turned off. High/low line compensation dominates the OCP level and cycle-by-cycle current limit to solve the unequal OCP level and power-limit problems under universal input.
5	RT	Over-Temperature Protection. For over-temperature protection, an external NTC thermistor is connected from this pin to GND. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. If the RT pin is not connected to the NTC resistor for over temperature protection, it is recommended to connect one 100 K Ω resistor to ground to prevent noise interference. This pin is limited by internal clamping circuit.
6	SENSE	Current Sense. This pin is used to sense the MOSFET current for the Current-Mode PWM and OCP. If the switching current is higher than the OCP threshold and lasts 215 ms, the controller latches off the PWM.
7	VDD	Supply Voltage. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external bulk capacitor of typically 10 μ F. The threshold voltages for startup and turn-off are 16.5 V and 9 V, respectively. The operating current is lower than 2 mA.
8	GATE	Gate Driver Output. The totem-pole output driver for the power MOSFET. It is internally clamped below 13.5 V.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	DC Supply Voltage		30	V
V _{HV}	Suddenly Input Voltage to HV Pin within 1 Second (Series connect with R _{HV})		640	V
V _L	Input Voltage to FB, SENSE, RT Pin	-0.3	7.0	V
P _D	Power Dissipation (T _A <50°C)		400	mW
θ _{JA}	Thermal Resistance (Junction-to-Ambient)		150	°C/W
T _J	Operating Junction Temperature	-40	+125	°C
T _{STG}	Storage Temperature Range	-55	+150	°C
T _L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin ⁽³⁾	Human Body Model, JESD22-A114	5	kV
		Charge Device Model, JESD22-C101	2	

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the network ground terminal.
3. ESD with the HV pin: CDM = 1250 V and HBM = 1000 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T _A	Operating Ambient Temperature	-40		+105	°C
V _{HV}	Input Voltage to HV Pin			500	V
R _{HV}	HV Startup Resistor	150	200	250	kΩ

Electrical Characteristics

$V_{DD} = 15\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				24	V
V_{DD-ON}	Turn-On Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	PWM Turn-Off Threshold Voltage		8	9	10	V
V_{DD-OLP}	Threshold Voltage on V_{DD} for HV JFET Turn-On in Protection Condition	After Trigger OCP/SCP/ OVP/ OTP	5.5	6.5	7.5	V
V_{DD-LH}	Threshold Voltage on VDD Pin for Latch-Off Release Voltage		3.5	4.0	4.5	V
V_{DD-AC}	Threshold Voltage on VDD Pin for Disable AC Recovery to Avoid Startup Failure		$V_{DD-OFF} + 2.5$	$V_{DD-OFF} + 3.0$	$V_{DD-OFF} + 3.5$	V
V_{DD-SCP}	Threshold Voltage on VDD Pin for Short-Circuit Protection (SCP)	$V_{FB} > V_{FBO}$	$V_{DD-OFF} + 0.5$	$V_{DD-OFF} + 1.0$	$V_{DD-OFF} + 1.5$	V
I_{LH}	Holding Current Under Latch-Off Condition	$V_{DD} = 5\text{ V}$	80	100	120	μA
I_{DD-ST}	Startup Current	$V_{DD-ON} - 0.16\text{ V}$			30	μA
I_{DD-OLP}	Holding Current at PWM-Off Phase	$V_{DD-OLP} + 0.1\text{ V}$	180	240	300	μA
I_{DD-OP1}	Operating Supply Current when PWM Operating	$V_{DD} = 20\text{ V}$, $V_{FB} = 3\text{ V}$, Gate Open		1.7	2.0	mA
I_{DD-OP2}	Operating Supply Current when PWM Stopped	$V_{DD} = 20\text{ V}$, $V_{FB} = 3\text{ V}$, Gate Open		1.2	1.5	mA
V_{DD-OVP}	Threshold Voltage on VDD Pin for V_{DD} Over-Voltage Protection (Latch-Off)		24	25	26	V
t_{D-OVP}	V_{DD} OVP Debounce Time	$V_{FB} > V_{FB-N}$	75	160	245	μs

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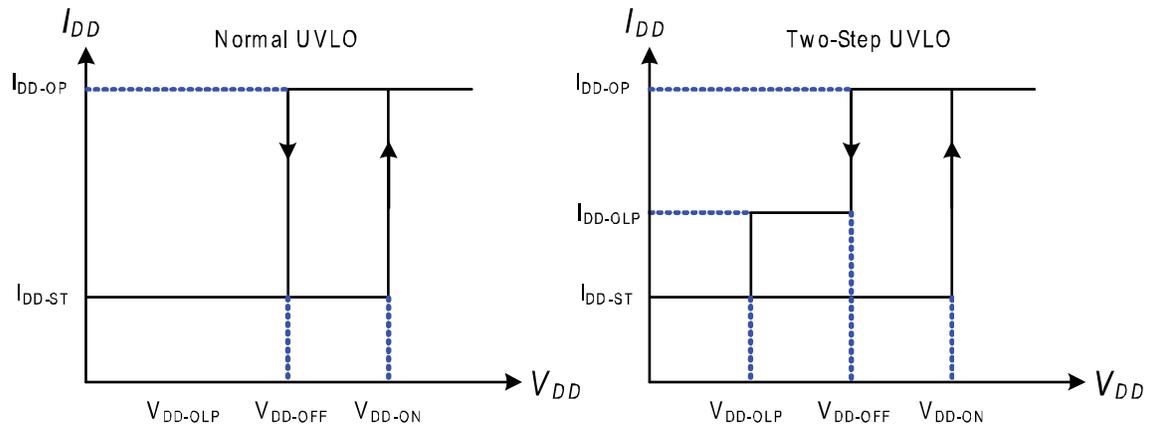


Figure 5. UVLO Specification

Electrical Characteristics (Continued)

$V_{DD} = 15\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	$V_{HV} = 120\text{ V}$, $V_{DD} = 0\text{ V}$	2.0	3.5	5.0	mA
V_{IN-OFF}	PWM Turn-Off Threshold	DC Source Series R = 200 k Ω to HV Pin	92	102	112	V
V_{IN-ON}	PWM Turn-On Threshold	DC Source Series R = 200 k Ω to HV Pin	104	114	124	V
ΔV_{IN}	Change in V_{IN} , $V_{IN-ON} - V_{IN-OFF}$	DC Source Series R = 200 k Ω to HV Pin	6	12	18	V
$t_{S-CYCLE}$	Line Voltage Sample cycle	$V_{FB} > V_{FB-N}$	170	205	240	μs
		$V_{FB} < V_{FB-G}$	450	615	780	
t_{S-TIME}	Line Voltage Sample Period			20		μs
$t_{D_VIN-OFF}$	PWM Turn-Off Debounce Time	$V_{FB} > V_{FB-N}$	65	75	85	ms
		$V_{FB} < V_{FB-G}$	180	235	290	ms

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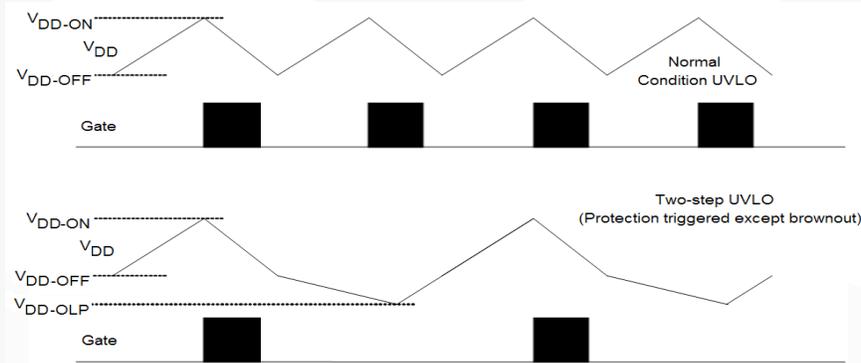


Figure 6. Normal UVLO and Two-Step UVLO Behavior

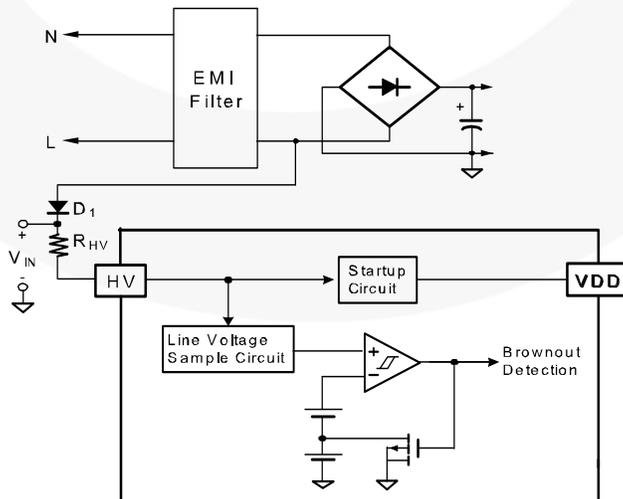


Figure 7. Brownout Circuit

Electrical Characteristics (Continued)

$V_{DD} = 15\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise specified.

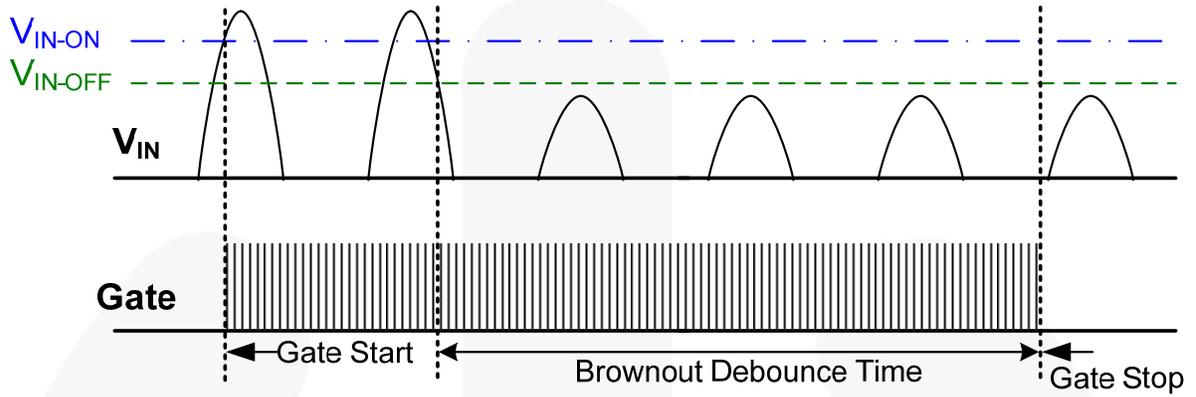


Figure 8. Brownout Behavior

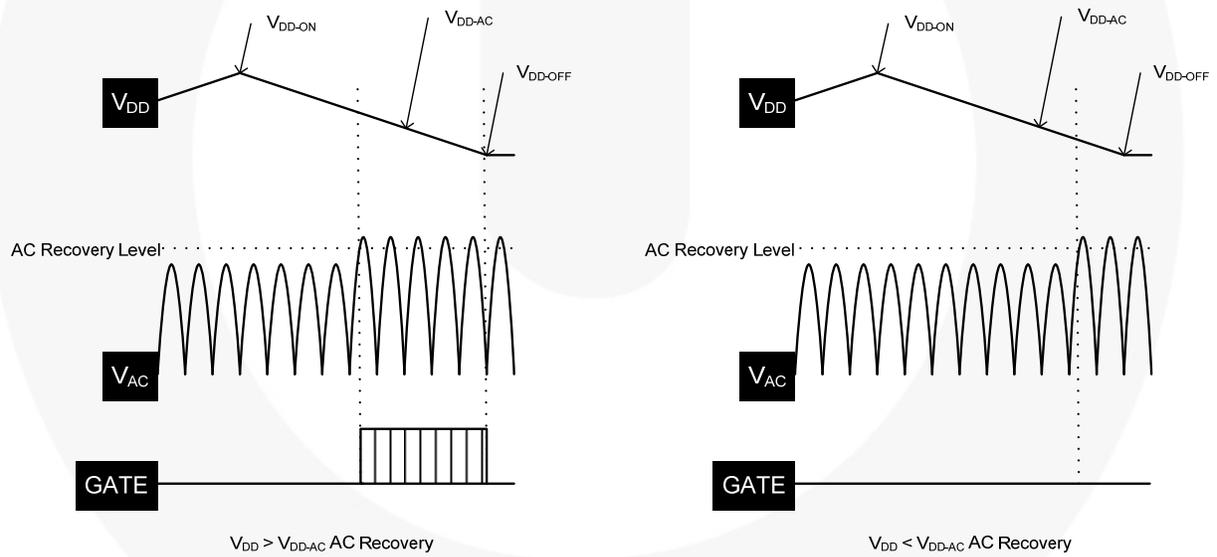


Figure 9. V_{DD-AC} and AC Recovery

Electrical Characteristics (Continued)

$V_{DD} = 15\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Oscillator Section						
f_{OSC}	Normal PWM Frequency	Center Frequency ($V_{FB} > V_{FB-N}$)	61	65	69	kHz
t_{JTR}	Hopping Period			4.8		ms
f_{OSC-G}	Green-Mode Minimum Frequency		20	23	26	kHz
V_{FB-N}	FB Threshold Voltage for Frequency Reduction Beginning	Pin, FB Voltage ($V_{FB} = V_{FB-N}$), $f_{OSC} - 5\text{ KHz}$	2.6	2.8	3.0	V
		Hopping Range	± 3.7	± 4.2	± 4.7	kHz
V_{FB-G}	FB Threshold Voltage for Turn-Off Hopping and Frequency Reduction Destination	Pin, FB Voltage ($V_{FB} = V_{FB-G}$)	2.1	2.3	2.5	V
		Hopping Range		± 1.45		kHz
V_{OZ-ON}	FB Threshold Voltage for Zero-Duty Recovery		1.6	1.8	2.0	V
V_{FB-ZDC} (V_{OZ-OFF})	FB Threshold Voltage for Zero Duty		1.5	1.7	1.9	V
$V_{OZ-ON} - V_{OZ-OFF}$	FB Voltage Hysteresis for V_{OZ-ON} to V_{OZ-OFF}		50	100	150	mV
f_{DV}	Frequency Variation vs. V_{DD} Deviation	$V_{DD} = 12\text{ V to } 22\text{ V}$			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	$T_A = -40\text{ to } 105^\circ\text{C}$			5	%

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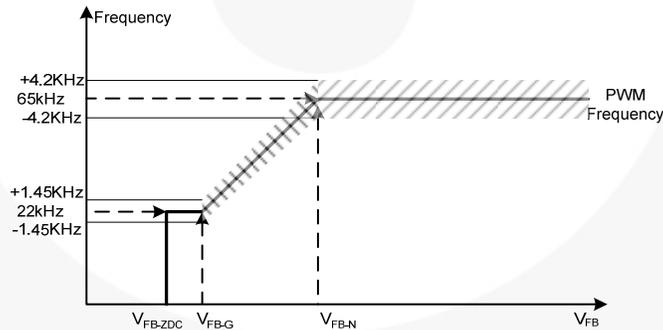


Figure 10. PWM Frequency

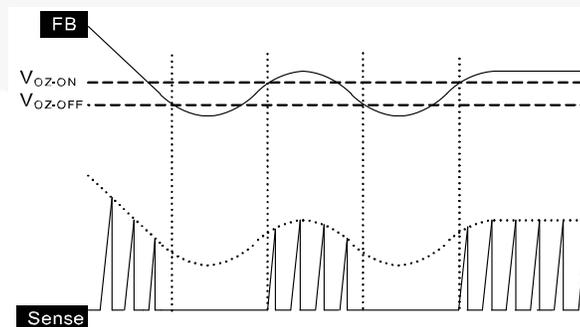


Figure 11. Burst-Mode Diagram

Electrical Characteristics (Continued)V_{DD} = 15 V and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Feedback Input Section						
A _V	Input-Voltage to Current-Sense Attenuation	V _{FB} < V _{FB-G}	1/4.5	1/4.0	1/3.5	V/V
Z _{FB}	Input Impedance		13.4	15.5	17.6	kΩ
V _{FBO}	FB Pin Open Voltage		4.8	5.0	5.2	V
V _{FB-OLP}	FB Open-Loop Protection Threshold Voltage		4.3	4.6	4.9	V
t _{D-OLP}	Open-Loop Protection Debounce Time	V _{FB} > V _{FB-OLP}	190	215	240	ms
Current Sense Section						
t _{PD}	Delay to Output			65	200	ns
t _{LEB}	Leading-Edge Blanking Time		230	270	310	ns
V _{limit-L}	Current Limit at Low Line (V _{AC-RMS} = 86 V)	V _{DC} = 122 V, Series R = 200 kΩ to HV	0.790	0.825	0.860	V
V _{limit-H}	Current Limit at High Line (V _{AC-RMS} = 259 V)	V _{DC} = 366 V, Series R = 200 kΩ to HV	0.690	0.725	0.760	V
V _{OCP-L}	OCP Trigger Level at Low Line (V _{AC-RMS} = 86 V)	V _{DC} = 122 V, Series R = 200 kΩ to HV	0.450	0.480	0.510	V
V _{OCP-H}	OCP Trigger Level at High Line (V _{AC} = 259 V)	V _{DC} = 366 V, Series R = 200 kΩ to HV	0.390	0.420	0.450	V
t _{SOFT-START}	Period During Startup	Startup Time	7	8	9	ms
t _{D-OCP}	Debounce Time for Output OCP	V _{CS} > V _{OCP}	190	215	240	ms
t _{D-SCP}	Debounce Time for Output SCP	V _{CS} > V _{OCP} and V _{DD} < V _{DD-SCP}	12	15	18	ms
PWM Output Section						
DCY _{MAX}	Maximum Duty Cycle		82.0	87.0	92.0	%
V _{OL}	Output Voltage Low	V _{DD} = 15 V, I _O = 50 mA			1.5	V
V _{OH}	Output Voltage High	V _{DD} = 12 V, I _O = 50 mA	8			V
t _R	Rising Time	GATE = 1 nF		95		ns
t _F	Falling Time	GATE = 1 nF		30		ns
V _{CLAMP}	Gate Output Clamping Voltage	V _{DD} = 22 V	11.0	13.5	16.0	V
Over-Temperature Protection Section						
I _{RT}	Output Current of RT Pin		92	100	108	μA
V _{OTP-LATCH-OFF}	Threshold Voltage for Over-Temperature Protection		1.00	1.05	1.10	V
t _{D_OTP-LATCH}	Over-Temperature Latch-Off Debounce Time	V _{FB} > V _{FB-N}	14	16	18	ms
		V _{FB} < V _{FB-G}	40	51	62	ms
V _{OTP2-LATCH-OFF}	Second Threshold Voltage for Over-Temperature Protection		0.65	0.70	0.75	V
t _{D_OTP2-LATCH}	Second Over-Temperature Latch-Off Debounce Time	V _{FB} > V _{FB-N}	110	185	260	μs
		V _{FB} < V _{FB-G}	320	605	890	

Typical Performance Characteristics

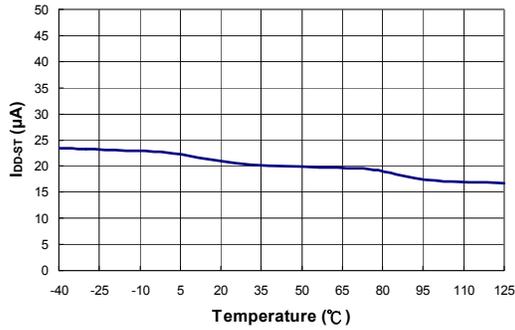


Figure 12. Startup Current (I_{DD-ST}) vs. Temperature

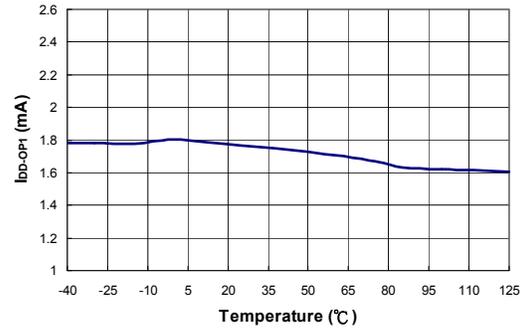


Figure 13. Operation Supply Current (I_{DD-OP1}) vs. Temperature

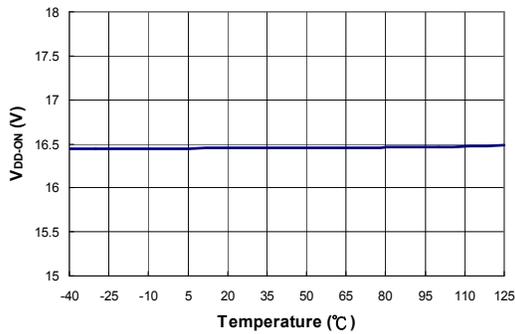


Figure 14. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

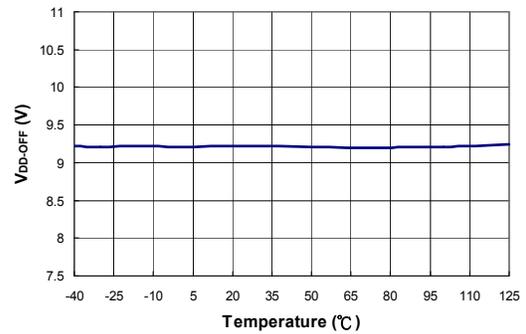


Figure 15. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

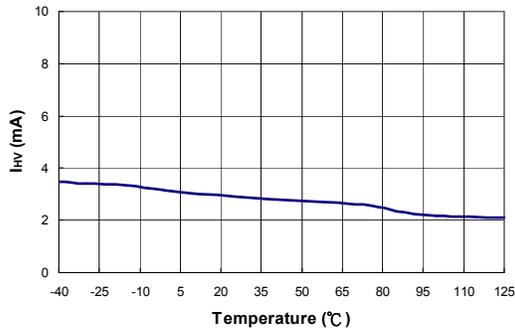


Figure 16. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

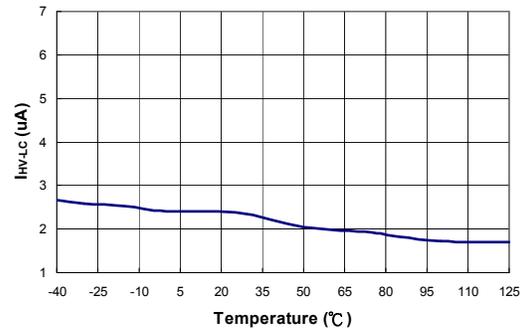


Figure 17. HV Pin Leakage Current After Startup (I_{HV-LC}) vs. Temperature

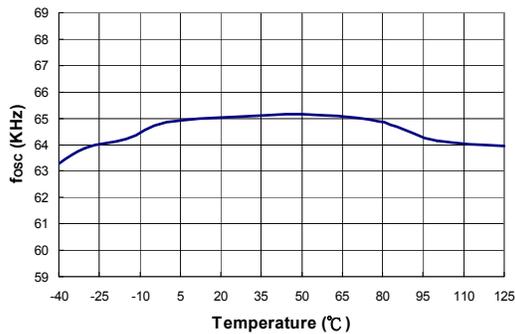


Figure 18. Frequency in Normal Mode (f_{osc}) vs. Temperature

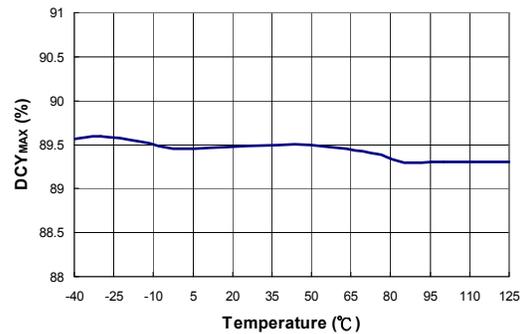


Figure 19. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics

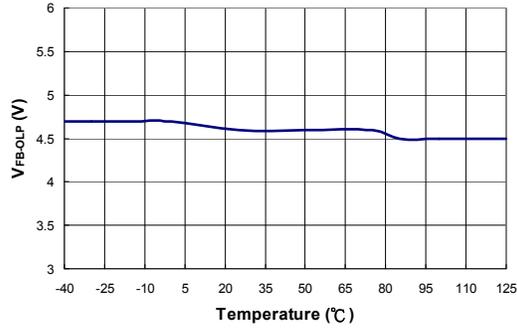


Figure 20. FB Open-Loop Trigger Level (V_{FB-OLP}) vs. Temperature

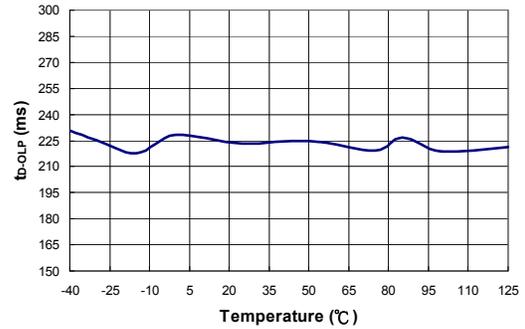


Figure 21. Debounce Time of FB Pin Open-Loop Protection (t_{D-OLP}) vs. Temperature

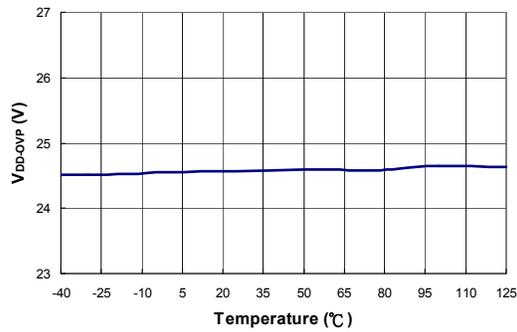


Figure 22. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

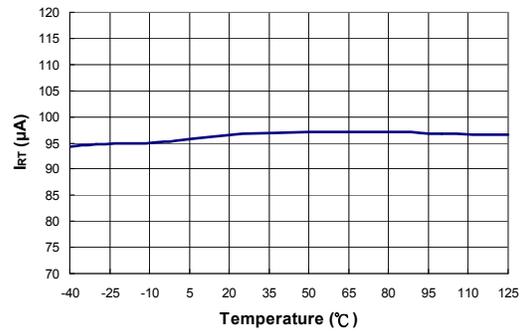


Figure 23. Output Current from RT Pin (I_{RT}) vs. Temperature

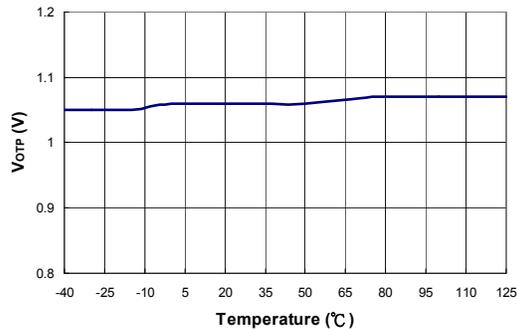


Figure 24. Over-Temperature Protection Threshold Voltage (V_{OTP}) vs. Temperature

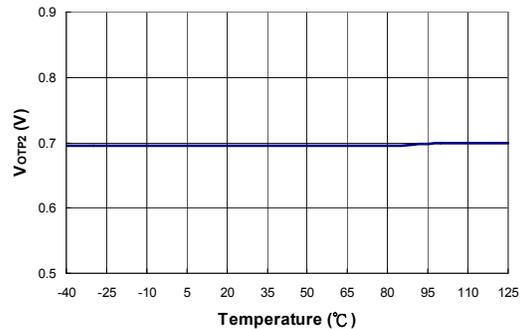


Figure 25. Over-Temperature Protection Threshold Voltage (V_{OTP2}) vs. Temperature

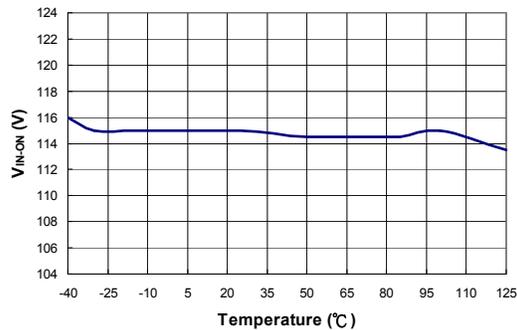


Figure 26. Brown-In (V_{IN-ON}) vs. Temperature

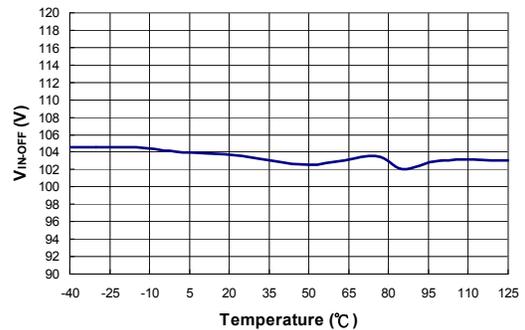


Figure 27. Brownout (V_{IN-OFF}) vs. Temperature

Operation Description

Startup Current

For startup, the HV pin is connected to the line input through an external diode and resistor, R_{HV} , (1N4007 / 200 K Ω recommended). Peak startup current drawn from the HV pin is $(V_{AC} \times \sqrt{2})/R_{HV}$ and charges the hold-up capacitor through the diode and resistor. When the V_{DD} capacitor level reaches V_{DD-ON} , the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6747WL to maintain the V_{DD} before the auxiliary winding of the main transformer provides the operating current.

Operating Current

Operating current is around 1.7 mA. The low current enables better efficiency, lower power consumption, and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary Green-Mode function provides off-time modulation to reduce the switching frequency in light-load and no-load conditions. V_{FB} , which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage, switching frequency is continuously decreased to the minimum Green-Mode frequency of around 23 KHz.

Two-Level Over-Current Protection (OCP)

The cycle-by-cycle current limiting shuts down the PWM immediately if the sense voltage is over the limited threshold voltage (0.825 V at low line). If the sense voltage is higher than the OCP threshold (0.48 V at low line), the internal counter counts for 215 ms, then latches off the PWM. When OCP occurs, PWM output is turned off and V_{DD} begins decreasing.

If V_{DD} goes below the turn-off threshold (~9 V), the controller is totally shut down. V_{DD} continues to discharge below V_{DD-OLP} by I_{DD-OLP} . Then V_{DD} is charged up to the turn-on threshold voltage of 16.5 V through the startup resistor. When V_{DD} is charged to 16.5 V, it cycles again. This phenomenon is called two-level UVLO.

Brownout and Constant Power Limited HV Pin

The HV pin can detect the peak value of the AC line voltage for brownout function and adjust the current-limit level for constant output power limit. Through two fast diodes and a startup resistor to sample the AC line voltage, the peak value is refreshed and stored in a register at each sampling cycle.

Equations 1 and 2 calculate the level of brown-in and brownout in RMS value:

$$V_{AC-ON} \text{ (RMS)} = 0.9V \times \frac{(R_{HV} + 1.6)}{1.6} \gamma \sqrt{2} \quad (1)$$

$$V_{AC-OFF} \text{ (RMS)} = 0.81V \times \frac{(R_{HV} + 1.6)}{1.6} \gamma \sqrt{2} \quad (2)$$

where R_{HV} is in k Ω .

The HV pin can perform current limit to shrink the tolerance of Over-Current Protection (OCP) under the full range of AC voltage to linearly current limit curve, as shown in Figure 28.

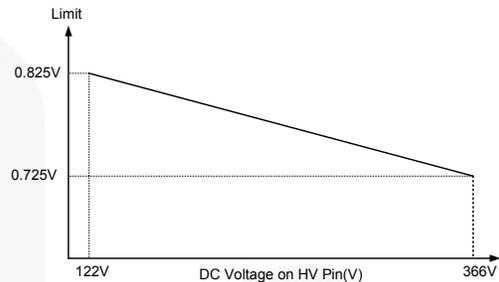


Figure 28. Linearly Current Limit Curve

Short-Circuit Protection (SCP)

This protection is used to handle the huge output demand if the power supply output is suddenly shorted to ground. If V_{DD} drops under 10 V and the sensed voltage is higher than the limited threshold voltage, SCP is triggered and PWM output is latched off. This latch condition is reset only if V_{DD} is discharged under 4 V.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5 V and 9 V, respectively. During startup, the hold-up capacitor must be charged to 16.5 V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} until the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 9 V during startup. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during startup.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 13.5 V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft-driving waveform is implemented to minimize EMI.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection is built in to prevent damage due to abnormal conditions. If the V_{DD} voltage is over the over-voltage protection voltage (V_{DD-OVP}) and lasts for t_{D-OVP} , the PWM pulses are disabled until the V_{DD} voltage drops below 4 V, then restarts. Over-voltage conditions are usually caused by open feedback loops.

Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 8ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

Built-In Slope Compensation

The sensed voltage across the current-sense resistor is used for Peak-Current-Mode control and pulse-by-pulse current limiting. Slope compensation improves stability and prevents sub-harmonic oscillation. FAN6747WL inserts a synchronized, positive-going, ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage across sense resistor R_S reaches the threshold voltage, the output GATE drive is turned off after a small delay, t_{PD} . This delay introduces an additional current proportional to $t_{PD} \cdot V_{IN} / L_P$. Since the delay is nearly constant regardless of the input voltage V_{IN} , higher input voltage results in a larger additional current and the output power limit is higher than under low input line voltage. To compensate this variation for a wide AC input range, a power-limiter is controlled by the HV pin to solve the unequal power-limit problem. The power limiter is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line input than at low-line input.

Over-Temperature Protection (OTP)

A NTC thermistor, R_{NTC} , in series with a resistor, R_A , is connected from the RT pin to GND pin. A constant current, I_{RT} , is output from this pin. The voltage of the RT pin can be expressed as $V_{RT} = I_{RT} \cdot (R_{NTC} + R_A)$, where I_{RT} is 100 μ A. The headroom of V_{RT} is limited at around 5 V by internal circuitry. As high ambient temperatures occur, R_{NTC} is smaller, such that the V_{RT} decreases. When V_{RT} is less than 1.05 V (V_{OTP}) but over 0.7 V, the PWM turns off after $t_{D_OTP_LATCH}$. The other threshold, V_{DD} under 0.7V, is used for fast shut down of FAN6747WL. If the RT pin is not connected to the NTC resistor for OTP, it is recommended to connect one 100 K Ω resistor to ground to prevent noise interference. This pin is limited by an internal clamping circuit.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in Continuous-Conduction Mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6747WL, and increasing the power MOS gate resistance improve performance.



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