Low Cost, Low Power, Differential ADC Driver

AD8137

FEATURES

Fully differential
Extremely low power with power-down feature
- **2.6 mA quiescent supply current @ 5 V**
- **450 μA in power-down mode @ 5 V**

High speed
- **110 MHz large signal 3 dB bandwidth @ G = 1**
- **450 V/μs slew rate**

12-bit SFDR performance @ 500 kHz
Fast settling time: 100 ns to 0.02%
Low input offset voltage: ±2.6 mV max
Low input offset current: 0.45 μA max
Differential input and output
Differential-to-differential or single-ended-to-differential operation
Rail-to-rail output
Adjustable output common-mode voltage
Externally adjustable gain
Wide supply voltage range: 2.7 V to 12 V
Available in small SOIC package

APPLICATIONS

ADC drivers
Portable instrumentation
Battery-powered applications
Single-ended-to-differential converters
Differential active filters
Video amplifiers
Level shifters

FUNCTIONAL BLOCK DIAGRAM

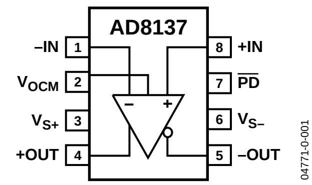


Figure 1.

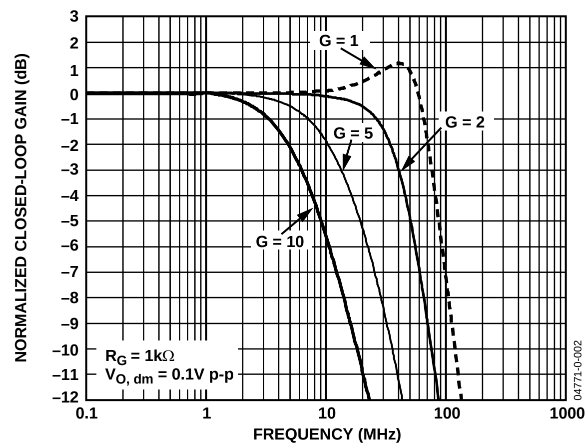


Figure 2. Small Signal Response for Various Gains

GENERAL DESCRIPTON

The AD8137 is a low cost differential driver with a rail-to-rail output that is ideal for driving ADCs in systems that are sensitive to power and cost. The AD8137 is easy to apply, and its internal common-mode feedback architecture allows its output common-mode voltage to be controlled by the voltage applied to one pin. The internal feedback loop also provides inherently balanced outputs as well as suppression of even-order harmonic distortion products. Fully differential and single-ended-to-differential gain configurations are easily realized by the AD8137. External feedback networks consisting of four resistors determine the closed-loop gain of the amplifier. The power-down feature is beneficial in critical low power applications.

The AD8137 is manufactured on Analog Devices, Inc., proprietary second-generation XFCB process, enabling it to achieve high levels of performance with very low power consumption.

The AD8137 is available in the small 8-lead SOIC package and 3 mm × 3 mm LFCSP package. It is rated to operate over the extended industrial temperature range of −40°C to +125°C.

Rev. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

12/09—Rev. B to Rev. C

Changes to Product Title, Applications Section, and General Description Section ... 1
Changes to Input Resistance Parameter Unit, Table 3 ... 5
Added EPAD Mnemonic/Description, Table 6 ... 7
Added Figure 61; Renumbered Sequentially ... 17
Moved Test Circuits Section ... 18
Changes to Power Down Section ... 24
Updated Outline Dimensions ... 26

7/05—Rev. A to Rev. B

Changes to Ordering Guide ... 24

8/04—Rev. 0 to Rev. A.

Added 8-Lead LFCSP ... Universal
Changes to Layout ... Universal
Changes to Product Title and Figure 1 ... 1
Changes to Specifications ... 3
Changes to Absolute Maximum Ratings ... 6
Changes to Figure 4 and Figure 5 ... 7
Added Figure 6, Figure 20, Figure 23, Figure 35, Figure 48, and Figure 58; Renumbered Sequentially ... 7
Changes to Figure 32 ... 12
Changes to Figure 40 ... 13
Changes to Figure 55 ... 16
Changes to Table 7 and Figure 63 ... 18
Changes to Equation 19 ... 19
Changes to Figure 64 and Figure 65 ... 20
Changes to Figure 66 ... 22
Added Driving an ADC with Greater Than 12-Bit Performance Section ... 22
Changes to Ordering Guide ... 24
Updated Outline Dimensions ... 24

5/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, V_{OCM} = 0 V (@ 25°C, differential gain = 1, $R_{L, dm}$ = R_F = R_G = 1 kΩ, unless otherwise noted, T_{MIN} to T_{MAX} = −40°C to +125°C).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
Dynamic Performance					
−3 dB Small Signal Bandwidth	$V_{O, dm}$ = 0.1 V p-p	64	76		MHz
−3 dB Large Signal Bandwidth	$V_{O, dm}$ = 2 V p-p	79	110		MHz
Slew Rate	$V_{O, dm}$ = 2 V step		450		V/µs
Settling Time to 0.02%	$V_{O, dm}$ = 3.5 V step		100		ns
Overdrive Recovery Time	G = 2, $V_{I, dm}$ = 12 V p-p triangle wave		85		ns
Noise/Harmonic Performance					
SFDR	$V_{O, dm}$ = 2 V p-p, f_C = 500 kHz		90		dB
	$V_{O, dm}$ = 2 V p-p, f_C = 2 MHz		76		dB
Input Voltage Noise	f = 50 kHz to 1 MHz		8.25		nV/√Hz
Input Current Noise	f = 50 kHz to 1 MHz		1		pA/√Hz
DC Performance					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} = 0 V	−2.6	±0.7	+2.6	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		3		µV/°C
Input Bias Current	T_{MIN} to T_{MAX}		0.5	1	µA
Input Offset Current			0.1	0.45	µA
Open-Loop Gain			91		dB
Input Characteristics					
Input Common-Mode Voltage Range		−4		+4	V
Input Resistance	Differential		800		KΩ
	Common-mode		400		KΩ
Input Capacitance	Common-mode		1.8		pF
CMRR	ΔV_{ICM} = ±1 V	66	79		dB
Output Characteristics					
Output Voltage Swing	Each single-ended output, $R_{L, dm}$ = 1 kΩ	V_{S-} + 0.55		V_{S+} − 0.55	V
Output Current			20		mA
Output Balance Error	f = 1 MHz		−64		dB
V_{OCM} to $V_{O, cm}$ PERFORMANCE					
V_{OCM} Dynamic Performance					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		58		MHz
Slew Rate	$V_{O, cm}$ = 0.5 V p-p		63		V/µs
Gain		0.992	1.000	1.008	V/V
V_{OCM} Input Characteristics					
Input Voltage Range		−4		+4	V
Input Resistance			35		kΩ
Input Offset Voltage		−28	±11	+28	mV
Input Voltage Noise	f = 100 kHz to 1 MHz		18		nV/√Hz
Input Bias Current			0.3	1.1	µA
CMRR	$\Delta V_{O, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±0.5 V	62	75		dB
Power Supply					
Operating Range		+2.7		±6	V
Quiescent Current			3.2	3.6	mA
Quiescent Current, Disabled	Power-down = low		750	900	µA
PSRR	ΔV_S = ±1 V	79	91		dB
$\overline{PD}$ Pin					
Threshold Voltage		V_{S-} + 0.7		V_{S-} + 1.7	V
Input Current	Power-down = high/low		150/210	170/240	µA
OPERATING TEMPERATURE RANGE		−40		+125	°C

V_S = 5 V, V_{OCM} = 2.5 V (@ 25°C, differential gain = 1, $R_{L,\,dm} = R_F = R_G$ = 1 kΩ, unless otherwise noted, T_{MIN} to T_{MAX} = −40°C to +125°C).

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
Dynamic Performance					
−3 dB Small Signal Bandwidth	$V_{O,\,dm}$ = 0.1 V p-p	63	75		MHz
−3 dB Large Signal Bandwidth	$V_{O,\,dm}$ = 2 V p-p	76	107		MHz
Slew Rate	$V_{O,\,dm}$ = 2 V step		375		V/μs
Settling Time to 0.02%	$V_{O,\,dm}$ = 3.5 V step		110		ns
Overdrive Recovery Time	G = 2, $V_{I,\,dm}$ = 7 V p-p triangle wave		90		ns
Noise/Harmonic Performance					
SFDR	$V_{O,\,dm}$ = 2 V p-p, f_C = 500 kHz		89		dB
	$V_{O,\,dm}$ = 2 V p-p, f_C = 2 MHz		73		dB
Input Voltage Noise	f = 50 kHz to 1 MHz		8.25		nV/√Hz
Input Current Noise	f = 50 kHz to 1 MHz		1		pA/√Hz
DC Performance					
Input Offset Voltage	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−2.7	±0.7	+2.7	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		3		μV/°C
Input Bias Current	T_{MIN} to T_{MAX}		0.5	0.9	μA
Input Offset Current			0.1	0.45	μA
Open-Loop Gain			89		dB
Input Characteristics					
Input Common-Mode Voltage Range		1		4	V
Input Resistance	Differential		800		kΩ
	Common-mode		400		kΩ
Input Capacitance	Common-mode		1.8		pF
CMRR	ΔV_{ICM} = ±1 V	64	90		dB
Output Characteristics					
Output Voltage Swing	Each single-ended output, $R_{L,\,dm}$ = 1 kΩ	V_{S-} + 0.45		V_{S+} − 0.45	V
Output Current			20		mA
Output Balance Error	f = 1 MHz		−64		dB
V_{OCM} to $V_{O,\,cm}$ PERFORMANCE					
V_{OCM} Dynamic Performance					
−3 dB Bandwidth	$V_{O,\,cm}$ = 0.1 V p-p		60		MHz
Slew Rate	$V_{O,\,cm}$ = 0.5 V p-p		61		V/μs
Gain		0.980	1.000	1.020	V/V
V_{OCM} Input Characteristics					
Input Voltage Range		1		4	V
Input Resistance			35		kΩ
Input Offset Voltage		−25	±7.5	+25	mV
Input Voltage Noise	f = 100 kHz to 5 MHz		18		nV/√Hz
Input Bias Current			0.25	0.9	μA
CMRR	$\Delta V_{O,\,dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±0.5 V	62	75		dB
Power Supply					
Operating Range		+2.7		±6	V
Quiescent Current			2.6	2.8	mA
Quiescent Current, Disabled	Power-down = low		450	600	μA
PSRR	ΔV_S = ±1 V	79	91		dB
$\overline{PD}$ Pin					
Threshold Voltage		V_{S-} + 0.7		V_{S-} + 1.5	V
Input Current	Power-down = high/low		50/110	60/120	μA
OPERATING TEMPERATURE RANGE		−40		+125	°C

V_S = 3 V, V_{OCM} = 1.5 V (@ 25°C, differential gain = 1, $R_{L, dm}$ = R_F = R_G = 1 kΩ, unless otherwise noted, T_{MIN} to T_{MAX} = −40°C to +125°C).

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
Dynamic Performance					
−3 dB Small Signal Bandwidth	$V_{O, dm}$ = 0.1 V p-p	61	73		MHz
−3 dB Large Signal Bandwidth	$V_{O, dm}$ = 2 V p-p	62	93		MHz
Slew Rate	$V_{O, dm}$ = 2 V step		340		V/µs
Settling Time to 0.02%	$V_{O, dm}$ = 3.5 V step		110		ns
Overdrive Recovery Time	G = 2, $V_{I, dm}$ = 5 V p-p triangle wave		100		ns
Noise/Harmonic Performance					
SFDR	$V_{O, dm}$ = 2 V p-p, f_C = 500 kHz		89		dB
	$V_{O, dm}$ = 2 V p-p, f_C = 2 MHz		71		dB
Input Voltage Noise	f = 50 kHz to 1 MHz		8.25		nV/√Hz
Input Current Noise	f = 50 kHz to 1 MHz		1		pA/√Hz
DC Performance					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} = 0 V	−2.75	±0.7	+2.75	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		3		µV/°C
Input Bias Current	T_{MIN} to T_{MAX}		0.5	0.9	µA
Input Offset Current			0.1	0.4	µA
Open-Loop Gain			87		dB
Input Characteristics					
Input Common-Mode Voltage Range		1		2	V
Input Resistance	Differential		800		kΩ
	Common-mode		400		kΩ
Input Capacitance	Common-mode		1.8		pF
CMRR	ΔV_{ICM} = ±1 V	64	80		dB
Output Characteristics					
Output Voltage Swing	Each single-ended output, $R_{L, dm}$ = 1 kΩ	V_{S-} + 0.37		V_{S+} − 0.37	V
Output Current			20		mA
Output Balance Error	f = 1 MHz		−64		dB
V_{OCM} to $V_{O, cm}$ PERFORMANCE					
V_{OCM} Dynamic Performance					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		61		MHz
Slew Rate	$V_{O, cm}$ = 0.5 V p-p		59		V/µs
Gain		0.96	1.00	1.04	V/V
V_{OCM} Input Characteristics					
Input Voltage Range		1.0		2.0	V
Input Resistance			35		kΩ
Input Offset Voltage		−25	±5.5	+25	mV
Input Voltage Noise	f = 100 kHz to 5 MHz		18		nV/√Hz
Input Bias Current			0.3	0.7	µA
CMRR	$\Delta V_{O, dm}$ /ΔV_{OCM}, ΔV_{OCM} = ±0.5 V	62	74		dB
Power Supply					
Operating Range		+2.7		±6	V
Quiescent Current			2.3	2.5	mA
Quiescent Current, Disabled	Power-down = low		345	460	µA
PSRR	ΔV_S = ±1 V	78	90		dB
$\overline{PD}$ Pin					
Threshold Voltage		V_{S-} + 0.7		V_{S-} + 1.5	V
Input Current	Power-down = high/low		8/65	10/70	µA
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12 V
V_{OCM}	V_{S+} to V_{S-}
Power Dissipation	See Figure 3
Input Common-Mode Voltage	V_{S+} to V_{S-}
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC/2-Layer	157	56	°C/W
8-Lead SOIC/4-Layer	125	56	°C/W
8-Lead LFCSP/4-Layer	70	56	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8137 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8137. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and the internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a 1 kΩ differential load on the output. RMS output voltages should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (125°C/W) and 8-lead LFCSP (θ_{JA} = 70°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

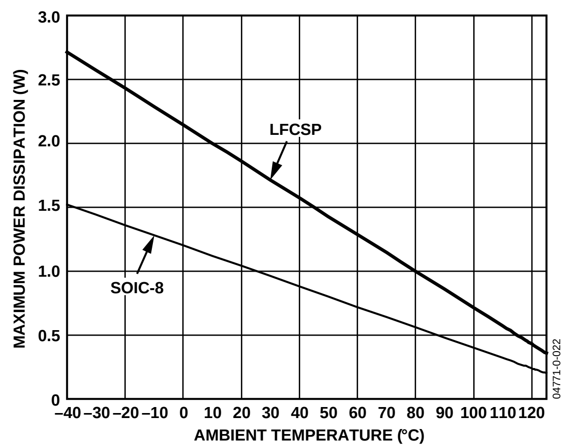
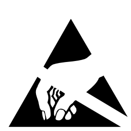


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

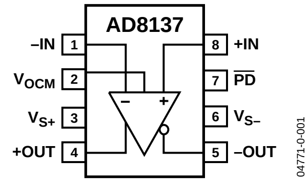


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Inverting Input.
2	V_{OCM}	An internal feedback loop drives the output common-mode voltage to be equal to the voltage applied to the V_{OCM} pin, provided the operation of the amplifier remains linear.
3	V_{S+}	Positive Power Supply Voltage.
4	+OUT	Positive Side of the Differential Output.
5	−OUT	Negative Side of the Differential Output.
6	V_{S-}	Negative Power Supply Voltage.
7	$\overline{PD}$	Power Down.
8	+IN	Noninverting Input.
	EPAD	Exposed paddle may be connected to either ground plane or power plane.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, differential gain = 1, $R_G = R_F = R_{L,\,dm} = 1\ k\Omega$, $V_S = 5\ V$, $T_A = 25°C$, $V_{OCM} = 2.5V$. Refer to the basic test circuit in Figure 60 for the definition of terms.

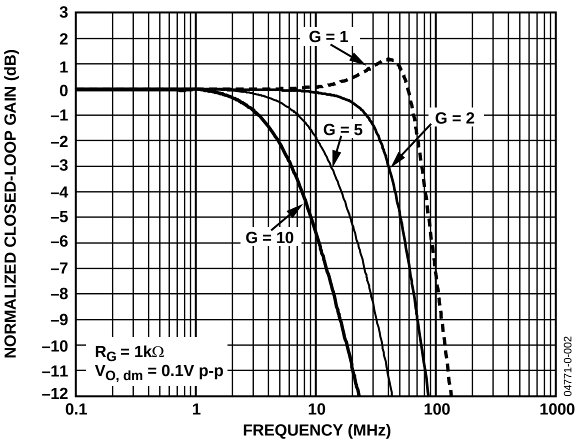


Figure 5. Small Signal Frequency Response for Various Gains

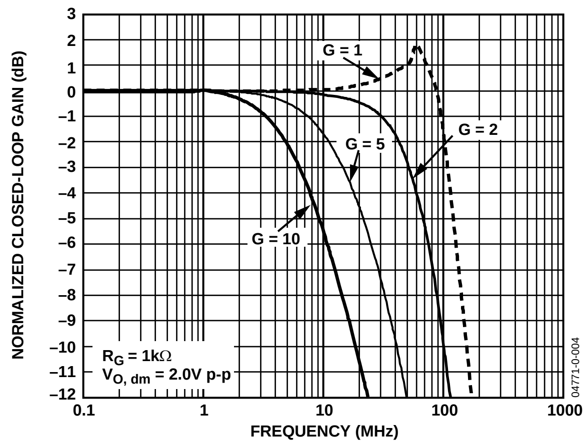


Figure 8. Large Signal Frequency Response for Various Gains

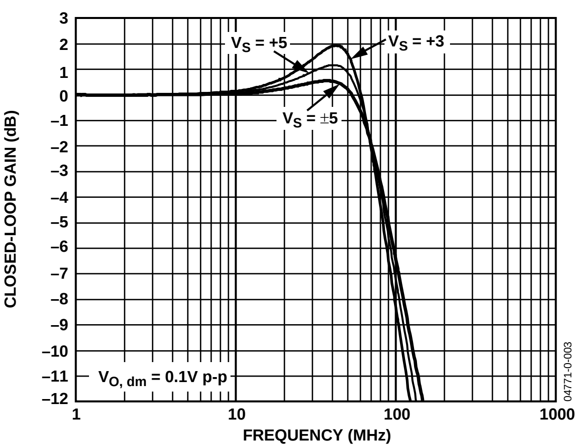


Figure 6. Small Signal Frequency Response for Various Power Supplies

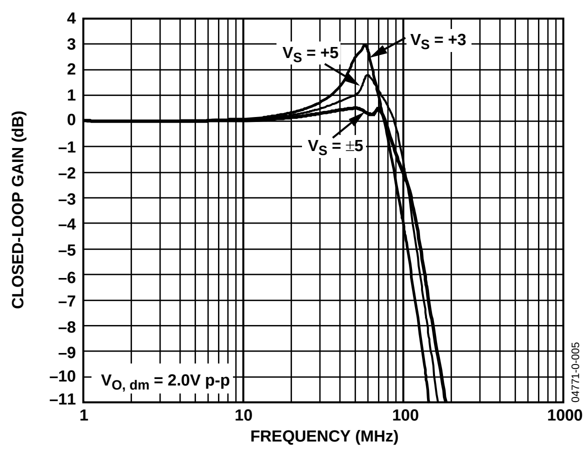


Figure 9. Large Signal Frequency Response for Various Power Supplies

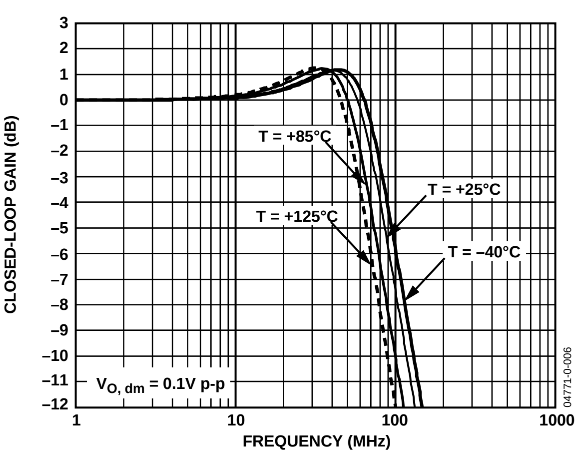


Figure 7. Small Signal Frequency Response at Various Temperatures

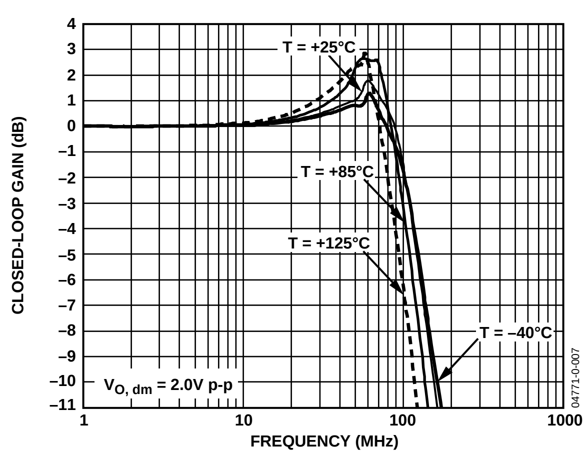


Figure 10. Large Signal Frequency Response at Various Temperatures

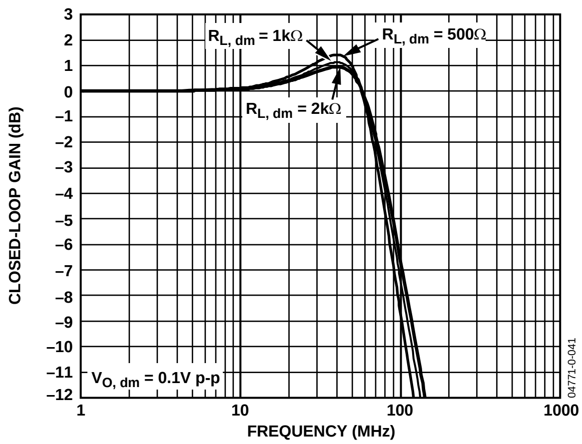


Figure 11. Small Signal Frequency Response for Various Loads

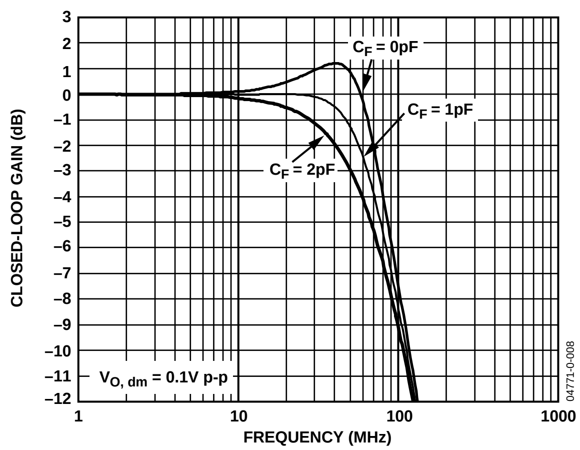


Figure 12. Small Signal Frequency Response for Various C_F

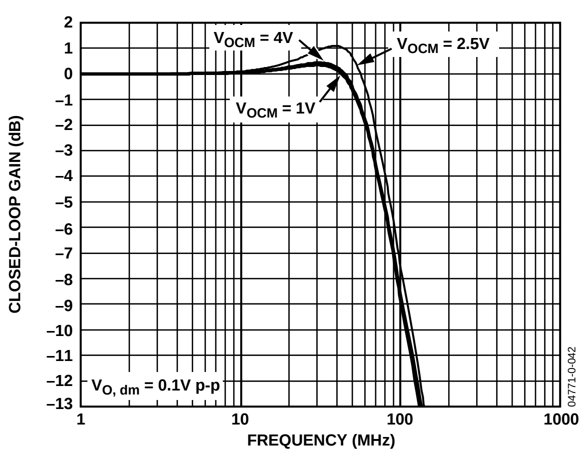


Figure 13. Small Signal Frequency Response at Various V_{OCM}

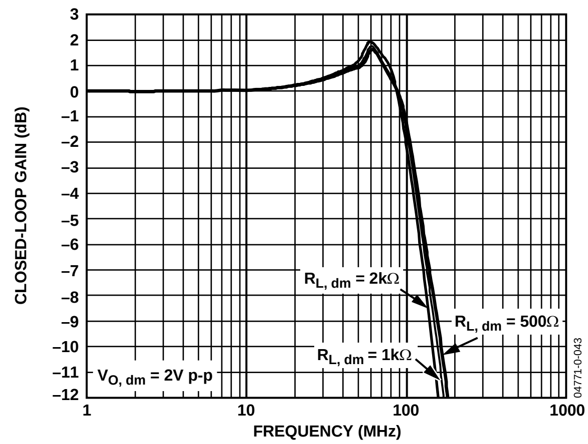


Figure 14. Large Signal Frequency Response for Various Loads

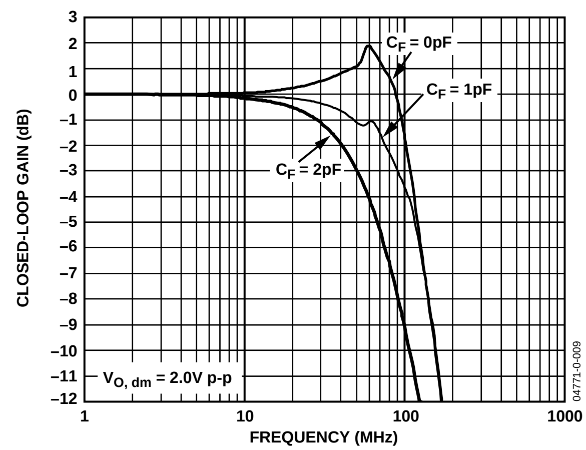


Figure 15. Large Signal Frequency Response for Various C_F

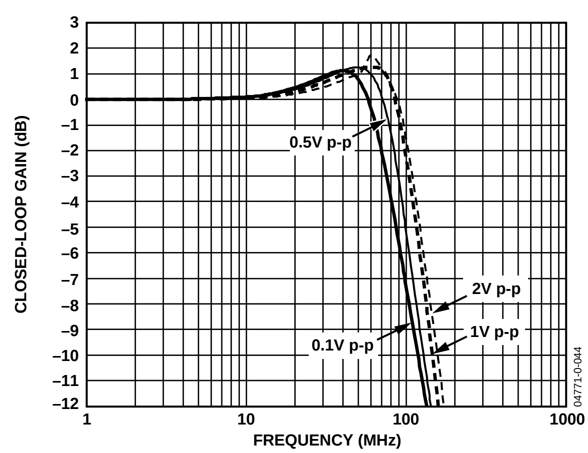


Figure 16. Frequency Response for Various Output Amplitudes

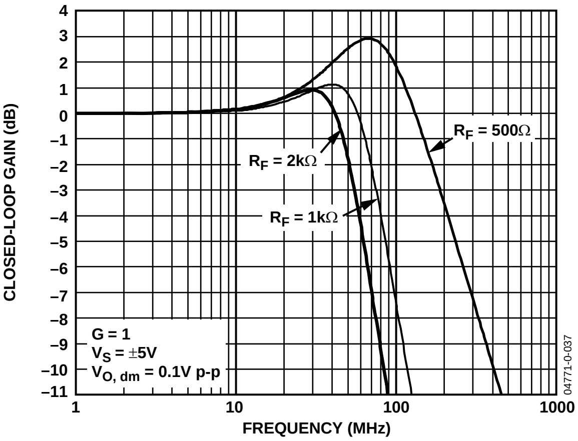


Figure 17. Small Signal Frequency Response for Various R_F

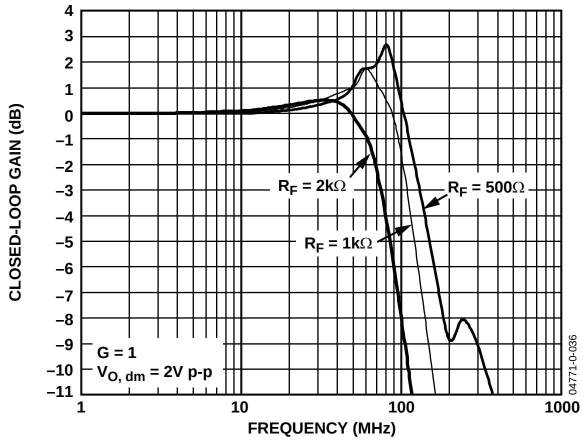


Figure 20. Large Signal Frequency Response for Various R_F

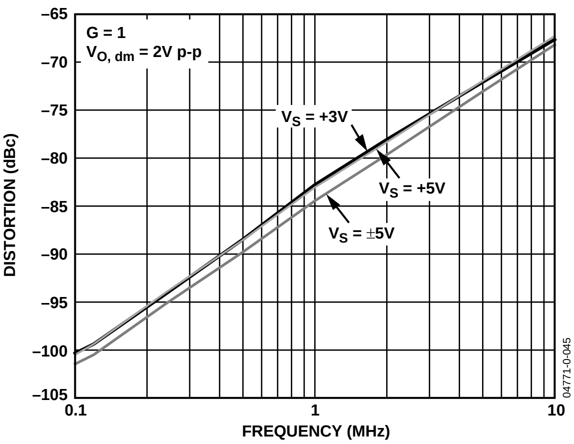


Figure 18. Second Harmonic Distortion vs. Frequency and Supply Voltage

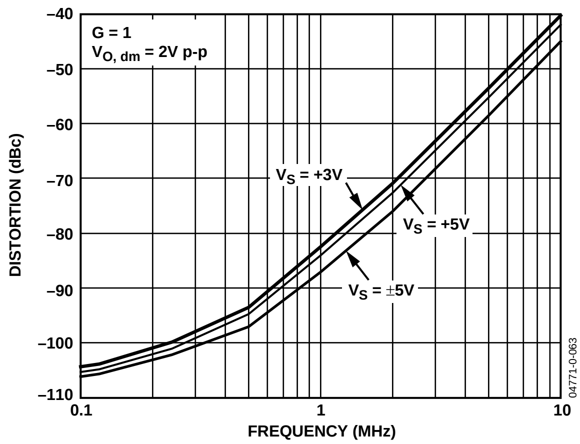


Figure 21. Third Harmonic Distortion vs. Frequency and Supply Voltage

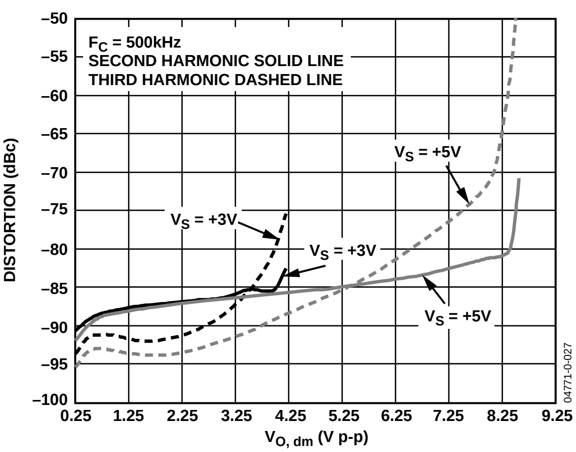


Figure 19. Harmonic Distortion vs. Output Amplitude and Supply, F_C = 500 kHz

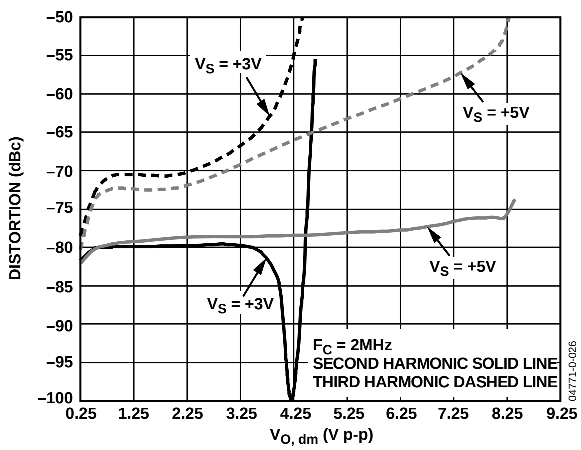


Figure 22. Harmonic Distortion vs. Output Amplitude and Supply, F_C = 2 MHz

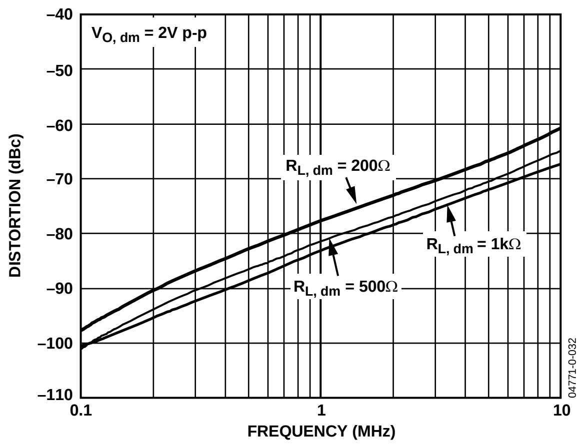


Figure 23. Second Harmonic Distortion at Various Loads

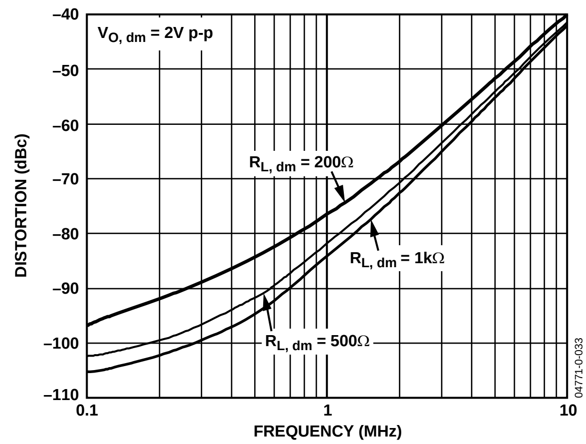


Figure 26. Third Harmonic Distortion at Various Loads

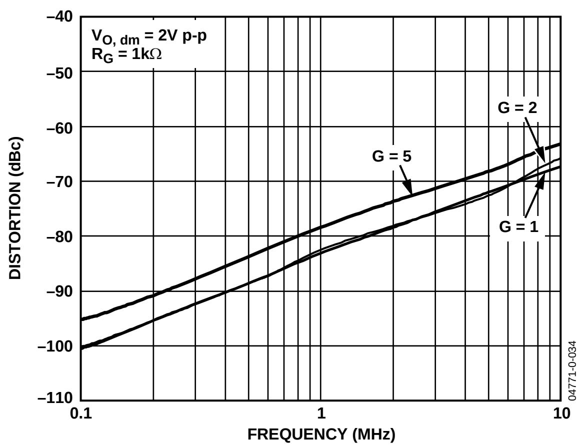


Figure 24. Second Harmonic Distortion at Various Gains

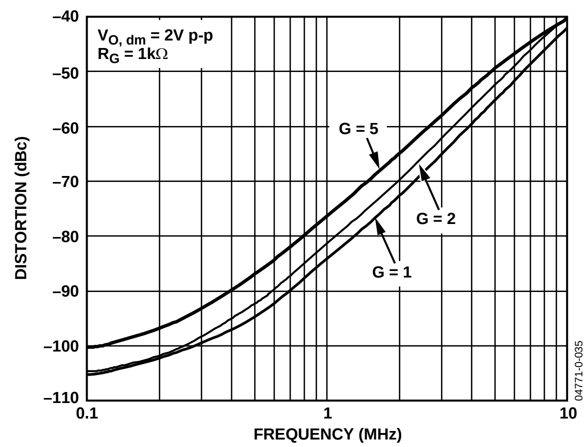


Figure 27. Third Harmonic Distortion at Various Gains

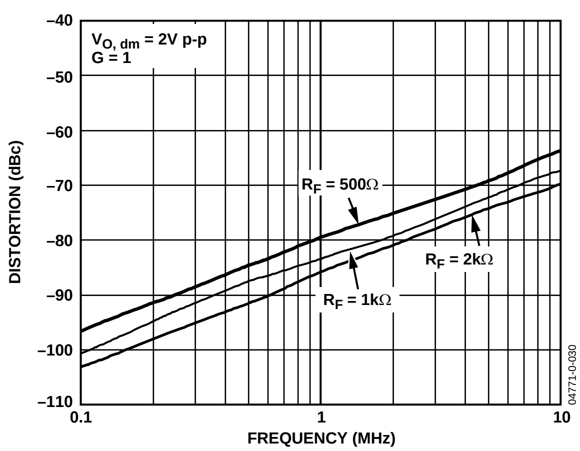


Figure 25. Second Harmonic Distortion at Various R_F

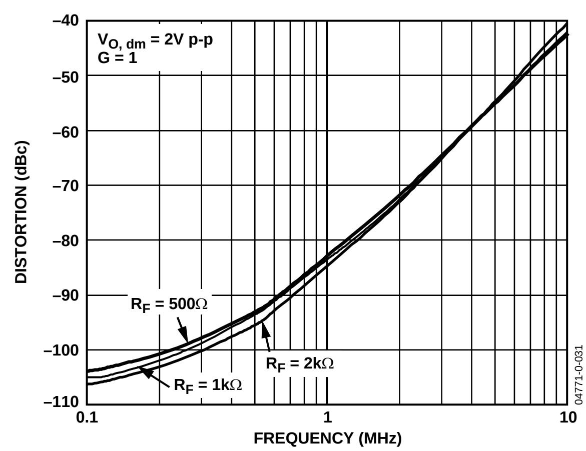


Figure 28. Third Harmonic Distortion at Various R_F

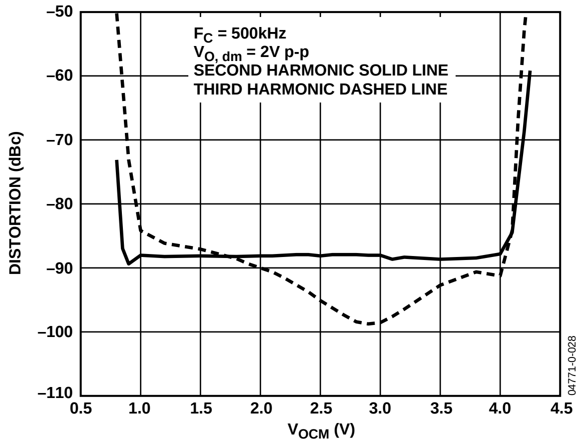


Figure 29. Harmonic Distortion vs. V_{OCM}, $V_S = 5$ V

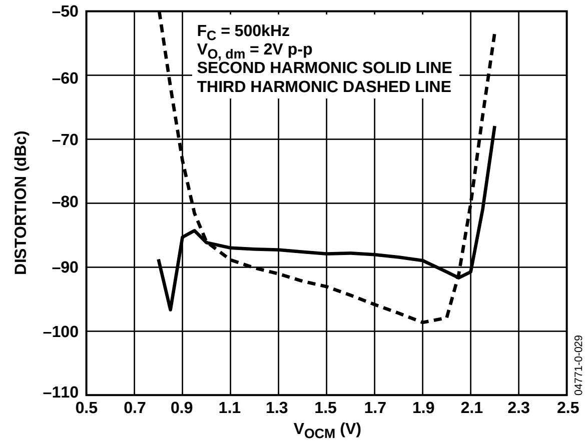


Figure 32. Harmonic Distortion vs. V_{OCM}, $V_S = 3$ V

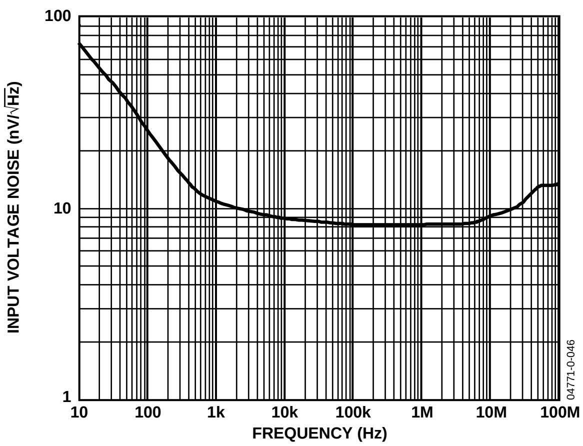


Figure 30. Input Voltage Noise vs. Frequency

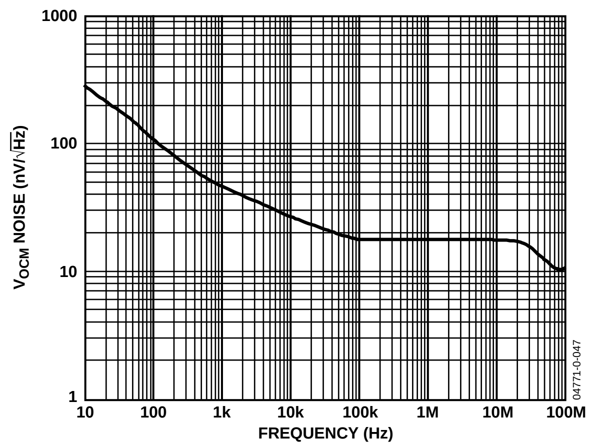


Figure 33. V_{OCM} Voltage Noise vs. Frequency

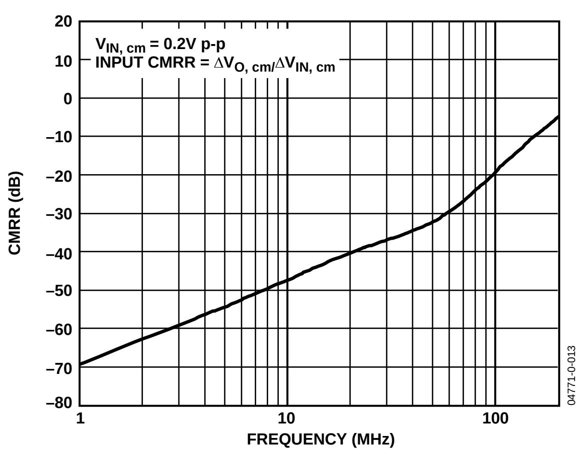


Figure 31. CMRR vs. Frequency

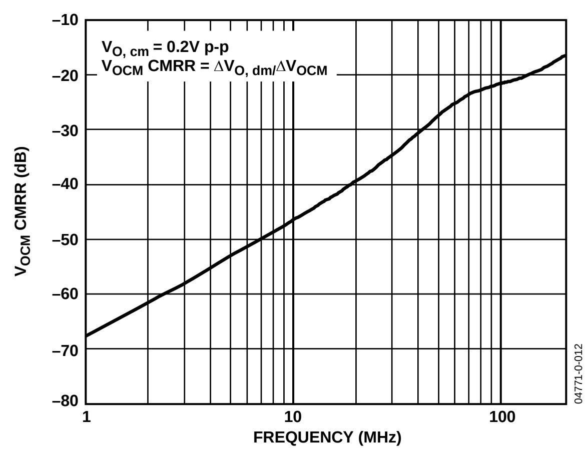


Figure 34. V_{OCM} CMRR vs. Frequency

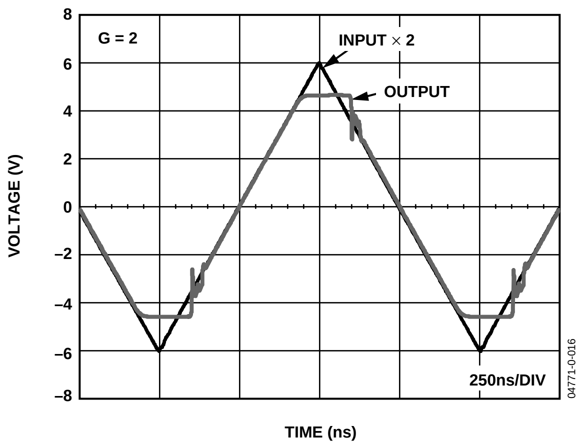


Figure 35. Overdrive Recovery

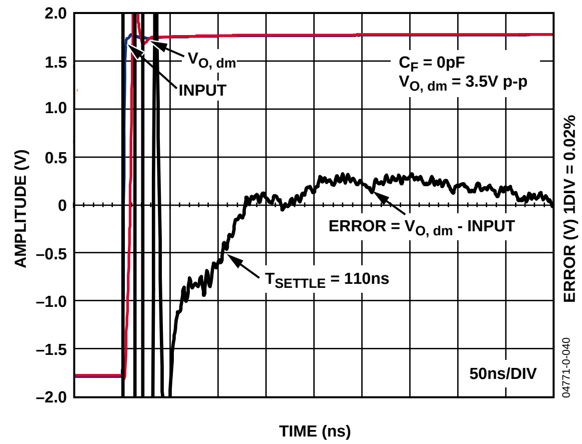


Figure 38. Settling Time (0.02%)

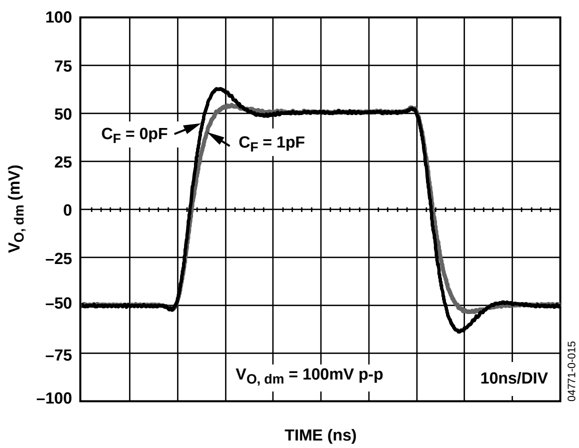


Figure 36. Small Signal Transient Response for Various Feedback Capacitances

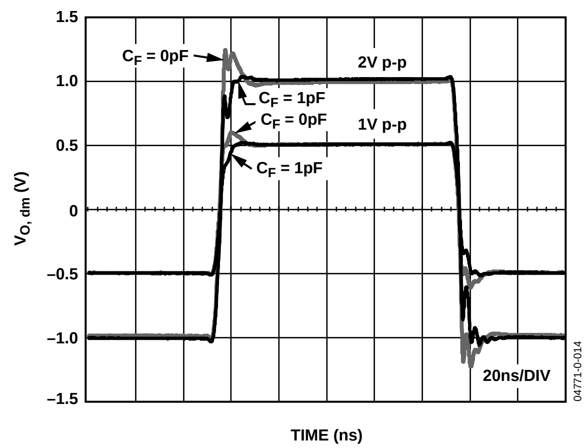


Figure 39. Large Signal Transient Response for Various Feedback Capacitances

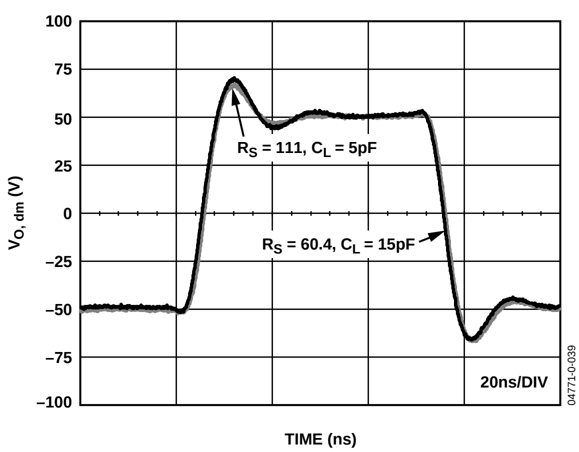


Figure 37. Small Signal Transient Response for Various Capacitive Loads

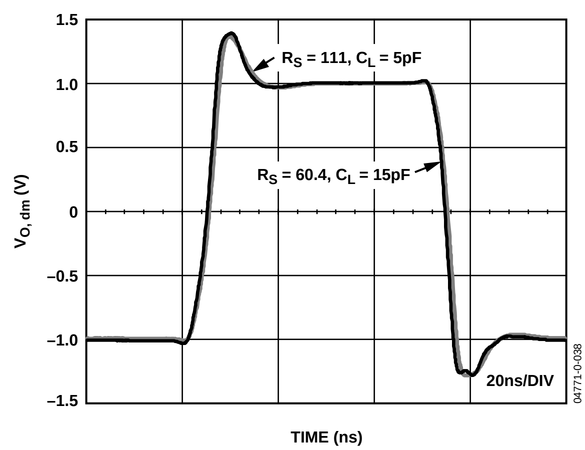


Figure 40. Large Signal Transient Response for Various Capacitive Loads

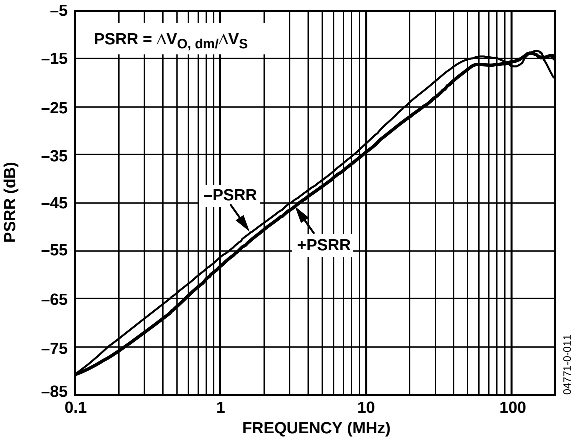


Figure 41. PSRR vs. Frequency

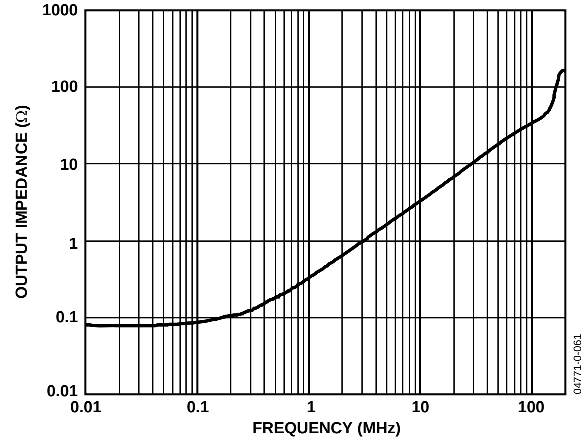


Figure 44. Single-Ended Output Impedance vs. Frequency

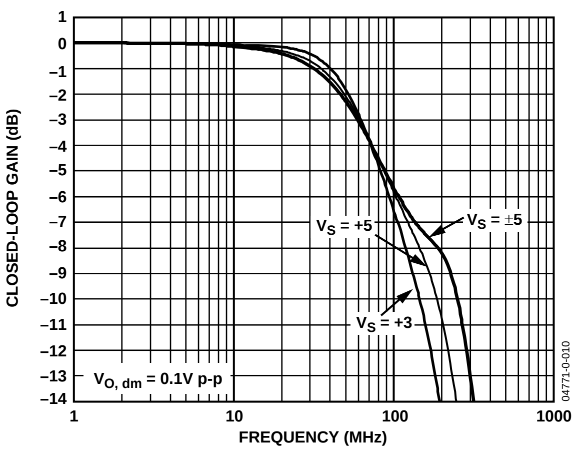


Figure 42. V_{OCM} Small Signal Frequency Response for Various Supply Voltages

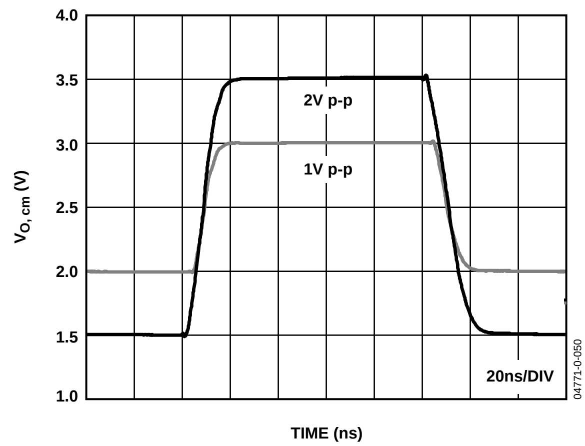


Figure 45. V_{OCM} Large Signal Transient Response

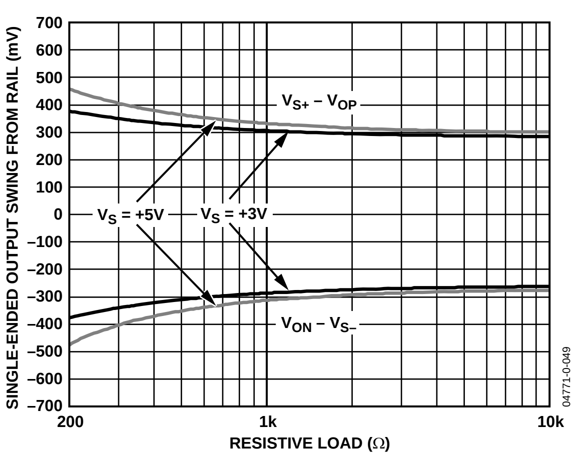


Figure 43. Output Saturation Voltage vs. Output Load

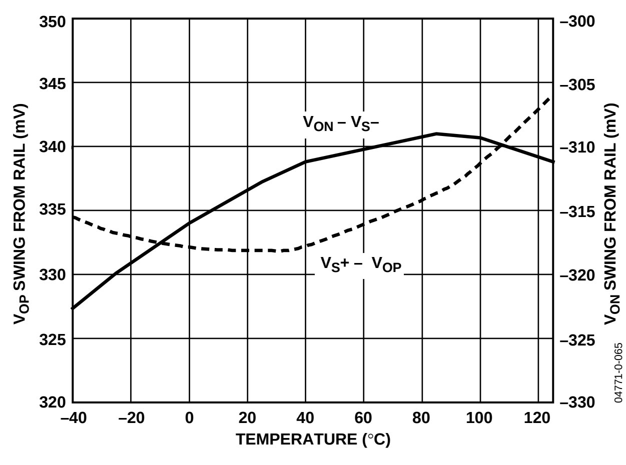


Figure 46. Output Saturation Voltage vs. Temperature

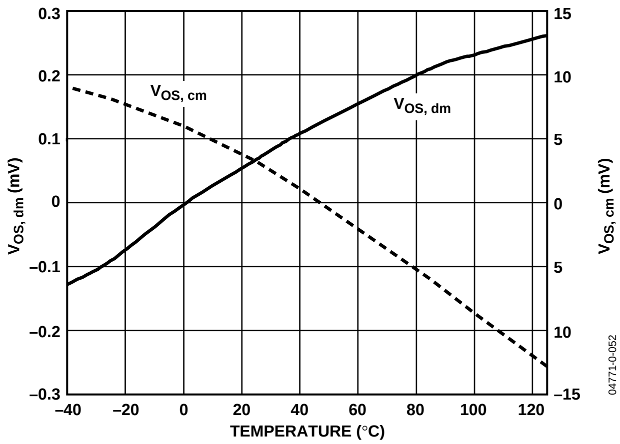


Figure 47. Offset Voltage vs. Temperature

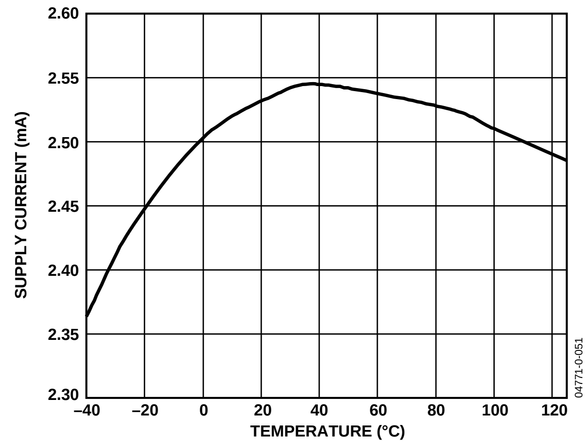


Figure 50. Supply Current vs. Temperature

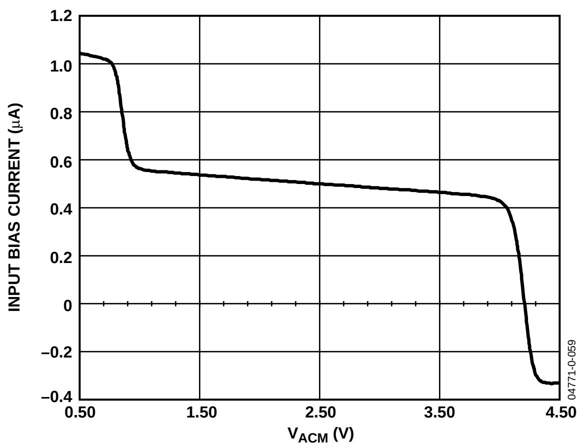


Figure 48. Input Bias Current vs. Input Common-Mode Voltage, V_{ACM}

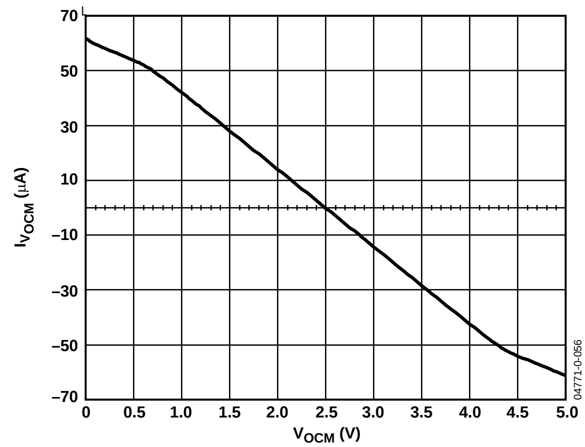


Figure 51. V_{OCM} Bias Current vs. V_{OCM} Input Voltage

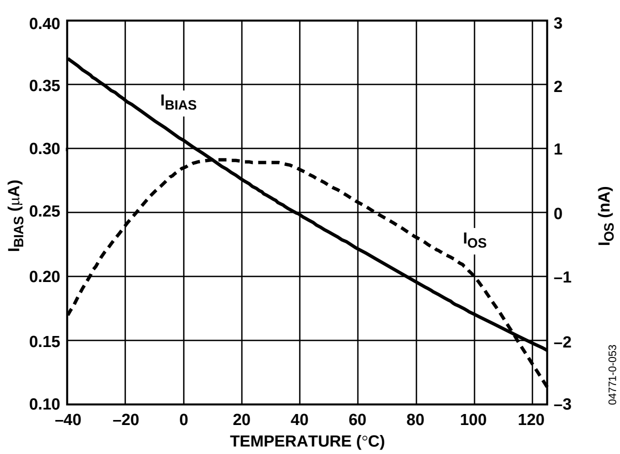


Figure 49. Input Bias and Offset Current vs. Temperature

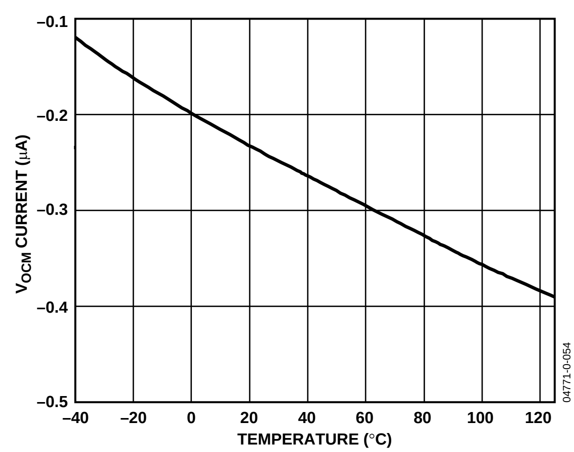


Figure 52. V_{OCM} Bias Current vs. Temperature

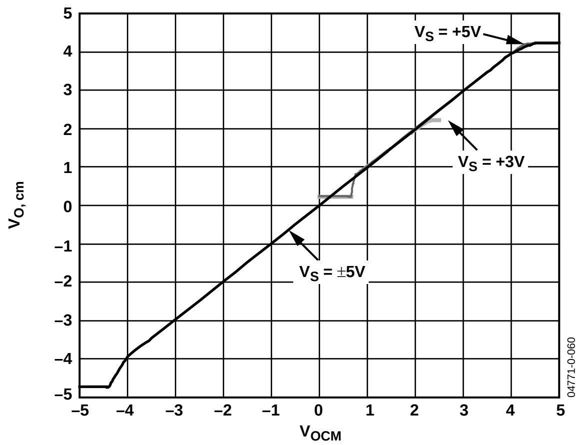


Figure 53. $V_{O,cm}$ vs. V_{OCM} Input Voltage

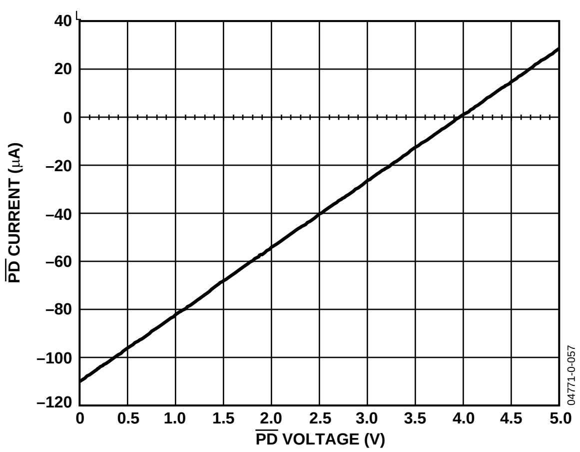


Figure 54. $\overline{PD}$ Current vs. $\overline{PD}$ Voltage

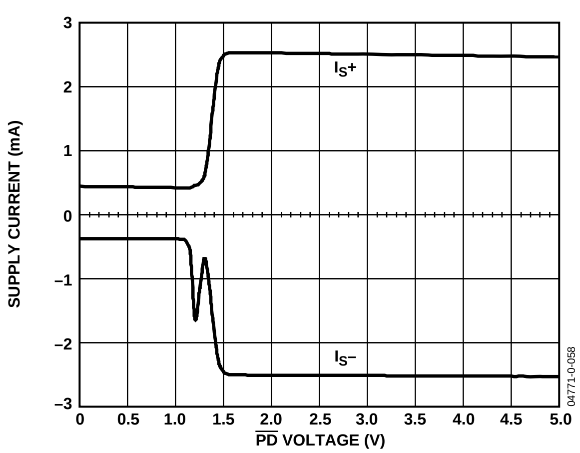


Figure 55. Supply Current vs. $\overline{PD}$ Voltage

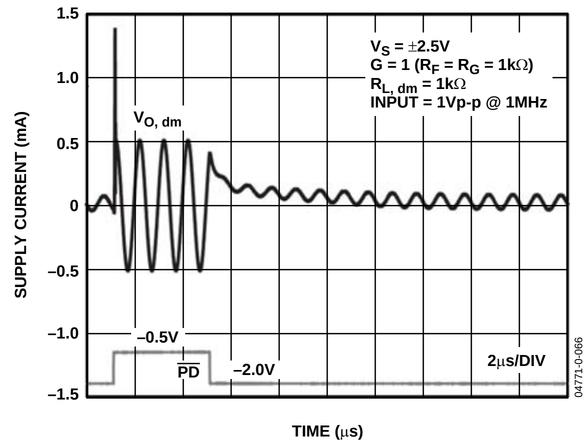


Figure 56. Power-Down Transient Response

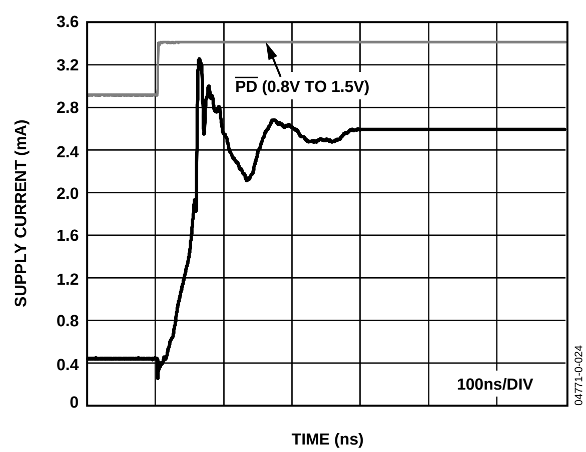


Figure 57. Power-Down Turn-On Time

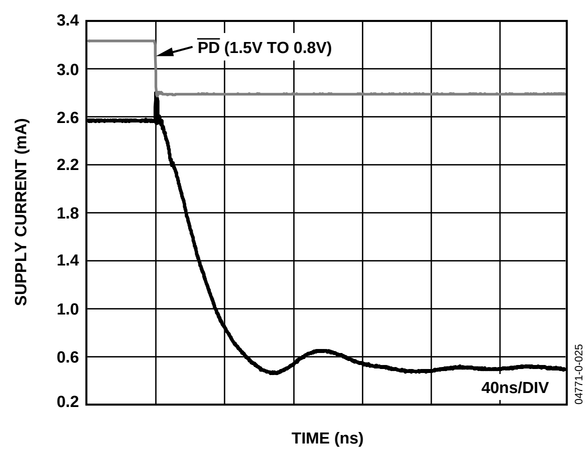


Figure 58. Power-Down Turn-Off Time

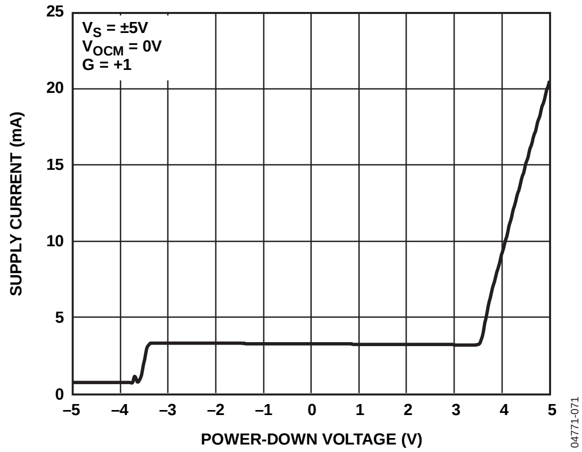


Figure 59. Supply Current vs. Power-Down Voltage

TEST CIRCUITS

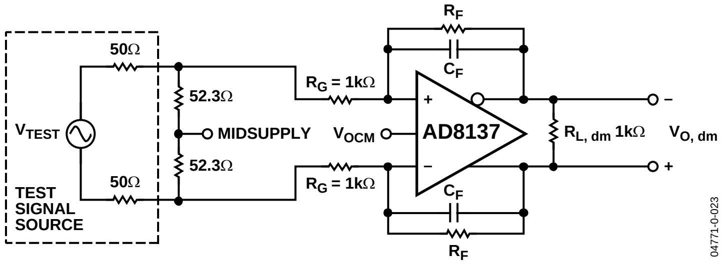


Figure 60. Basic Test Circuit

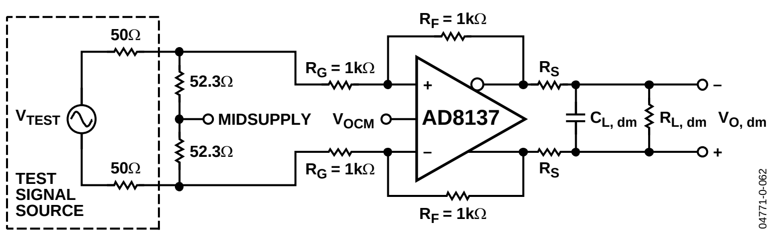


Figure 61. Capacitive Load Test Circuit, G = 1

THEORY OF OPERATION

The AD8137 is a low power, low cost, fully differential voltage feedback amplifier that features a rail-to-rail output stage, common-mode circuitry with an internally derived common-mode reference voltage, and bias shutdown circuitry. The amplifier uses two feedback loops to separately control differential and common-mode feedback. The differential gain is set with external resistors as in a traditional amplifier, and the output common-mode voltage is set by an internal feedback loop, controlled by an external V_{OCM} input. This architecture makes it easy to set arbitrarily the output common-mode voltage level without affecting the differential gain of the amplifier.

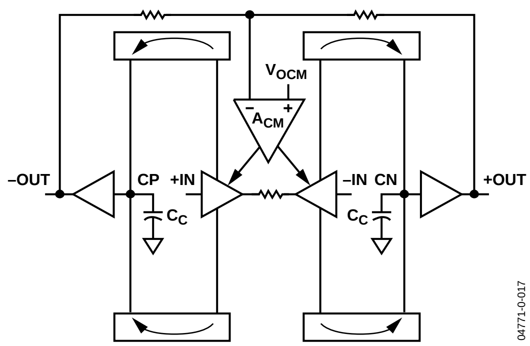


Figure 62. Block Diagram

From Figure 62, the input transconductance stage is an H-bridge whose output current is mirrored to high impedance nodes CP and CN. The output section is traditional H-bridge driven circuitry with common emitter devices driving nodes +OUT and –OUT. The 3 dB point of the amplifier is defined as

$$BW = \frac{g_m}{2\pi \times C_C}$$

where:

g_m is the transconductance of the input stage.

C_C is the total capacitance on node CP/CN (capacitances CP and CN are well matched).

For the AD8137, the input stage g_m is ~1 mA/V and the capacitance C_C is 3.5 pF, setting the crossover frequency of the amplifier at 41 MHz. This frequency generally establishes an amplifier's unity gain bandwidth, but with the AD8137, the closed-loop bandwidth depends upon the feedback resistor value as well (see Figure 17). The open-loop gain and phase simulations are shown in Figure 63.

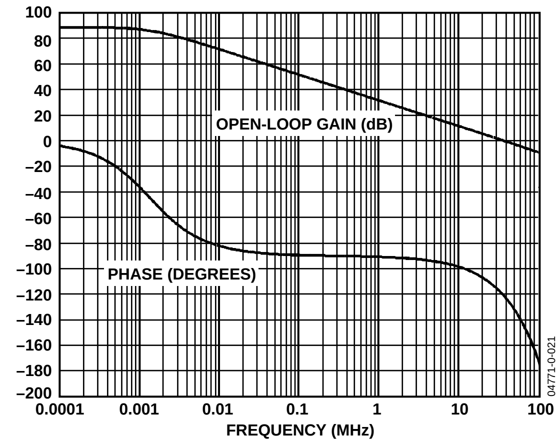


Figure 63. Open-Loop Gain and Phase

In Figure 62, the common-mode feedback amplifier A_{CM} samples the output common-mode voltage, and by negative feedback forces the output common-mode voltage to be equal to the voltage applied to the V_{OCM} input. In other words, the feedback loop servos the output common-mode voltage to the voltage applied to the V_{OCM} input. An internal bias generator sets the V_{OCM} level to approximately midsupply; therefore, the output common-mode voltage is set to approximately midsupply when the V_{OCM} input is left floating. The source resistance of the internal bias generator is large and can be overridden easily by an external voltage supplied by a source with a relatively small output resistance. The V_{OCM} input can be driven to within approximately 1 V of the supply rails while maintaining linear operation in the common-mode feedback loop.

The common-mode feedback loop inside the AD8137 produces outputs that are highly balanced over a wide frequency range without the requirement of tightly matched external components, because it forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase.

APPLICATIONS INFORMATION

ANALYZING A TYPICAL APPLICATION WITH MATCHED R_F AND R_G NETWORKS

Typical Connection and Definition of Terms

Figure 64 shows a typical connection for the AD8137, using matched external R_F/R_G networks. The differential input terminals of the AD8137, V_{AP} and V_{AN}, are used as summing junctions. An external reference voltage applied to the V_{OCM} terminal sets the output common-mode voltage. The two output terminals, V_{OP} and V_{ON}, move in opposite directions in a balanced fashion in response to an input signal.

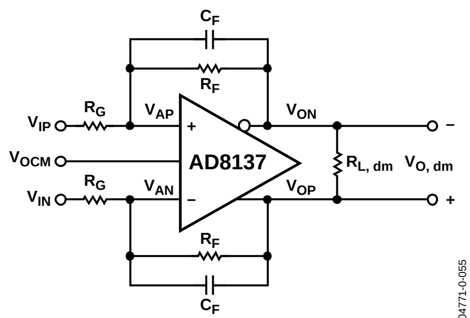


Figure 64. Typical Connection

The differential output voltage is defined as

$$V_{O, dm} = V_{OP} - V_{ON} \tag{1}$$

Common-mode voltage is the average of two voltages. The output common-mode voltage is defined as

$$V_{O, cm} = \frac{V_{OP} + V_{ON}}{2} \tag{2}$$

Output Balance

Output balance is a measure of how well V_{OP} and V_{ON} are matched in amplitude and how precisely they are 180° out of phase with each other. It is the internal common-mode feedback loop that forces the signal component of the output common-mode toward zero, resulting in the near perfectly balanced differential outputs of identical amplitude and are exactly 180° out of phase. The output balance performance does not require tightly matched external components, nor does it require that the feedback factors of each loop be equal to each other. Low frequency output balance is ultimately limited by the mismatch of an on-chip voltage divider.

Output balance is measured by placing a well-matched resistor divider across the differential voltage outputs and comparing the signal at the divider's midpoint with the magnitude of the differential output. By this definition, output balance is equal to the magnitude of the change in output common-mode voltage divided by the magnitude of the change in output differential mode voltage:

$$Output\ Balance = \left|\frac{\Delta V_{O, cm}}{\Delta V_{O, dm}}\right| \tag{3}$$

The differential negative feedback drives the voltages at the summing junctions V_{AN} and V_{AP} to be essentially equal to each other.

$$V_{AN} = V_{AP} \tag{4}$$

The common-mode feedback loop drives the output common-mode voltage, sampled at the midpoint of the two internal common-mode tap resistors in Figure 62, to equal the voltage set at the V_{OCM} terminal. This ensures that

$$V_{OP} = V_{OCM} + \frac{V_{O, dm}}{2} \tag{5}$$

and

$$V_{ON} = V_{OCM} - \frac{V_{O, dm}}{2} \tag{6}$$

ESTIMATING NOISE, GAIN, AND BANDWITH WITH MATCHED FEEDBACK NETWORKS

Estimating Output Noise Voltage and Bandwidth

The total output noise is the root-sum-squared total of several statistically independent sources. Because the sources are statistically independent, the contributions of each must be individually included in the root-sum-square calculation. Table 7 lists recommended resistor values and estimates of bandwidth and output differential voltage noise for various closed-loop gains. For most applications, 1% resistors are sufficient.

Table 7. Recommended Values of Gain-Setting Resistors and Voltage Gain for Various Closed-Loop Gains

Gain	R_G (Ω)	R_F (Ω)	3 dB Bandwidth (MHz)	Total Output Noise (nV/√Hz)
1	1 k	1 k	72	18.6
2	1 k	2 k	40	28.9
5	1 k	5 k	12	60.1
10	1 k	10 k	6	112.0

The differential output voltage noise contains contributions from the AD8137's input voltage noise and input current noise as well as those from the external feedback networks.

The contribution from the input voltage noise spectral density is computed as

$$Vo\_n1 = v_n\left(1+\frac{R_F}{R_G}\right)\text{, or equivalently, } v_n/\beta \quad (7)$$

where v_n is defined as the input-referred differential voltage noise. This equation is the same as that of traditional op amps.

The contribution from the input current noise of each input is computed as

$$Vo\_n2 = i_n\,(R_F) \quad (8)$$

where i_n is defined as the input noise current of one input. Each input needs to be treated separately because the two input currents are statistically independent processes.

The contribution from each R_G is computed as

$$Vo\_n3 = \sqrt{4kTR_G}\left(\frac{R_F}{R_G}\right) \quad (9)$$

This result can be intuitively viewed as the thermal noise of each R_G multiplied by the magnitude of the differential gain.

The contribution from each R_F is computed as

$$Vo\_n4 = \sqrt{4kTR_F} \quad (10)$$

Voltage Gain

The behavior of the node voltages of the single-ended-to-differential output topology can be deduced from the signal definitions and Figure 64. Referring to Figure 64, $C_F = 0$ and setting $V_{IN} = 0$, one can write:

$$\frac{V_{IP}-V_{AP}}{R_G} = \frac{V_{AP}-V_{ON}}{R_F} \quad (11)$$

$$V_{AN} = V_{AP} = V_{OP}\left[\frac{R_G}{R_F+R_G}\right] \quad (12)$$

Solving the previous two equations and setting V_{IP} to V_i gives the gain relationship for $V_{O,\,dm}/V_i$.

$$V_{OP} - V_{ON} = V_{O,\,dm} = \frac{R_F}{R_G}V_i \quad (13)$$

An inverting configuration with the same gain magnitude can be implemented by simply applying the input signal to V_{IN} and setting $V_{IP} = 0$. For a balanced differential input, the gain from $V_{IN,\,dm}$ to $V_{O,\,dm}$ is also equal to R_F/R_G, where $V_{IN,\,dm} = V_{IP} - V_{IN}$.

Feedback Factor Notation

When working with differential drivers, it is convenient to introduce the feedback factor β, which is defined as

$$\beta \equiv \frac{R_G}{R_F+R_G} \quad (14)$$

This notation is consistent with conventional feedback analysis and is very useful, particularly when the two feedback loops are not matched.

Input Common-Mode Voltage

The linear range of the V_{AN} and V_{AP} terminals extends to within approximately 1 V of either supply rail. Because V_{AN} and V_{AP} are essentially equal to each other, they are both equal to the amplifier's input common-mode voltage. Their range is indicated in the specifications tables as input common-mode range. The voltage at V_{AN} and V_{AP} for the connection diagram in Figure 64 can be expressed as

$$V_{AN} = V_{AP} = V_{ACM} = \left(\frac{R_F}{R_F+R_G}\times\frac{(V_{IP}+V_{IN})}{2}\right)+\left(\frac{R_G}{R_F+R_G}\times V_{OCM}\right) \quad (15)$$

where V_{ACM} is the common-mode voltage present at the amplifier input terminals.

Using the β notation, Equation (15) can be written as

$$V_{ACM} = \beta V_{OCM} + (1-\beta)V_{ICM} \quad (16)$$

or equivalently,

$$V_{ACM} = V_{ICM} + \beta(V_{OCM} - V_{ICM}) \quad (17)$$

where V_{ICM} is the common-mode voltage of the input signal, that is

$$V_{ICM} \equiv \frac{V_{IP}+V_{IN}}{2}$$

For proper operation, the voltages at V_{AN} and V_{AP} must stay within their respective linear ranges.

Calculating Input Impedance

The input impedance of the circuit in Figure 64 depends on whether the amplifier is being driven by a single-ended or a differential signal source. For balanced differential input signals, the differential input impedance ($R_{IN,\,dm}$) is simply

$$R_{IN,\,dm} = 2R_G \quad (18)$$

For a single-ended signal (for example, when V_{IN} is grounded and the input signal drives V_{IP}), the input impedance becomes

$$R_{IN} = \frac{R_G}{1-\dfrac{R_F}{2(R_G+R_F)}} \quad (19)$$

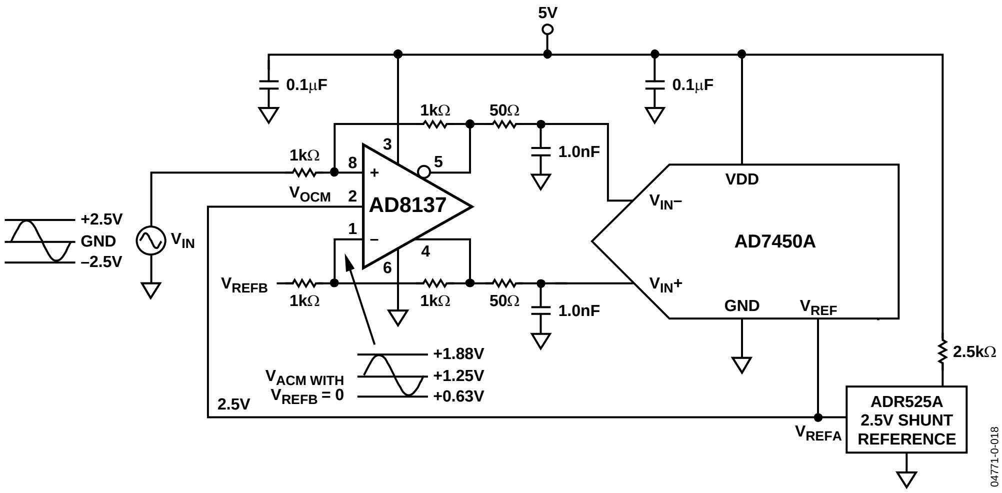


Figure 65. AD8137 Driving AD7450A, 12-Bit ADC

The input impedance of a conventional inverting op amp configuration is simply R_G; however, it is higher in Equation 19 because a fraction of the differential output voltage appears at the summing junctions, V_{AN} and V_{AP}. This voltage partially bootstraps the voltage across the input resistor R_G, leading to the increased input resistance.

Input Common-Mode Swing Considerations

In some single-ended-to-differential applications, when using a single-supply voltage, attention must be paid to the swing of the input common-mode voltage, V_{ACM}.

Consider the case in Figure 65, where V_{IN} is 5 V p-p swinging about a baseline at ground and V_{REFB} is connected to ground. The input signal to the AD8137 is originating from a source with a very low output resistance.

The circuit has a differential gain of 1.0 and β = 0.5. V_{ICM} has an amplitude of 2.5 V p-p and is swinging about ground. Using the results in Equation 16, the common-mode voltage at the inputs of the AD8137, V_{ACM}, is a 1.25 V p-p signal swinging about a baseline of 1.25 V. The maximum negative excursion of V_{ACM} in this case is 0.63 V, which exceeds the lower input common-mode voltage limit.

One way to avoid the input common-mode swing limitation is to bias V_{IN} and V_{REF} at midsupply. In this case, V_{IN} is 5 V p-p swinging about a baseline at 2.5 V, and V_{REF} is connected to a low-Z 2.5 V source. V_{ICM} now has an amplitude of 2.5 V p-p and is swinging about 2.5 V. Using the results in Equation 17, V_{ACM} is calculated to be equal to V_{ICM} because $V_{OCM} = V_{ICM}$. Therefore, V_{ICM} swings from 1.25 V to 3.75 V, which is well within the input common-mode voltage limits of the AD8137. Another benefit seen by this example is that because $V_{OCM} = V_{ACM} = V_{ICM}$, no wasted common-mode current flows. Figure 66 illustrates a way to provide the low-Z bias voltage. For situations that do not require a precise reference, a simple voltage divider suffices to develop the input voltage to the buffer.

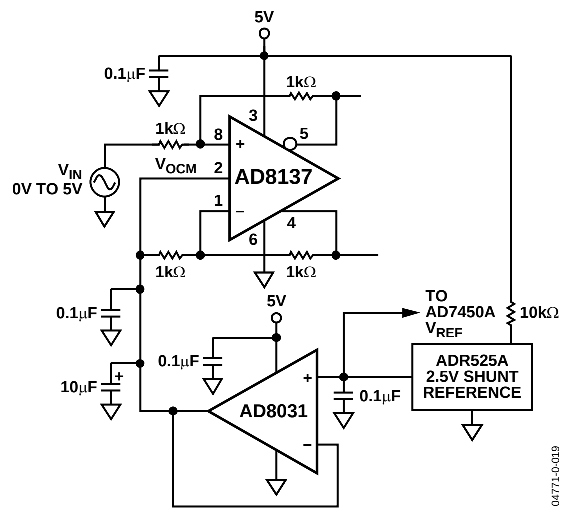


Figure 66. Low-Z Bias Source

Another way to avoid the input common-mode swing limitation is to use dual power supplies on the AD8137. In this case, the biasing circuitry is not required.

Bandwidth vs. Closed-Loop Gain

The 3 dB bandwidth of the AD8137 decreases proportionally to increasing closed-loop gain in the same way as a traditional voltage feedback operational amplifier. For closed-loop gains greater than 4, the bandwidth obtained for a specific gain can be estimated as

$$f_{-3dB}, V_{O,\ dm} = \frac{R_G}{R_G + R_F} \times (72\,\text{MHz}) \tag{20}$$

or equivalently, β(72 MHz).

This estimate assumes a minimum 90° phase margin for the amplifier loop, a condition approached for gains greater than 4. Lower gains show more bandwidth than predicted by the equation due to the peaking produced by the lower phase margin.

Estimating DC Errors

Primary differential output offset errors in the AD8137 are due to three major components: the input offset voltage, the offset between the V_{AN} and V_{AP} input currents interacting with the feedback network resistances, and the offset produced by the dc voltage difference between the input and output common-mode voltages in conjunction with matching errors in the feedback network.

The first output error component is calculated as

$$Vo\_e1 = V_{IO}\left(\frac{R_F + R_G}{R_G}\right), \text{ or equivalently as } V_{IO}/\beta \qquad (21)$$

where V_{IO} is the input offset voltage.

The second error is calculated as

$$Vo\_e2 = I_{IO}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_G R_F}{R_F + R_G}\right) = I_{IO}(R_F) \qquad (22)$$

where I_{IO} is defined as the offset between the two input bias currents.

The third error voltage is calculated as

$$Vo\_e3 = \Delta enr \times (V_{ICM} - V_{OCM}) \qquad (23)$$

where Δenr is the fractional mismatch between the two feedback resistors.

The total differential offset error is the sum of these three error sources.

Additional Impact of Mismatches in the Feedback Networks

The internal common-mode feedback network still forces the output voltages to remain balanced, even when the R_F/R_G feedback networks are mismatched. The mismatch, however, causes a gain error proportional to the feedback network mismatch.

Ratio-matching errors in the external resistors degrade the ability to reject common-mode signals at the V_{AN} and V_{IN} input terminals, similar to a four resistor, difference amplifier made from a conventional op amp. Ratio-matching errors also produce a differential output component that is equal to the V_{OCM} input voltage times the difference between the feedback factors (βs). In most applications using 1% resistors, this component amounts to a differential dc offset at the output that is small enough to be ignored.

Driving a Capacitive Load

A purely capacitive load reacts with the bondwire and pin inductance of the AD8137, resulting in high frequency ringing in the transient response and loss of phase margin. One way to minimize this effect is to place a small resistor in series with each output to buffer the load capacitance. The resistor and load capacitance forms a first-order, low-pass filter; therefore, the resistor value should be as small as possible. In some cases, the ADCs require small series resistors to be added on their inputs.

Figure 37 and Figure 40 illustrate transient response vs. capacitive load and were generated using series resistors in each output and a differential capacitive load.

Layout Considerations

Standard high speed PCB layout practices should be adhered to when designing with the AD8137. A solid ground plane is recommended and good wideband power supply decoupling networks should be placed as close as possible to the supply pins.

To minimize stray capacitance at the summing nodes, the copper in all layers under all traces and pads that connect to the summing nodes should be removed. Small amounts of stray summing-node capacitance cause peaking in the frequency response, and large amounts can cause instability. If some stray summing-node capacitance is unavoidable, its effects can be compensated for by placing small capacitors across the feedback resistors.

Terminating a Single-Ended Input

Controlled impedance interconnections are used in most high speed signal applications, and they require at least one line termination. In analog applications, a matched resistive termination is generally placed at the load end of the line. This section deals with how to properly terminate a single-ended input to the AD8137.

The input resistance presented by the AD8137 input circuitry is seen in parallel with the termination resistor, and its loading effect must be taken into account. The Thevenin equivalent circuit of the driver, its source resistance, and the termination resistance must all be included in the calculation as well. An exact solution to the problem requires solution of several simultaneous algebraic equations and is beyond the scope of this data sheet. An iterative solution is also possible and is easier, especially considering the fact that standard resistor values are generally used.

Figure 67 shows the AD8137 in a unity-gain configuration, and with the following discussion, provides a good example of how to provide a proper termination in a 50 Ω environment.

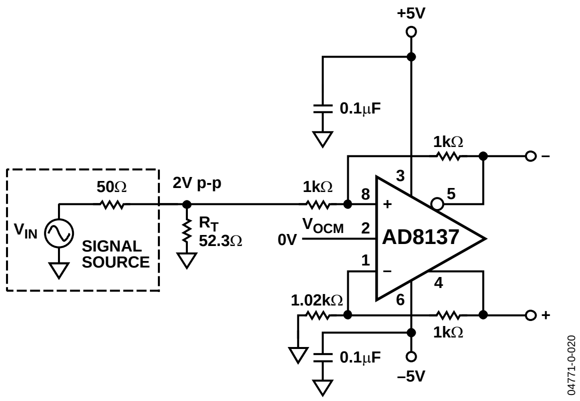


Figure 67. AD8137 with Terminated Input

The 52.3 Ω termination resistor, R_T, in parallel with the 1 kΩ input resistance of the AD8137 circuit, yields an overall input resistance of 50 Ω that is seen by the signal source. To have matched feedback loops, each loop must have the same R_G if it has the same R_F. In the input (upper) loop, R_G is equal to the 1 kΩ resistor in series with the (+) input plus the parallel combination of R_T and the source resistance of 50 Ω. In the upper loop, R_G is therefore equal to 1.03 kΩ. The closest standard value is 1.02 kΩ and is used for R_G in the lower loop.

Things become more complicated when it comes to determining the feedback resistor values. The amplitude of the signal source generator V_{IN} is two times the amplitude of its output signal when terminated in 50 Ω. Therefore, a 2 V p-p terminated amplitude is produced by a 4 V p-p amplitude from V_S. The Thevenin equivalent circuit of the signal source and R_T must be used when calculating the closed-loop gain because R_G in the upper loop is split between the 1 kΩ resistor and the Thevenin resistance looking back toward the source. The Thevenin voltage of the signal source is greater than the signal source output voltage when terminated in 50 Ω because R_T must always be greater than 50 Ω. In this case, R_T is 52.3 Ω and the Thevenin voltage and resistance are 2.04 V p-p and 25.6 Ω, respectively.

Now the upper input branch can be viewed as a 2.04 V p-p source in series with 1.03 kΩ. Because this is to be a unity-gain application, a 2 V p-p differential output is required, and R_F must therefore be 1.03 kΩ × (2/2.04) = 1.01 kΩ ≈ 1 kΩ.

This example shows that when R_F and R_G are large compared to R_T, the gain reduction produced by the increase in R_G is essentially cancelled by the increase in the Thevenin voltage caused by R_T being greater than the output resistance of the signal source. In general, as R_F and R_G become smaller in terminated applications, R_F needs to be increased to compensate for the increase in R_G.

When generating the typical performance characteristics data, the measurements were calibrated to take the effects of the terminations on closed-loop gain into account.

Power Down

The AD8137 features a $\overline{PD}$ pin that can be used to minimize the quiescent current consumed when the device is not being used. $\overline{PD}$ is asserted by applying a low logic level to Pin 7. The threshold between high and low logic levels is nominally 1.1 V above the negative supply rail. See Table 1 to Table 3 for the threshold limits. Do not connect the $\overline{PD}$ pin directly to V_{S+}; this causes the amplifier to draw excessive supply current, see Figure 59.

DRIVING AN ADC WITH GREATER THAN 12-BIT PERFORMANCE

Because the AD8137 is suitable for 12-bit systems, it is desirable to measure the performance of the amplifier in a system with greater than 12-bit linearity. In particular, the effective number of bits (ENOB) is most interesting. The AD7687, 16-bit, 250 KSPS ADC performance makes it an ideal candidate for showcasing the 12-bit performance of the AD8137.

For this application, the AD8137 is set in a gain of 2 and driven single-ended through a 20 kHz band-pass filter, while the output is taken differentially to the input of the AD7687 (see Figure 68). This circuit has mismatched R_G impedances and, therefore, has a dc offset at the differential output. It is included as a test circuit to illustrate the performance of the AD8137. Actual application circuits should have matched feedback networks.

For an AD7687 input range up to −1.82 dBFS, the AD8137 power supply is a single 5 V applied to V_{S+} with V_{S-} tied to ground. To increase the AD7687 input range to −0.45 dBFS, the AD8137 supplies are increased to +6 V and −1 V. In both cases, the V_{OCM} pin is biased with 2.5 V and the $\overline{PD}$ pin is left floating. All voltage supplies are decoupled with 0.1 µF capacitors. Figure 69 and Figure 70 show the performance of the −1.82 dBFS setup and the −0.45 dBFS setup, respectively.

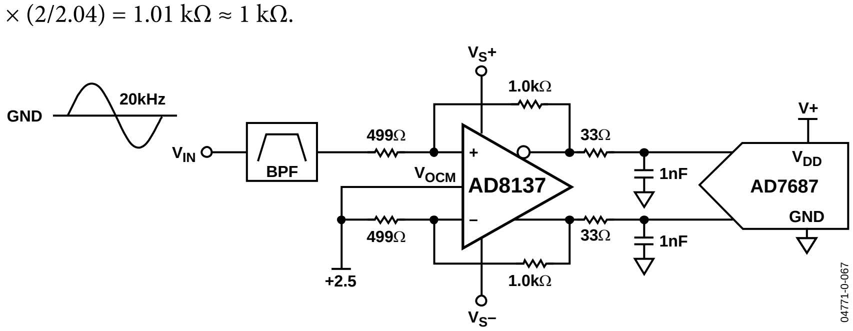


Figure 68. AD8137 Driving AD7687, 16-Bit 250 KSPS ADC

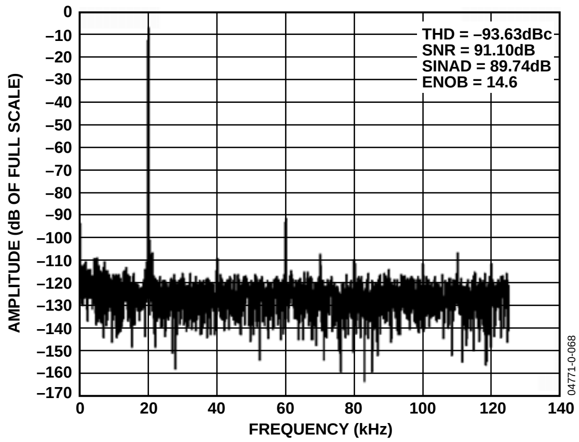


Figure 69. AD8137 Performance on Single 5 V Supply, −1.82 dBFS

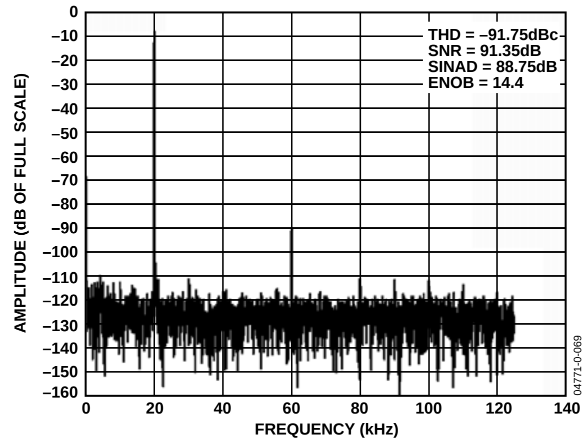


Figure 70. AD8137 Performance on +6 V, −1 V Supplies, −0.45 dBFS

OUTLINE DIMENSIONS

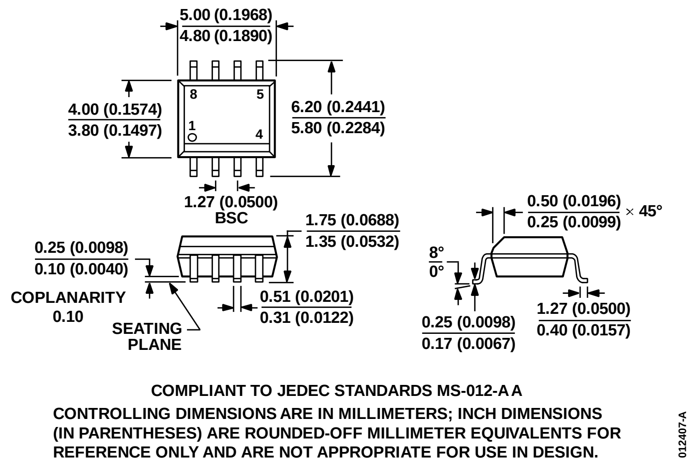


Figure 71. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

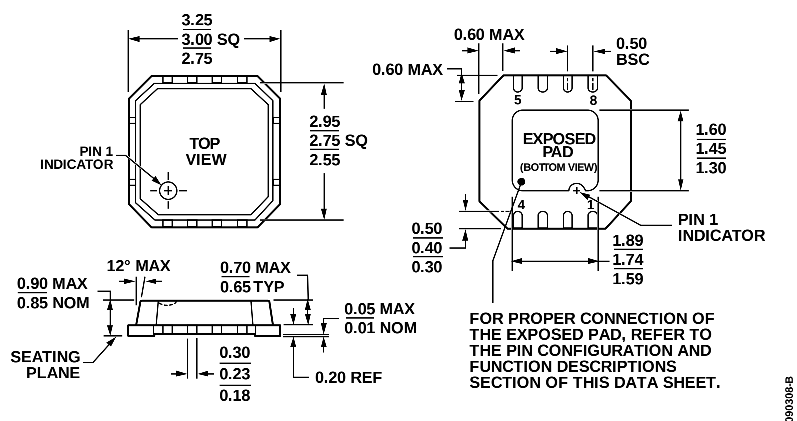


Figure 72. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8137YR	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8137YR-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8137YRZ	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8137YRZ-REEL	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8137YRZ-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
AD8137YCP-REEL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HFB
AD8137YCPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HFB#
AD8137YCPZ-REEL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HFB#
AD8137YCPZ-REEL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HFB#

[1] Z = RoHS Compliant Part; # denotes RoHS compliant part, may be top or bottom marked.

NOTES

D04771-0-12/09(C)