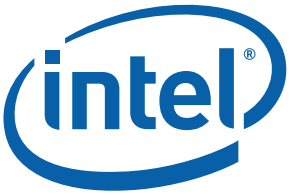

Intel® 7500/7510/7512 Scalable Memory Buffer

Datasheet

April 2011

Document Number: 322824-002

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Revision History

Document Number	Revision Number	Description	Date
322824	001	• Initial release of the document.	March 2010
322824	002	• Added Intel 7510/7512 Scalable Memory Buffer	April 2011

§

1 Introduction

1.1 Intel® 7500/7510/7512 Scalable Memory Buffer Overview

Intel® 7500/7510/7512 Scalable Memory Buffer supports DDR3 SDRAM main memory. It interfaces with the host memory controller via an Intel® Scalable Memory Interconnect (Intel® SMI) channel.

Intel 7500/7510/7512 Scalable Memory Buffer is responsible for handling Intel SMI channel and memory requests to and from the local DIMM. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management.

The Intel®7500 Scalable Memory Buffer is the first generation product of this memory buffer family; the Intel 7510 Scalable Memory Buffer adds greater memory capacity over its predecessor while the Intel 7512 Scalable Memory Buffer is the low power version of Intel 7510 Scalable Memory Buffer.

1.2 Intel® 7500/7510/7512 Scalable Memory Buffer Functionality

The following is a summary of Intel 7500/7510/7512 Scalable Memory Buffer functionality.

1.2.1 Intel® SMI Functionality

Intel 7500/7510/7512 Scalable Memory Buffer provides a single Intel SMI interface, with the following functionality.

- Intel SMI protocol and signalling includes support for the following:
  - 4.8 Gbps, 5.86 Gbps, 6.4 Gbps signalling
  - forwarded clock fail-over Northbound (NB) and Southbound (SB).
  - 9 data lanes plus 1 CRC lane plus 1 spare lane SB.
  - 12 data lanes plus 1 CRC lane plus 1 spare NB.
  - Support for integrating RDIMM thermal sensor information into Intel SMI Status Frame.
- No support for daisy chaining (Intel 7500/7510/7512 Scalable Memory Buffer is the only Intel SMI device in the channel).
- No support for FB-DIMM1 protocol and signaling.

1.2.2 DDR3 Functionality

Intel 7500/7510/7512 Scalable Memory Buffer provides two DDR3 interfaces. Each interface provides the following functionality. DDR3 protocol and signalling, includes support for the following:

  - Up to two RDIMMs per DDR3 bus
  - Support for DDR3L (low power) RDIMMs *(not supported by Intel 7500 Scalable Memory Buffer)*

  - Up to eight logical ranks per DDR3 bus (sixteen per Intel 7500/7510/7512 Scalable Memory Buffer).
  - 800 MT/s, 978 MT/s, or 1067 MT/s (both DDR3 buses must operate at the same frequency).
  - Single Rank x4, Dual Rank x4, Single Rank x8, Dual Rank x8, Quad Rank x4, Quad Rank x8
  - 1 GB, 2 GB, 4 GB, 8 GB, 16 GB, and 32 GB DIMM *(Intel 7500 Scalable Memory Buffer does not support 32 GB DIMMs)*
  - DRAM device sizes: 1 Gb, 2 Gb, 4 Gb *(Intel 7500 Scalable Memory Buffer does not support 4 Gb device size)*
  - DIMMs with independent device configurations.
    DIMMs with different numbers of row, column, bank and ranks can be mixed.
    DIMMs with different device sizes can be mixed.
    DIMMs with x4 and x8 widths can be mixed. (Host lockstep requirements may impose additional requirements on DIMMs on separate Intel SMI channels).
  - All DIMMs attached to Intel 7500/7510/7512 Scalable Memory Buffer must run with a common frequency and core timings). (Host lockstep requirements may impose additional requirements on DIMMs on separate Intel SMI channels).
  - DDR buses may contain different number of DIMMs, zero through two. (Host lockstep requirements may impose additional requirements on DIMMs on separate Intel SMI channels).
  - Cmd/Addr parity generation and error logging.
- No support for non-ECC DIMMs
- No support for non-zero Additive Latency
- No support for Data mask functionality
- No support for BL = 8 for host initiated transactions (supported on with MEMBIST). Only BL=4 supported for host initiated transactions.
- No support for DDR2 protocol and signaling
- Support for integrating RDIMM thermal sensor information into Intel SMI Status Frame.

Intel 7500 Scalable Memory Buffer supports the following 2-DIMMs-Per-Channel (2DPC) configurations for each channel. The two channels are not required to have the same configuration. Intel 7500 Scalable Memory Buffer also supports one channel unpopulated, with the other channel having one of the configurations shown below.

Table 1-1. 2DPC Supported Configurations

CONFIG	SLOT1	SLOT0
CONFIG-1	QR RDIMM	QR RDIMM
CONFIG-2	DR RDIMM	QR RDIMM
CONFIG-3	SR RDIMM	QR RDIMM
CONFIG-5	DR RDIMM	DR RDIMM
CONFIG-6	SR RDIMM	DR RDIMM
CONFIG-8	DR RDIMM	SR RDIMM
CONFIG-9	SR RDIMM	SR RDIMM
CONFIG-10	Empty	QR RDIMM
CONFIG-11	Empty	DR RDIMM
CONFIG-12	Empty	SR RDIMM

1.2.3 Management/DFx Functionality

- SMbus slave interface at 100 KHz. Provides access to all configuration and status registers out of band.
- Testing/debug modes:
  - LAI Mode
    Provides demuxed northbound and southbound Intel SMI traffic in LA compatible signal levels and timing format through the reuse of the existing device DDR3 I/O pins.
    Triggers on programmable events in normal operation.
  - MEMBIST
    Memory Built In Self Test for memory initialization during system boot up and for testing the high speed interface to DDR3 RDIMMs.
  - Intel® Interconnect BIST
    Interconnect Built In Self Test for at speed Intel SMI channel testing in a system or HVM environment.

1.3 Intel 7500/7510/7512 Scalable Memory Buffer Interfaces and Logical View

The following table lists Intel 7500 Scalable Memory Buffer support for features and is followed by exceptions:

Table 1-2. Intel® Scalable Memory Interconnect (Intel® SMI) Architecture and Protocol Support on Intel® 7500/7510/7512 Scalable Memory Buffer (Sheet 1 of 2)

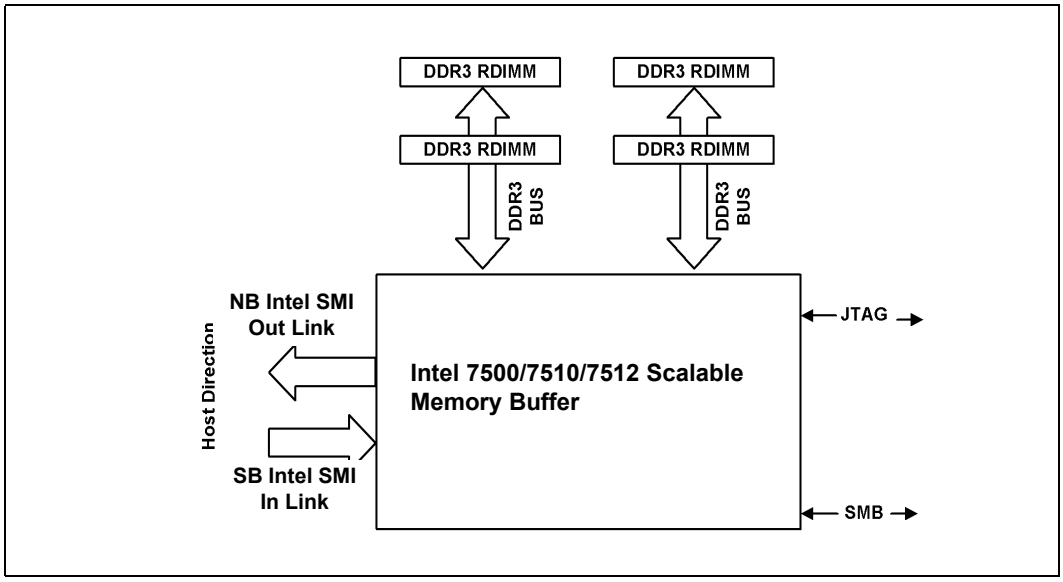
Feature		Intel 7500/7510/7512 Scalable Memory Buffer Support
Link Frequency		4.8 Gb/s, 5.86 Gb/s and 6.4 Gb/s
NB ECC Modes	14-lane	Not Supported
	14-lane failover	Supported
	13-lane	Supported
	13-lane failover	Supported
NB 12-lane mode (no ECC)		Not Supported
NB 15th Spare Lane		Not Supported
SB ECC Modes	Normal	Supported
	Fail-over	Supported
	Fail-over to Spare	Supported
SB 11th Spare Lane		Supported
Forwarded Clock Failover		Supported
Sync command with non-zero status delay		Not Supported
Recalibrate Command		Not Supported
Lane Staggering		Not Supported
Data Scrambling		Not Supported
Logic Analyzer Mode		Supported
L0s Protocol		Not Supported
Variable Read Latency		Not Supported

Table 1-2. Intel® Scalable Memory Interconnect (Intel® SMI) Architecture and Protocol Support on Intel® 7500/7510/7512 Scalable Memory Buffer (Sheet 2 of 2)

Feature		Intel 7500/7510/7512 Scalable Memory Buffer Support
Northbound Disable on Idle		Not Supported
Quad Rank	Mode A	Supported
	Mode B	Not Supported
Broadcast Configuration Write Commands		Not Supported
ZQ Calibration Commands to Multiple Ranks		Not Supported

Figure 1-1 illustrates the Intel 7500/7510/7512 Scalable Memory Buffer and its interfaces. They consist of one Intel SMI link, two DDR3 buses, a JTAG interface, and an SMBus interface.

Figure 1-1. Intel® 7500/7510/7512 Scalable Memory Buffer Interfaces



1.3.1 Intel SMI Channel Interface

Intel SMI builds off of the foundation of the Fully Buffered DIMM (FBD) architecture, providing higher speed operation, support for DDR3 memory devices, as well as additional features. There are very few protocol changes from FB-DIMM to Intel SMI.

Intel 7500/7510/7512 Scalable Memory Buffer supports one Intel SMI Channel interface consisting of a bidirectional link interface using high-speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wide (plus an 11th spare lane) and carries commands and write data from the host memory controller.

The northbound output link is 13 lanes wide (plus a 14th spare lane) and carries read return data or status information from the Intel 7500/7510/7512 Scalable Memory Buffer back towards the host.

In addition, Intel 7500/7510/7512 Scalable Memory Buffer will have a differential forwarded clock lane in each direction. The SB and NB links may be operated in fail over mode to map out a bad bit lane or a bad clock lane. Intel 7500/7510/7512 Scalable Memory Buffer will support Intel SMI interface speeds of 4.8 Gbps, 5.86 Gbps and 6.4 Gbps

1.3.2 DDR3 Bus Interface

DDR3 builds off of the foundation of the DDR2 architecture, providing higher speed operation, as well as additional features.

Each DDR3 bus supports up to two DIMMs, and up to eight logical ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals. Intel 7500/7510/7512 Scalable Memory Buffer supports four-transfer bursts on the data and check-bit lines at 800 MT/s, 978 MT/s or 1067 MT/s.

Supported DIMM types are:

- DDR3 RDIMM
- DDR3L RDIMM (Low Voltage DDR3 RDIMMs @1.35 V) *(not supported by Intel 7500 Scalable Memory Buffer)*

In this specification, the term DIMM may be used interchangeably to refer to DDR3 RDIMM, or DDR3L RDIMM unless a specific DIMM type is called out.

Propagation delays between read and write data strobe lanes on a given bus can differ. Each strobe can be calibrated by hardware state machines during boot.

Intel 7500/7510/7512 Scalable Memory Buffer provides parity on the command/address outputs, and accepts and logs parity error signals from the RDIMMs, as defined in the *Registering Clock Driver with Parity for DDR3 RDIMM Applications* specification.

Intel 7500/7510/7512 Scalable Memory Buffer can connect to the EVENT_N signals from Thermal Sensor Modules on the RDIMMs, and report information from these signals back to the host in Intel SMI status frames.

1.3.3 SMBus Slave Interface

Intel 7500/7510/7512 Scalable Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the Intel SMI link. Accesses can occur concurrent with normal Intel SMI traffic, or before the Intel SMI link has been trained. Intel 7500/7510/7512 Scalable Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz.

SMBus access to Intel 7500/7510/7512 Scalable Memory Buffer is a requirement to boot a system. This provides a mechanism to set link strength, frequency and other parameters needed to insure robust operation given platform specific configurations.

One SMBus address strap is used by Intel 7500/7510/7512 Scalable Memory Buffer to allow up to two Intel 7500/7510/7512 Scalable Memory Buffers to reside on a bus.

For detailed information about the SMBus, refer to the *System Management Bus (SMBus) Specification*.

1.3.4 JTAG Interface

A JTAG (Joint Test Action Group) port is supported for boundary scan. Not all I/Os are boundary scannable. Using the JTAG port to access Intel 7500/7510/7512 Scalable Memory Buffer information during normal mode of operation at runtime is not supported.

1.4 Debug and Logic Analyzer Interface

In addition to normal operation, Intel 7500/7510/7512 Scalable Memory Buffer will support a logic analyzer mode of operation to provide debug and test support.

Intel 7500/7510/7512 Scalable Memory Buffer can be used to support the connection of Intel SMI links to a Logic Analyzer (LA) for debug.

Intel 7500/7510/7512 Scalable Memory Buffer debug functionality:

- Reconfigures DDR3 interface to act as a Logic Analyzer Interface (LAI) to observe activity on Intel SMI high speed links
- Triggers on programmable events in normal operation

Please see Chapter 3 for more detail on the Intel 7500/7510/7512 Scalable Memory Buffer implementation of this operating mode.

1.5 References

Table 1-3. References

Document	Revision
JESD79-3 DDR3 SDRAM Specification	April 2008
Mobile Platform Memory Module Thermal Sensor Component Specification	June 2007
Registering Clock Driver with Parity for DDR3 RDIMM Applications	3/12/2008
PCI Local Bus Specification	2.2
System Management Bus (SMBus) Specification	2.0
IEEE 1149.1a-1993 (JTAG)	

1.6 List of Terms and Abbreviations

Term	Definition
AMB	Advanced Memory Buffer - First Generation
AMB2	Advanced Memory Buffer - Second Generation
DDR	Double Data Rate (SDRAM)
DDR2	Double Data Rate - Second Generation
DDR3	Double Data Rate - Third Generation
DDR3L	Low Voltage DDR3 DIMM
DDR Bus	A DDR Bus consists of a data bus with 72 bits of data and an ADDR/DDR Data bus A DDR data bus consists of 72 bits of data, divided into 18 data groups. DDR Data group Each data group consists of 4 data signals and a differential strobe pair.
DRAM Page	The DRAM cells selected by the Row Address
DRAM	Dynamic Random Access Memory
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR bus.
ECC	Error Correction Code. For Intel 7500/7510/7512 Scalable Memory Buffer, this is a chip disable code.
EMI	Electromagnetic interference
FB-DIMM (FBD-1, FBD)	Fully Buffered DIMM - First Generation
Intel SMI	Intel Scalable Memory Interconnect
FB-DIMM Channel	Combination of 10 or 11 lane Southbound Links and 13 or 14 lane Northbound Links that make up a logical memory channel from host perspective
Frame	Group of bits containing commands or data
ISI	Inter Symbol Interference
LA	Logic Analyzer
LAI	Logic Analyzer Interface
Lane	Differential pair of receivers or transmitters
Link	High speed parallel Differential Point-to-Point interface
LP SKU	Low Power Intel 7510/7512 Scalable Memory Buffer
Mesochronous	Same frequency, but unknown phase relationship
Northbound (NB)	The direction of signals running from the furthest DIMM toward the host.
RDIMM	Registered Dual In-Line Memory Module.
Southbound (SB)	The direction of signals running from the host toward the furthest DIMM.

§

2 Electrical and Power

2.1 Storage Conditions

Table 2-1 include a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceeded in storage or transportation.

Table 2-1. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{absolute\ storage}$	The minimum/maximum non-operating device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-55°C	125°C	1,2,3
$T_{sustained\ storage}$	The minimum/maximum device in storage temperature (in shipping media) for a sustained period of time	-5°C	40°C	4,5
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	-60% @ 24°		5,6
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with customer shelf life	0 months	6 months	6

Notes:
1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard and MAS document. Non-adherence may affect component reliability.
3. $T_{absolute\ storage}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28°C) Post board attach storage temperature limits are not specified for non-Intel® branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{sustained\ storage}$ and customer shelf life in applicable Intel box and bags.

2.2 Electrical DC Parameters

2.2.1 Absolute Maximum Ratings

Table 2-2. Absolute Maximum Ratings Over Operating Free-Air Temperature Range (See Note 1)

Symbol	Parameter	Min	Max	Unit
V_{DD1P5}	Supply voltage DRAM Interface	-0.3	1.8	V
$V_{IN\ (DDR3)}$, $V_{OUT\ (DDR3)}$	Voltage on any DDR3 interface pin relative to Vss	-0.3	1.8	V
V_{CC1P1}	Supply voltage for Core	-0.3	1.4	V
$V_{CCFBD1P1}$	Supply voltage for Intel SMI Interface	-0.3	1.4	V
$V_{CCTTA1P1}$	Supply voltage for DDR logic	-0.3	1.4	V

Table 2-2. Absolute Maximum Ratings Over Operating Free-Air Temperature Range (See Note 1)

Symbol	Parameter	Min	Max	Unit
$V_{IN\ (SMI)}$, $V_{OUT\ (SMI)}$	Voltage on any Intel SMI interface pin relative to Vss	-0.3	1.4	V
$I_{OUTK\ (SMI)}$	Output Clamp Current (Intel SMI)		30	mA
$I_{OUT\ (SMI)}$	Continuous Output Current (Intel SMI)		12	mA

Notes:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 2.2.2, "Component Operating Parameters" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2.2 Component Operating Parameters

Table 2-3. Intel® 7500 Scalable Memory Buffer Operating DC Electrical Parameters

Parameter	Min	Typ	Max	Units	Notes
V_{CC1P1}, $V_{CCTTA1P1}$	1.087	1.1	1.153	V	1
$V_{CCFBD1P1}$	1.087	1.1	1.153	V	2
V_{DD1P5}	1.455	1.5	1.545	V	2
V_{REG1P8}	1.746	1.8	1.854	V	1
T_{CASE8}	5		92	°C	

Notes:
1. Maximum allowed AC Noise voltage tolerance (Total allowable Low frequency Noise upto 20 MHz BW) =±2%. Noise sources could be VR ripple and/or any noise coupling from other interfaces/components sharing the same power plane on platform.
2. Maximum allowed AC Noise voltage tolerance (Total allowable Low frequency Noise upto 20 MHz BW) =±1%. Noise sources could be VR ripple and/or any noise coupling from other interfaces/components sharing the same power plane on platform.

Table 2-4. Intel® 7510 Scalable Memory Buffer Operating Parameters (Standard SKU)

Parameter	Units	Min	Typ	Max	Notes
V_{CC1P1} (digital core)	Volts	1.097	1.11	1.163	1
$V_{CCFBD1P1}$ (analog Intel SMI)	Volts	1.097	1.11	1.163	2
$V_{CCTTA1P1}$ (analog DDR)	Volts	1.097	1.11	1.163	1
V_{DD1P5}	Volts	1.455	1.5	1.545	1
$V_{DD1P5(\ DDR3L)}$	Volts	1.31	1.35	1.39	1
V_{REG1P8}	Volts	1.746	1.8	1.854	1
T_{CASE8}	°C	5		92°C	

Notes:
1. Maximum allowed AC Noise voltage tolerance (Total allowable Low frequency Noise upto 20 MHz BW) =±2%. Noise sources could be VR ripple and/or any noise coupling from other interfaces/components sharing the same power plane on platform.
2. Maximum allowed AC Noise voltage tolerance (Total allowable Low frequency Noise upto 20 MHz BW) =±1%. Noise sources could be VR ripple and/or any noise coupling from other interfaces/components sharing the same power plane on platform.

Table 2-5. Intel® 7512 Scalable Memory Buffer Operating Parameters (Low Power SKU)

Parameter	Units	Min	Typ	Max	Notes
V_{CC1P1} (digital core)	Volts	0.946	0.956	0.985	1
$V_{CCFBD1P1}$ (analog Intel SMI)	Volts	1.087	1.1	1.153	2
$V_{CCTTA1P1}$ (analog DDR)	Volts	0.946	0.956	0.985	1
V_{DD1P5}	Volts	1.455	1.5	1.545	1
$V_{DD1P5(\ DDR3L)}$	Volts	1.31	1.35	1.39	1
V_{REG1P8}	Volts	1.746	1.8	1.854	1
T_{CASE8}	°C	5		92°C	

Notes:
1. Maximum allowed AC Noise voltage tolerance (Total allowable Low frequency Noise upto 20 MHz BW) =±2%. Noise sources could be VR ripple and/or any noise coupling from other interfaces/components sharing the same power plane on platform.
2. Maximum allowed AC Noise voltage tolerance (Total allowable Low frequency Noise upto 20 MHz BW) =±1%. Noise sources could be VR ripple and/or any noise coupling from other interfaces/components sharing the same power plane on platform.

Note: There will also be a V_{TT} termination supply at $V_{DDR}/2$ available on the DIMM but does not connect to the Intel 7500/7510/7512 Scalable Memory Buffer component.

2.2.3 Scalable Memory Buffer Pin Power Supply Specifications

Note: Intel 7510 Scalable memory Buffer is not supported with split-rail implementation.

Intel 7512 Scalable Memory Buffer is not supported with single 1.1 V VR implementation, and requires split-rail.

Refer to the Intel® 7500/7510/7512 Scalable Memory Buffer Thermal Mechanical Design Guidelines for details on the thermal power dissipation specifications.

Table 2-6. Intel 7500 Scalable Memory Buffer Active Power Specifications at DDR3-1067 MT/s for a Single 1.1 V VR

Conditions	Power Supply	Max Current	Units	Notes[1]
40% Utilization per DDR bus 67% Read, 33% Write	@1.1 V Analog	2.8	A	$V_{CCFBD1P1}$, $V_{CCTTA1P1}$
	@1.1 V Digital	4.6	A	V_{CC1P1}
	@1.5 V	4.0	A	V_{DD1P5}
	@1.8 V	0.16	A	V_{REG1P8}

Notes:
1. Voltage Regulators should be designed to meet Max Current specification.

Table 2-7. Intel 7510 Scalable Memory Buffer Power Specifications at 1067 for a Single 1.11 V VR (Standard SKU)

Conditions	Power Supply	Max Current	Units	Notes[1]
40% Utilization per DDR bus 67% Read, 33% Write	@1.11 V Analog	2.8	A	VCCFBD1P1 and VCCTTA1P1
	@1.11 V Digital	4.6	A	VCC1P1
	@1.5 V	4.0	A	V_{DD1P5}[2]
	@1.8 V	0.16	A	PLL

Notes:

1. Voltage Regulators should be designed to meet Max Current specification.
2. For DDR3L DIMMs, DDR I/O power supply must be @ 1.35 V, and max current=3.6 A.

Table 2-8. Intel 7512 Scalable Memory Buffer Active Power Specifications at 1067 for Two 1.1V VRs (a.k.a. Split-rail Implementation, Low Power SKU)

Conditions	Power Supply	Max Current	Units	Notes,[1]
40% Utilization per DDR bus 67% Read, 33% Write	@1.1 V Analog	2.4	A	VCCFBD1P1
	@0.956 V Analog/Digital	5.0	A	VCCTTA1P1 and VCC1P1
	@1.5 V	4.0	A	V_{DD1P5}[2]
	@1.8 V	0.16	A	PLL

Notes:

1. Voltage Regulators should be designed to meet Max Current specification.
2. for DDR3L DIMMs, DDR I/O power supply must be @ 1.35 V, and max current=3.6 A.

2.3 Reference Clock

2.3.1 Supported Clock Frequencies and Ratios

The core, DDR3 and Intel SMI link clock domains are fixed in a 1:2:12 ratio. The JTAG and SMBus asynchronous subsystems need not scale. The clock frequencies and ratios supported by Intel 7500/7510/7512 Scalable Memory Buffer are shown in Table 2-9.

Table 2-9. Intel 7500/7510/7512 Scalable Memory Buffer Clock Ratios

Intel SMI Link Data Rate	DDR3 Data Rate	Core Frequency	Ref Clk: Core	Intel SMI Link: Core	Core: DDR3
4.8 Gb/s	800 MT/s	400 MHz	1: 3	12: 1	1: 2
5.87 Gb/s	978 MT/s	489 MHz	1: 3.67	12: 1	1: 2
6.4 Gb/s	1066 MT/s	533 MHz	1: 4	12: 1	1: 2

2.4 DDR3 Signaling Specifications

This section defines the DDR3 signalling specification. This includes DDR3 800, 987 and 1067 MHz frequencies.

2.4.1 DC and AC Characteristics

Table 2-10. DDR3 and DDR3L Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage			0.43*V_{DDQ}	V	2
V_{IH}	Input High Voltage	0.57*V_{DDQ}			V	3,4
V_{OL}	Output Low Voltage		(V_{DDQ} / 2)* (R_{ON} /(R_{ON}+R_{VTT_TERM}))		V	6
V_{OH}	Output High Voltage		V_{DDQ} - ((V_{DDQ} / 2)* (R_{ON}/(R_{ON}+R_{VTT_TERM}))		V	4,6
R_{ON}	DDR3 Clock Buffer On Resistance	21		31	Ω	5
R_{ON}	DDR3 Command Buffer On Resistance	16		24	Ω	5
R_{ON}	DDR3 Control Buffer On Resistance	21		31	Ω	5
R_{ON}	DDR3 Data Buffer On Resistance	21		31	Ω	5
R_{ON}	DDR3 Reset Buffer On Resistance	30		75	Ω	5
Data ODT	On-Die Termination for Data Signals	45 90		55 110	Ω	7
ParErr ODT	On-Die Termination for Parity Error bits	60		80	Ω	7, 8
I_{LI}	Input Leakage Current	N/A	N/A	± 200	uA	

Notes:
1. Unless otherwise noted, all specifications in this table apply to all Intel 7500/7510/7512 Scalable Memory Buffer frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. VIH and VOH may experience excursions above VDDQ. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance.
6. R_{VTT_TERM} is the termination on the DIMM and is not controlled by Intel 7500/7510/7512 Scalable Memory Buffer.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the 2 sets.
8. On Intel 7510/7512 Scalable Memory Buffer, the ParErr ODT values are Min=55;Max75.

Table 2-11. DDR3 Electrical Characteristics and AC Timings at 800 MHz, (V_{DDQ} = 1.5 V ± 0.075 V) (Sheet 1 of 2)

Symbol	Parameter	Channel 0 Channel 1		Unit	Note
		Max	Min		
Electrical Characteristics					
T_{SLR_D}	DQ[63:0], DQS[7:0], DQS#[7:0] Input Slew Rate	4.0	1.0	V/ns	2
System Memory Clock Timings					
T_{CK}	CLK Period	3.00	2.50	ns	
T_{CH}	CLK High Time	1.66	1.25	ns	
T_{CL}	CLK Low Time	1.66	1.25	ns	

Table 2-11. DDR3 Electrical Characteristics and AC Timings at 800 MHz, (V_{DDQ} = 1.5 V ± 0.075 V) (Sheet 2 of 2)

Symbol	Parameter	Channel 0 Channel 1		Unit	Note
		Max	Min		
T_{SKEW}	Intra-differential system memory clock pair (CLK_P/CLK_N)		+155	ps	
System Memory Command Signal Timings					
T_{CMD_CO}	RAS#, CAS#, WE#, MA[14:0], BA[2:0] Edge Placement Accuracy	+375	-375	ps	3,4,6
System Memory Control Signal Timings					
T_{CTRL_CO}	CS#[1:0], CKE[1:0], ODT[1:0] Edge Placement Accuracy	+375	-375	ps	3,6
System Memory Data and Strobe Signal Timings					
$T_{DVA} + T_{DVB}$	DQ[63:0] Valid before and after DQS[7:0] Rising or Falling Edge		0.67 * UI	UI	7
$T_{Su}+T_{HD}$	DQ Input Setup and Hold Time to DQS Rising or Falling Edge		0.25 * UI	ns	1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CLK Rising Edge Before Write Levelling	+375	-375	ns	3,6,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CLK Rising Edge after Write Levelling	+275	-275	ns	8
T_{WPRE}	DQS/DQS# Write Preamble Duration		2.379	ns	
T_{WPST}	DQS/DQS# Write Postamble Duration	1.371	1.129	ns	
T_{DQSS}	CLK rising edge output access time, where a write command is referenced, to the first DQS rising edge	C_{WL} x (T_{CK} + 4)		ns	5,6

Notes:

1. Unless otherwise noted, all specifications in this table apply to all Intel 7500 Scalable Memory Buffer frequencies.
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the tSU and tHD specifications must be increased by a derating factor. The input single ended slew rate is measured DC to AC levels; VIL_DC to VIH_AC for rising edges, and VIH_DC to VIL_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derating value. No derating is required for single ended slew rates equal to or greater than 1.0 V/ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital registers that allow independent timing adjustment of both the DDR reference clocks and DDR signals. The difference in delay between the signal and clock digital registers is accurate to within ±EPA. This EPA includes jitter, skew, within die variation and several other effects.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the Intel 7500 Scalable Memory Buffer pins are determined by the minimum Read DQS/DQS# delay.
5. C_{WL} (CAS Write Latency) is the delay, in clock cycles, between the rising edge of CLK where a write command is referenced and the first rising strobe edge where the first byte of write data is present. The C_{WL} value is determined by the value of the CWL (CAS Latency) setting.
6. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
7. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
8. This value specifies the parameter after write leveling, representing the residual error in the controller after training, and does not include any effects from the DRAM itself.

Table 2-12. DDR3 Electrical Characteristics and AC Timings at 1066 MHz

Symbol	Parameter	Channel 0 Channel 1		Unit	Figure	Note
		Max	Min			
Electrical Characteristics						
T_{SLR_D}	DQ[63:0], DQS[7:0], DQS#[7:0] Input Slew Rate	4.0	1.0	V/ns		2
System Memory Clock Timings						
T_{CK}	CLK Period	2.49	1.875	ns		
T_{CH}	CLK High Time	1.25	0.95	ns		
T_{CL}	CLK Low Time	1.25	0.95	ns		
T_{SKEW}	Intra-differential system memory clock pair (CLK_P/CLK_N) [not seen in C-spec]		+155	ps		
System Memory Command Signal Timings						
T_{CMD_CO}	RAS#, CAS#, WE#, MA[14:0], BA[2:0] Edge placement accuracy	+300	-300	ps		3,4,6
System Memory Control Signal Timings						
T_{CTRL_CO}	CS#[1:0], CKE[1:0], ODT[1:0] Edge placement accuracy	+300	-300	ps		3,6
System Memory Data and Strobe Signal Timings						
$T_{DVA} + T_{DVB}$	DQ[63:0] Valid before and after DQS[7:0] Rising or Falling Edge		0.67 * UI	UI		7
$T_{Su}+T_{HD}$	DQ Input Setup and Hold Time to DQS Rising or Falling Edge		0.25 * UI	ns		1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge before write levelling	+300	-300	ns		3,6,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge after write levelling	+206	-206	ns		8
T_{WPRE}	DQS/DQS# Write Preamble Duration		1.781	ns		
T_{WPST}	DQS/DQS# Write Postamble Duration	1.031	0.844	ns		
T_{DQSS}	CK Rising Edge Output Access Time, Where a Write Command Is Referenced, to the First DQS Rising Edge	C_{WL} x (T_{CK} + 4)		ns		5,6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all Intel 7500 Scalable Memory Buffer frequencies.
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the tSU and tHD specifications must be increased by a derating factor. The input single ended slew rate is measured DC to AC levels; VIL_DC to VIH_AC for rising edges, and VIH_DC to VIL_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derating value. No derating is required for single ended slew rates equal to or greater than 1.0 V/ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital registers that allow independent timing adjustment of both the DDR reference clocks and DDR signals. The difference in delay between the signal and clock digital registers is accurate to within ±EPA. This EPA includes jitter, skew, within die variation and several other effects.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the Intel 7500 Scalable Memory Buffer pins are determined with the minimum Read DQS/DQS# delay.
5. CWL (CAS Write Latency) is the delay, in clock cycles, between the rising edge of CK where a write command is referenced and the first rising strobe edge where the first byte of write data is present. The CWL value is determined by the value of the CWL (CAS Latency) setting.
6. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
7. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.

8. This value specifies the parameter after write leveling, representing the residual error in the controller after training, and does not include any effects from the DRAM itself.

2.5 SMBus, TAP, and other CMOS I/O

Note: Intel 7500/7510/7512 Scalable Memory Buffer does not provide a 3.3 V SMBus interface. It requires external voltage translation to connect to a 3.3 V SMBus.

Note: The TAP TDO signal (Open Drain CMOS Output) characteristics assume a 50 Ohm external pull up.

Table 2-13. Recommended Operating Conditions for SMBUS, TAP, and other CMOS I/O Pins

Symbol	Parameter	Min	Max	Unit	Comments
V_{OH}	Output High Voltage	0.75*VCC1P1		V	Nominal 50 Ohm Drive Setting (Not applicable for Open Drain)
V_{OL}	Output Low voltage		0.25*VCC1P1	V	Nominal 50 Ohm Drive Setting
I_{OH}	Output High Current	-4		mA	Nominal 50 Ohm Drive Setting (Not applicable for Open Drain)
I_{OL}	Output Low Current	4		mA	Nominal 50 Ohm Drive Setting
V_{IH}	Input High Voltage	0.65*VCC1P1		V	
V_{IL}	Input Low voltage		0.35*VCC1P1	V	
V_{HYST}	Hysteresis Voltage	10	30	mV	
$I_{LEAK-PIN}$	Input Leakage per device pin	-120	50	µA	
C_{PADI}	I/O Pin Capacitance		10	pF	

Table 2-14. SMBus Signal Group AC Timing Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes 1, 2
Transmitter and Receiver Timings						
F_{SMB}	SMBCLK Frequency	10	100	kHz		
TCK	SMBCLK Period	10	100	µs		
t_{LOW}	SMBCLK High Time	4		µs	2-1	
t_{HIGH}	SMBCLK Low Time	4.7		µs	2-1	
t_R	SMBus Rise Time		1	µs	2-1	3
t_F	SMBus Fall Time		0.3	µs	2-1	3
T_{AA}	SMBus Output Valid Delay	0.1	4.5	µs	2-1	
$t_{SU;DAT}$	SMBus Input Setup Time	250		ns	2-1	
$t_{HD;DAT}$	SMBus Input Hold Time	10		ns	2-1	
t_{BUF}	Bus Free Time between Stop and Start Condition	4.7		µs	2-1	4, 5
$t_{HD;STA}$	Hold Time after Repeated Start Condition	4.0		µs	2-1	
$t_{SU;STA}$	Repeated Start Condition Setup Time	4.7		µs	2-1	
$t_{SU;STD}$	Stop Condition Setup Time	4.0		µs	2-1	

Notes:
1. These parameters are based on design characterization and are not tested
2. All AC timings for the SMBus signals are referenced at VIL_MAX or VIL_MIN and measured at the Intel 7500/7510/7512 Scalable Memory Buffer pins. Refer to Figure 2-1.
3. Rise time is measured from (VIL_MAX - 0.15 V) to (VIH_MIN + 0.15 V). Fall time is measured from (0.9 * VCC33_SM) to (VIL_MAX - 0.15 V).

4. Minimum time allowed between request cycles.
5. Following a write transaction, an internal write cycle time of 10 ms must be allowed before starting the next transaction.

Figure 2-1. SMBus Timing Waveform

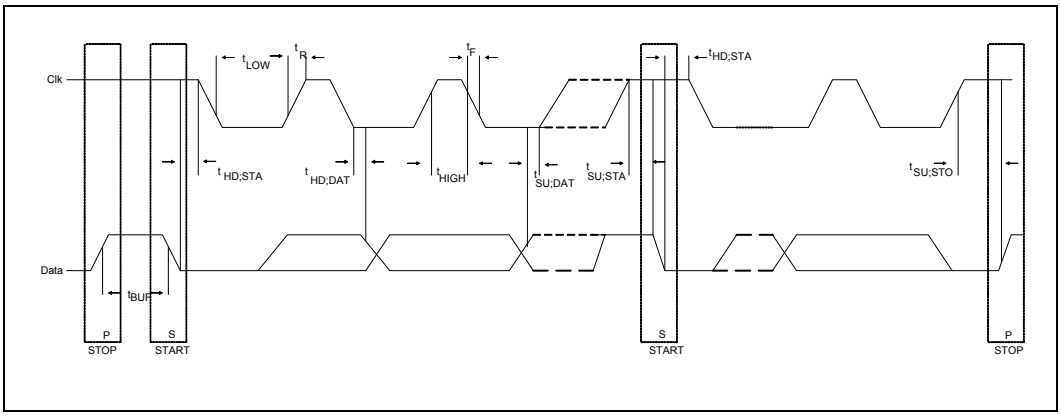
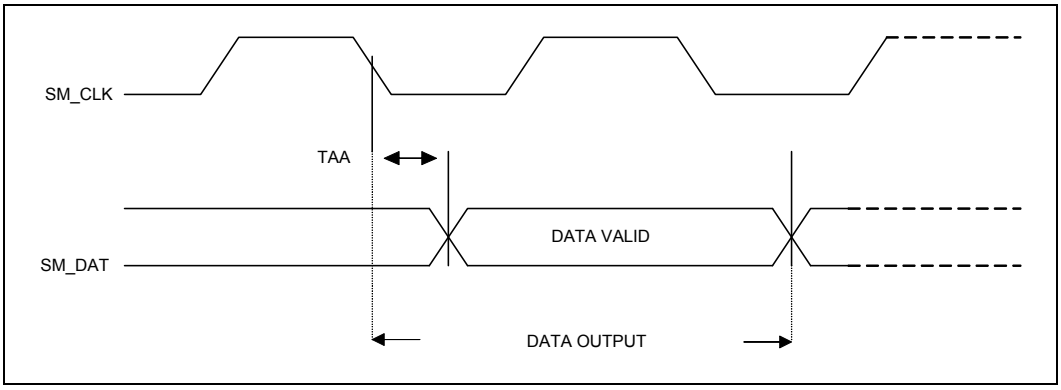


Figure 2-2. SMBus Valid Delay Timing Waveform



2.6 VCCPWRGOOD and VDDPWRGOOD

Table 2-15. VCCPWRGOOD and VDDPWRGOOD AC and DC Characteristics

Symbol	Parameter	Min	Max	Unit	Comments
V_{IH}	Input High Voltage	0.75*VCC1P1		V	
V_{IL}	Input Low voltage		0.25*VCC1P1	V	
V_{HYST}	Hysteresis Voltage	350	440	mV	
t_R	PWRGOOD Rise Time	10	100000	nS	
t_F	PWRGOOD Fall Time	10	100000	nS	
$I_{LEAK-PIN}$	Input Leakage per device pin	-120	5	µA	
C_{PADI}	I/O Pin Capacitance		7	pF	

2.7 RESET

Table 2-16. Recommended Operating Conditions for RST_N

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage	0.65*VCC1P1		V
V_{IL}	Input Low voltage		0.35*VCC1P1	V
V_{HYST}	Hysteresis Voltage	10	30	mV
t_R	RST_N Rise Time	1	30000	nS
t_F	RST_N Fall Time	1	30000	nS
$I_{LEAK-PIN}$	Input Leakage per device pin	-120	50	µA
C_{PADI}	I/O Pin Capacitance		10	pF

2.8 Intel 7500/7510/7512 Scalable Memory Buffer Overshoot/Undershoot Specifications

"Pulse duration" describes the total amount of time that an overshoot/undershoot event exceeds a reference voltage level. The total time could encompass several oscillations above or below the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 2-17 specifies the overshoot/undershoot parameters for different Intel 7500/7510/7512 Scalable Memory Buffer signal groups. This table assumes an Activity Factor (AF) of 0.12 for DDR3 and 0.25 for Intel SMI and MiscIO/TAP. For example, a 0.25 AF has one out of every four cycles with the worst case overshoot or undershoot for constant traffic during the entire life of the part.

The following Notes apply to ALL IO Signal Quality Specifications listed below:

1. The signal voltage must not exceed the absolute maximum Vcc and Vdd overshoot/undershoot voltage at any time (all voltages relative to Vss).
2. The pulse duration is defined as the total amount of time per data transaction (for data signals) or clock cycle (for clock signals) that the pulse overshoots the reference voltage or undershoots 0V (all voltage values are relative to Vss). See Figure 2-3.

Example of interpreting a row in the specification table:

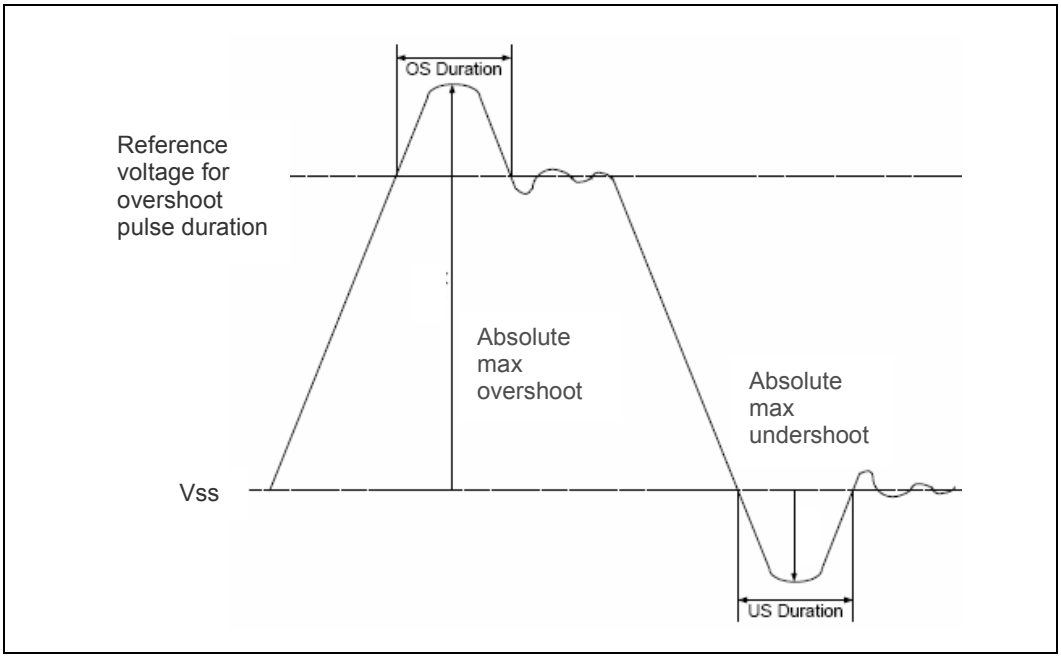
If the Absolute maximum overshoot is 1.8 V, the max pulse duration is 0.475 ns, and the overshoot reference voltage is 1.5 V, then the following is the interpretation: given that the data signal does not exceed 1.5 V for more than 0.475 ns during each data transaction, the max voltage of the signal must never exceed 1.8 V. In addition, if the activity factor is 0.25, only one out of every four cycles may have this worst case overshoot or undershoot with constant traffic for the entire life of the part.

Table 2-17. Intel 7500/7510/7512 Scalable Memory Buffer Overshoot/Undershoot Specifications

Signal Group	Maximum Overshoot	Overshoot Duration	Minimum Undershoot	Undershoot Duration
DDR3	1.2 * VDD1P5	0.5 * T_{CH}	-0.2 * VDD1P5	0.5 * T_{CH}
Intel SMI	1.2 * VCCFBD1P1	0.5 * T_{CH}	-0.2 * VCCFBD1P1	0.5 * T_{CH}
Misc IO and TAP	1.2 * VCC1P1	50 ns	-0.2 * VCC1P1	50 ns

Notes:
1. These specifications are measured at the device pin/pad.
2. Refer to Figure 2-3 for description of allowable Overshoot/Undershoot magnitude and duration.
3. T_{CH} refers to the Clock High Time as is specified in Section 2.4, "DDR3 Signaling Specifications"

Figure 2-3. Overshoot and Undershoot Durations



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3 Signal Lists

3.1 Conventions

The terms *assertion* and *de-assertion* are used extensively when describing signals, to avoid confusion when working with a mix of active-high and active-low signals. The term *assert*, or *assertion*, indicates that the signal is active, independent of whether the active level is represented by a high or low voltage. The term *de-assert*, or *de-assertion*, indicates that the signal is inactive.

Signal names may or may not use the suffix "_N". The "_N" suffix indicates that the active, or asserted state occurs when the signal is at a low voltage level. When the "_N" suffix is not present in the signal name the signal is asserted when at the high voltage level. **TRST_N** is an example of a signal that is asserted when at the low voltage level.

Differential pairs include "P" or "N" in the individual signal name to indicate the "positive" (P) signal in the pair or the "negative" (N) signal in the pair. **CLK133P and CLK133N** is an example of such a pair. When referring to the logic encoded by the differential pair of signals, sometimes the P/N notation will be dropped, e.g. **CLK133**.

Curly-bracketed numerical indices, for example, "{0/1}", represent DDR3 bus numbers (for example, **DDR{0/1}RAS_N**). Square-bracketed numerical indices, for example, "[3:0]" represent functionally similar but logically distinct bus signals; each signal provides an independent control, and may or may not be asserted at the same time as the other signals in the grouping. **DDR{0/1}CKE[3:0]** and **DDR{0/1}A[15:0]** are examples.

Typical frequencies of operation for the fastest operating modes are indicated. Test guard bands are not included. No frequency is mentioned for asynchronous or analog signals.

Table 3-1 summarizes the signal naming conventions used in this document**.**

Table 3-1. Signal Naming Conventions

Convention	Expands to
RR{0/1/2}XX	Expands to: RR0XX, RR1XX, and RR2XX. This denotes similar signals on separate buses.
RR[2:0]	Expands to: RR[2], RR[1], and RR[0]. This denotes a bus.
RR_N or RR_N[2:0]	Denotes an active low signal or bus.
RRN and RRP	Denotes a differential pair.

3.2 Intel 7500/7510/7512 Scalable Memory Buffer Component Pin Description List

Table 3-2. Pin Description (Sheet 1 of 3)

Signal	SignalType	Max Frequency	Description
Intel SMI Channel Interface			
FBDNBOP[13:0]	Intel SMI Output	6.4 GHz	**Northbound Output Data:** High speed serial signal. Read path from Intel 7500/7510/7512 Scalable Memory Buffer toward the host.
FBDNBON[13:0]	Intel SMI Output	6.4 GHz	**Northbound Output Data Complement**
FBDNBOCLKP	Intel SMI Output	6.4 GHz	Northbound Output Forwarded clock.
FBDNBOCLKN	Intel SMI Output	6.4 GHz	Northbound Output Forwarded clock Complement.
	Intel SMI Input	6.4 GHz	**Southbound Input Data:** High speed serial signal. Write path from host toward Intel 7500/7510/7512 Scalable Memory Buffer. FBDSBI{P/N}10 is the optional spare lane.
	Intel SMI Input	6.4 GHz	Southbound Input Data Complement.
FBDSBICLKP	Intel SMI Input	6.4 GHz	Southbound Input Forwarded clock.
FBDSBICLKN	Intel SMI Input	6.4 GHz	Southbound Input Forwarded clock Complement
FBDCDCMP	Analog		**External precision resistor for Tx/Rx termination calibration**. See Note 1 below.
DDR3 Buses 0/1			
DDR{0/1}DQ[63:0]	DDR3 I/O	1066 MHz	**Data**
DDR{0/1}CB[7:0]	DDR3 I/O	1066 MHz	**Check bits**
DDR{0/1}DQSP[7:0]	DDR3 I/O	1066 MHz	**Data Strobe:** x8 DRAM data strobes.
DDR{0/1}DQSN[7:0]	DDR3 I/O	1066 MHz	**Data Strobe Complement: x8** DRAM data strobe.
DDR{0/1}DQSP[8]	DDR3 I/O	1066 MHz	**Check-bit Strobe:** x8 DRAM check-bit strobes.
DDR{0/1}DQSN[8]	DDR3 I/O	1066 MHz	**Check-bit Strobe Complement: x8** DRAM check-bit strobe.
DDR{0/1}DQSP[16:9]	DDR3 I/O	1066 MHz	**Data Strobe:** DRAM data strobes for x4 devices.Not used for x8 devices.
DDR{0/1}DQSN[16:9]	DDR3 I/O	1066 MHz	**Data Strobe Complement:** DRAM data strobe complements for x4 devices. Not used for x8 devices.
DDR{0/1}DQSP[17]	DDR3 I/O	1066 MHz	**Check-bit Strobe:** DRAM check-bit strobe for x4 devices.Not used for x8 devices.
DDR{0/1}DQSN[17]	DDR3 I/O	1066 MHz	**Check-bit Strobe Complement:** DRAM check-bit strobe complements for x4 devices. Not used for x8 devices.
DDR{0/1}A[15:0]	DDR3 Output	1066 MHz	**Address:** Used for providing multiplexed row and column address to RDIMM.
DDR{0/1}BA[2:0]	DDR3 Output	1066 MHz	**Bank Active:** Used to select the bank within a rank.
DDR{0/1}RAS_N	DDR3 Output	1066 MHz	**Row Address Strobe:** Used with CS_N, CAS_N, and WE_N to specify the RDIMM command.
DDR{0/1}CAS_N	DDR3 Output	1066 MHz	**Column Address Strobe:** Used with CS_N, RAS_N, and WE_N to specify the RDIMM command.
DDR{0/1}WE_N	DDR3 Output	1066 MHz	**Write Enable:** Used with CS_N, CAS_N, and RAS_N to specify the RDIMM command.
DDR{0/1}CS_N[7:0]	DDR3 Output	1066 MHz	**Chip Select:** Used with CAS_N, RAS_N, and WE_N to specify the RDIMM command.
DDR{0/1}CKE[3:0]	DDR3 Output	1066 MHz	**Clock Enable:** DIMM Clock enable.

Table 3-2. Pin Description (Sheet 2 of 3)

Signal	SignalType	Max Frequency	Description
	DDR3 Output	533 MHz	**DIMM On-Die-Termination:** Dynamic ODT enables.
DDR{0/1}PAR	DDR3 Output	533 MHz	**Parity bit protecting A, BA, RAS_N, CAS_N, WE_N**.
	DDR3 Input	533 MHz	**Parity error detected signal from RDIMMs**.
DDR{0/1}EVENT_N	CMOS Input	Static	**Thermal Event detected signal from RDIMMs**. This signal is wire-or'ed, and driven by all RDIMMs. ***Note:*** This input pin is part of the MISC I/O block, and should be pulled up to 1.1 V.
DDR{0/1}RESET_N	DDR3 Output	Static	**DIMM Reset**. This signals drives the RESET_N inputs of the RDIMMs. RESET_N is asynchronous. It is unterminated to prevent current flow during suspend to RAM, when it must be driven while other signals are driven low.
	DDR3 Output	533 MHz	**Clock:** Clocks to RDIMMs.
	DDR3 Output	533 MHz	**Clock Complement:** Clocks to RDIMMs.
DDR Compensation			
DDRCOMP[2:0]	Analog		Analog Compensation
Clocking			
CLK133P	Reference Clock Input	133 MHz	Intel 7500/7510/7512 Scalable Memory Buffer Clock: This is one of the two differential reference clock inputs to the Phase Locked Loop in the Intel 7500/7510/7512 Scalable Memory Buffer core. Phase Locked Loops in the Intel 7500/7510/7512 Scalable Memory Buffer will shift this to all frequencies required by the core, DDR buses, and Intel SMI Channel.
CLK133N	Reference Clock Input	133 MHz	Intel 7500/7510/7512 Scalable Memory Buffer Clock Complement: This is the other differential reference clock input to the Phase Locked Loop in the Intel 7500/7510/7512 Scalable Memory Buffer core. Phase Locked Loops in the Intel 7500/7510/7512 Scalable Memory Buffer will shift this to all frequencies required by the core, DDR buses, and Intel SMI Channel.
System Management			
SCL	Open Drain CMOS Input	100 KHz	SMBus Clock
SDA	Open Drain CMOS I/O	100 KHz	SMBus Address/Data
SA0	CMOS Input	Static	SMBus Select ID
Reset			
VDDPWRGOOD	VDDPWRGOOD	Static	Power Good indication for VDD voltage
VCCPWRGOOD	VCCPWRGOOD	Static	Power Good indication for VCC voltage
RST_N	Reset	Static	Asynchronous Reset
LAI Interface			
LAIMODE_N	CMOS Input	Static	LAI Mode Input. Should be pulled high for normal system usage.
LAISCL	Open Drain CMOS Input	100 KHz	LAI SMBus Clock
LAISDA	Open Drain CMOS I/O	100 KHz	LAI SMBus Address/Data
Test Access Port (JTAG)			
TCK	Open Drain CMOS Input	50 MHz	**JTAG Test Clock:** Clock input used to drive Test Access Port (TAP) state machine during test and debugging. This input may change asynchronous to CLK133.

Table 3-2. Pin Description (Sheet 3 of 3)

Signal	SignalType	Max Frequency	Description
TDI	Open Drain CMOS Input	50 MHz	**JTAG Test Data In:** Data input for test mode. Used to serially shift data and instructions into TAP.
TDO	TDO (Open Drain CMOS Output)	50 MHz	**JTAG Test Data Out:** Data: Data output for test mode. Used to serially shift data out of the device.
TMS	Open Drain CMOS Input	50 MHz	**JTAG Test Mode Select:** This signal is used to control the state of the TAP controller.
TRST_N	Open Drain CMOS Input	50 MHz	**JTAG Test Reset:** This signal resets the TAP controller logic. It should be pulled down unless TCK is active. This input may change asynchronous to CLK133.
Power Supplies			
VCC1P1 (multiple pins)			Nominal 1.1 V supply for core logic.
VCCTTA1P1 (multiple pins)			Nominal 1.1 V supply for analog DDR3 logic.
VCCFBD1P1 (multiple pins)			Nominal 1.1 V supply for analog Intel SMI high speed I/O
VREG1P8			1.8 V nominal supply for the on-die regulator that supplies the PLL.
VDD1P5 (multiple pins)			1.5 V nominal supply for DDR I/O
VSS (multiple pins)			Ground
Other Pins			
RSVD_MBID	NC		Reserved pin in Intel 7500/7510/7512 Scalable Memory Buffer. Unconnected in package. Was defined as MBID in previous revisions, but functionality will not be implemented.
RSVD (multiple pins)	NC		Reserved pins. Must be floated (NC).

Notes:
1. FBDCDCMP should be connected to VSS (ground) through an external 21 W (1% tolerance) resistor. Resistor power rating to be 1/10 W to 1/16 W.

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4 Ballout and Package

4.1 Ballout Overview

The Intel 7500/7510/7512 Scalable Memory Buffers have the same ballout and pin allocation; it's the different board connectivity requirements of certain package pins that distinguishes the Intel 7512 Scalable Memory Buffer from the other two.

Section 4.2 describes the ballout for the Intel 7500/7510 Scalable Memory Buffer where a single VR is used to generate VCC1P1 and VCCFBD1P1 rail.

Section 4.4 describes the required changes starting from Section 4.2, to implement a split rail solution which is a requirement to support the Intel 7512 Scalable Memory Buffer, that is, one VR is used to generate VCC1P1 and a second VR is used to generate the VCCFBD1P1 rail.

4.2 Intel 7500/7510 Scalable Memory Buffer Pin Assignments (Non-split Rail Implementation)

Figure 4-1, Figure 4-2 and Figure 4-3 show the pin assignments for the Intel 7500/7510 Scalable Memory Buffer component. This ballout is applicable for the non-split rail implementation.

Table 4-1. Intel 7500/7510 Scalable Memory Buffer Ball Assignments - Left

	1	2	3	4	5	6	7	8	9	10	11
A			VDD1P5	DDR0CS_N[7]	DDR0ODT[3]	DDR0ODT[2]	VSS	DDR0CAS_N	DDR0RAS_N	DDR0BA[0]	DDR0A[10]
B		VSS	DDR0DQ[37]	DDR0DQ[36]	VSS	DDR0ODT[1]	DDR0CS_N[4]	DDR0A[13]	DDR0WE_N	VDD1P5	DDR0BA[1]
C	VDD1P5777	DDR0DQSP[13]	DDR0DQ[33]	DDR0CS_N[2]	DDR0CS_N[3]	DDR0CS_N[5]	DDR0CS_N[1]	VDD1P5	DDR0CS_N[0]	DDR1RAS_N	DDR1BA[1]
D	DDR0DQSN[13]	DDR0DQSN[4]	VSS	DDR0DQ[32]	DDR0CS_N[6]	VDD1P5	DDR0ODT[0]	DDR1ODT[2]	DDR1CS_N[4]	DDR1WE_N	VSS
E	DDR0DQSP[4]	VSS	DDR0DQ[38]	DDR0DQ[35]	DDR1CS_N[2]	DDR1CS_N[3]	DDR1ODT[3]	DDR1CS_N[5]	VSS	DDR1CAS_N	DDR1BA[0]
F	VSS	DDR0DQ[39]	DDR0DQ[34]	VSS	DDR1DQ[37]	DDR1CS_N[7]	VSS	DDR1CS_N[1]	DDR1ODT[0]	DDR1A[13]	DDR1EVENT_N
G	DDR0DQ[45]	DDR0DQ[44]	VSS	DDR1DQ[33]	DDR1DQ[32]	DDR1CS_N[6]	DDR1ODT[1]	DDR1CS_N[0]	DDRCOMP[0]	VDD1P5	DDRCOMP[2]
H	DDR0DQ[41]	VSS	DDR0DQ[40]	DDR1DQSN[13]	VSS	DDR1DQSP[13]	DDR1DQ[36]	VSS	DDRCOMP[1]	NC	TDO
J	VSS	DDR0DQSP[14]	DDR1DQSP[4]	VDD1P5	DDR1DQSN[4]	DDR1DQ[38]	VDD1P5	DDR1DQ[34]	VSS	VSS	NC
K	DDR0DQSN[14]	DDR0DQSN[5]	VSS	DDR1DQSN[5]	DDR1DQ[39]	VSS	DDR1DQ[40]	DDR1DQ[35]	VDD1P5	VDDPWRGOOD	TMS
L	DDR0DQSP[5]	VSS	DDR0DQ[46]	DDR1DQSP[5]	VSS	DDR1DQSN[14]	DDR1DQSP[14]	VSS	DDR1DQ[44]	VCCPWRGOOD	TDI
M	VDD1P5	DDR0DQ[47]	DDR1DQ[42]	VSS	DDR1DQ[47]	DDR1DQ[46]	VSS	DDR1DQ[41]	DDR1DQ[45]	VSS	TCK
N	DDR0DQ[42]	DDR0DQ[43]	VDD1P5	DDR1DQ[48]	DDR1DQ[53]	VDD1P5	DDR1DQ[52]	DDR1DQ[43]	VSS	NC	NC
P	DDR0DQ[48]	VSS	DDR0DQ[53]	DDR1DQ[49]	VSS	DDR1DQSP[15]	DDR1DQ[54]	VSS	DDR1DQ[55]	CLK133P	CLK133N
R	VSS	DDR0DQSP[15]	DDR0DQ[49]	VSS	DDR1DQSN[6]	DDR1DQSN[15]	VDD1P5	DDR1DQ[50]	DDR1DQ[51]	VSS	FBDCDCMP
T	DDR0DQSN[15]	DDR0DQSN[6]	VDD1P5	DDR0DQ[52]	DDR1DQSP[6]	VSS	DDR1DQ[61]	DDR1DQ[60]	VDD1P5	NC	NC
U	DDR0DQSP[6]	VSS	DDR0DQ[54]	DDR0DQ[51]	VSS	DDR1DQ[57]	DDR1DQ[56]	VSS	MB1_ID	NC	NC
V	VSS	DDR0DQ[55]	DDR0DQ[50]	VDD1P5	DDR1DQSP[16]	DDR1DQSN[16]	DDR1DQ[63]	NC	FBDSBIP[1]	VCCFBD1P1	NC
W	DDR0DQ[60]	DDR0DQ[61]	VSS	DDR1DQSN[7]	DDR1DQSP[7]	DDR1DQ[59]	VSS	FBDSBIP[0]	FBDSBIN[1]	FBDSBIN[2]	NC
Y	DDR0DQ[56]	VSS	DDR0DQ[57]	DDR1DQ[62]	VSS	DDR1DQ[58]	VDD1P5	FBDSBIN[0]	VSS	FBDSBIP[2]	VSS
AA	VDD1P5	DDR0DQSP[16]	DDR0DQSN[16]	VSS	DDR0DQ[62]	VSS	FBDNBOP[0]	VSS	FBDNBOP[2]	VSS	FBDNBOP[4]
AB		VSS	DDR0DQSN[7]	DDR0DQSP[7]	DDR0DQ[58]	NC	FBDNBON[0]	FBDNBOP[1]	FBDNBON[2]	FBDNBOP[3]	FBDNBON[4]
AC			VDD1P5	DDR0DQ[63]	DDR0DQ[59]	VSS	VSS	FBDNBON[1]	VSS	FBDNBON[3]	VSS
	1	2	3	4	5	6	7	8	9	10	11

Table 4-2. Intel 7500/7510 Scalable Memory Buffer Ball Assignment - Middle

	12	13	14	15	16	17	18	19	20	21
A	VDD1P5	DDR0EVENT_N	NC	DDR0A[2]	DDR0A[1]	VSS	DDR0A[5]	DDR0A[8]	DDR0A[11]	DDR0A[9]
B	DDR0A[0]	DDR0PAR	NC	VSS	DDR0A[3]	DDR0A[4]	DDR0A[6]	DDR0A[7]	VDD1P5	DDR0A[12]
C	DDR1A[10]	VSS	DDR0CLKP[1]	NC	NC	NC	NC	VDD1P5	DDR0ERR_N[0]	DDR0ERR_N[1]
D	DDR1A[0]	DDR0CLKP[0]	DDR0CLKN[1]	NC	VDD1P5	DDR1CLKP[1]	DDR1CLKN[1]	DDR1A[8]	NC	VSS
E	DDR1PAR	DDR0CLKN[0]	VDD1P5	NC	DDR1A[3]	DDR1A[4]	DDR1A[5]	VSS	DDR1A[11]	DDR1A[9]
F	VDD1P5	DDR1CLKN[0]	DDR1CLKP[0]	DDR1A[2]	DDR1A[1]	VSS	DDR1A[6]	DDR1A[7]	NC	DDR1A[15]
G	VSS	NC	NC	NC	NC	DDR1ERR_N[0]	DDR1ERR_N[1]	DDR1CKE[0]	VSS	VDD1P5
H	TRST_N	NC	NC	LAIMODE_N	LAISDA	LAISCL	SA0	VSS	DDR1DQ[27]	DDR1DQ[31]
J	VSS	NC	VSS	NC	VSS	VCC1P1	VSS	RST_N	DDR1DQ[26]	DDR1DQSP[3]
K	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	SDA	DDR1DQSN[3]	VSS
L	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	SCL	VSS	DDR1DQ[17]
M	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	LAIEV[2]	DDR1DQ[21]	DDR1DQ[16]
N	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	LAIEV[1]	DDR1DQ[20]	VSS
P	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	LAIEV[0]	VSS	DDR1DQ[8]
R	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	LAIEV[3]	DDR1DQ[12]	DDR1DQ[9]
T	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	NC	DDR1DQ[13]	DDR1DQ[3]
U	VSS	VCC1P1	VSS	VCC1P1	VSS	VCC1P1	VSS	VCCFBD1P1	NC	VSS
V	VCCFBD1P1	FBDSBIP[4]	VCCFBD1P1	FBDSBIP[9]	VCCFBD1P1	FBDSBIN[6]	VCCFBD1P1	NC	VSS	FBDSBIN[10]
W	FBDSBIN[3]	FBDSBIN[4]	FBDSBICLKN	FBDSBIN[9]	FBDSBIP[5]	FBDSBIP[6]	FBDSBIN[7]	NC	FBDSBIP[8]	FBDSBIP[10]
Y	FBDSBIP[3]	VSS	FBDSBICLKP	VSS	FBDSBIN[5]	VSS	FBDSBIP[7]	VSS	FBDSBIN[8]	VSS
AA	VSS	FBDNBOP[13]	VSS	FBDNBON[12]	VSS	FBDNBON[7]	VSS	FBDNBON[9]	VSS	NC
AB	FBDNBOP[5]	FBDNBON[13]	FBDNBOCLKP	FBDNBOP[12]	FBDNBON[6]	FBDNBOP[7]	FBDNBON[8]	FBDNBOP[9]	FBDNBON[10]	NC
AC	FBDNBON[5]	VSS	FBDNBOCLKN	VSS	FBDNBOP[6]	VSS	FBDNBOP[8]	VSS	FBDNBOP[10]	VSS
	12	13	14	15	16	17	18	19	20	21

Table 4-3. Intel 7500/7510 Scalable Memory Buffer Ball Assignment - Right

22	23	24	25	26	27	28	29	
VDD1P5	DDR0A[14]	DDR0CKE[3]	DDR0RESET_N	DDR0CB[3]	VSS			A
DDR0BA[2]	DDR0A[15]	DDR0CKE[1]	VSS	DDR0CB[2]	DDR0CB[7]	VDD1P5		B
DDR0CKE[0]	VSS	DDR0CKE[2]	DDR1CB[3]	VDD1P5	DDR1CB[7]	DDR0CB[6]	VSS	C
DDR1A[12]	DDR1BA[2]	DDR1RESET_N	DDR1CB[2]	DDR1CB[6]	VSS	DDR0DQSP[8]	DDR0DQSN[8]	D
DDR1A[14]	VDD1P5	DDR1DQSP[8]	DDR1DQSN[8]	VSS	DDR0DQSN[17]	DDR0DQSP[17]	VSS	E
DDR1CKE[3]	DDR1CKE[2]	DDR1DQSP[17]	VDD1P5	DDR1DQSN[17]	DDR0DQ[27]	VSS	DDR0CB[1]	F
DDR1CKE[1]	DDR1CB[0]	VSS	DDR1CB[1]	DDR0DQ[26]	VSS	DDR0CB[0]	DDR0CB[5]	G
DDR1DQ[30]	VSS	DDR1CB[4]	DDR1CB[5]	VSS	DDR0DQ[30]	DDR0CB[4]	VDD1P5	H
VDD1P5	DDR1DQSP[12]	DDR1DQSN[12]	VDD1P5	DDR0DQ[31]	DDR0DQSP[3]	VSS	DDR0DQSN[3]	J
DDR1DQ[28]	DDR1DQ[29]	VSS	DDR1DQ[25]	DDR0DQ[25]	VSS	DDR0DQSN[12]	DDR0DQSP[12]	K
DDR1DQSP[2]	VSS	DDR1DQ[19]	DDR1DQ[24]	VDD1P5	DDR0DQ[29]	DDR0DQ[24]	VSS	L
VDD1P5	DDR1DQSN[2]	DDR1DQ[18]	VSS	DDR0DQ[28]	DDR0DQ[19]	VSS	DDR0DQ[18]	M
DDR1DQSP[11]	DDR1DQSN[11]	VSS	DDR1DQ[23]	DDR1DQ[22]	VSS	DDR0DQ[23]	DDR0DQ[22]	N
DDR1DQSN[10]	VSS	DDR1DQ[11]	DDR1DQ[10]	VSS	DDR0DQSP[2]	DDR0DQSN[2]	VSS	P
VDD1P5	DDR1DQSN[1]	DDR1DQSP[1]	VDD1P5	DDR1DQ[14]	DDR1DQ[15]	VSS	DDR0DQSN[11]	R
DDR1DQSP[10]	DDR1DQ[2]	VSS	DDR0DQ[11]	DDR0DQ[10]	VSS	DDR0DQSP[11]	DDR0DQ[17]	T
DDR1DQ[7]	DDR1DQSP[0]	DDR1DQ[6]	DDR0DQ[15]	VDD1P5	DDR0DQ[16]	DDR0DQ[21]	VDD1P5	U
VSS	DDR1DQSN[9]	DDR1DQSN[0]	VSS	DDR0DQ[14]	DDR0DQSP[1]	VSS	DDR0DQ[20]	V
VSS	DDR1DQSP[9]	VDD1P5	DDR0DQ[13]	DDR0DQ[8]	VSS	DDR0DQSN[1]	DDR0DQSN[10]	W
DDR1DQ[5]	DDR1DQ[0]	DDR1DQ[1]	DDR0DQ[12]	VSS	DDR0DQ[3]	DDR0DQSP[10]	DDR0DQ[9]	Y
VSS	DDR1DQ[4]	DDR0DQ[0]	VSS	DDR0DQSP[0]	DDR0DQ[7]	DDR0DQ[2]	VSS	AA
FBDNBON[11]	VSS	DDR0DQ[4]	DDR0DQSP[9]	DDR0DQSN[0]	DDR0DQ[6]	VDD1P5		AB
FBDNBOP[11]	VREG1P8	DDR0DQ[5]	DDR0DQ[1]	DDR0DQSN[9]	VSS			AC
22	23	24	25	26	27	28	29	

Table 4-4. Intel 7500/7510/7512 Scalable Memory Buffer Signals by Ball Number (Sheet 1 of 6)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A1	----	B1	----	C1	VDD1P5
A2	----	B2	VSS	C2	DDR0DQSP[13]
A3	VDD1P5	B3	DDR0DQ[37]	C3	DDR0DQ[33]
A4	DDR0CS_N[7]	B4	DDR0DQ[36]	C4	DDR0CS_N[2]
A5	DDR0ODT[3]	B5	VSS	C5	DDR0CS_N[3]
A6	DDR0ODT[2]	B6	DDR0ODT[1]	C6	DDR0CS_N[5]
A7	VSS	B7	DDR0CS_N[4]	C7	DDR0CS_N[1]
A8	DDR0CAS_N	B8	DDR0A[13]	C8	VDD1P5
A9	DDR0RAS_N	B9	DDR0WE_N	C9	DDR0CS_N[0]
A10	DDR0BA[0]	B10	VDD1P5	C10	DDR1RAS_N
A11	DDR0A[10]	B11	DDR0BA[1]	C11	DDR1BA[1]
A12	VDD1P5	B12	DDR0A[0]	C12	DDR1A[10]
A13	DDR0EVENT_N	B13	DDR0PAR	C13	VSS
A14	NC	B14	NC	C14	DDR0CLKP[1]
A15	DDR0A[2]	B15	VSS	C15	NC
A16	DDR0A[1]	B16	DDR0A[3]	C16	NC
A17	VSS	B17	DDR0A[4]	C17	NC
A18	DDR0A[5]	B18	DDR0A[6]	C18	NC
A19	DDR0A[8]	B19	DDR0A[7]	C19	VDD1P5
A20	DDR0A[11]	B20	VDD1P5	C20	DDR0ERR_N[0]
A21	DDR0A[9]	B21	DDR0A[12]	C21	DDR0ERR_N[1]
A22	VDD1P5	B22	DDR0BA[2]	C22	DDR0CKE[0]
A23	DDR0A[14]	B23	DDR0A[15]	C23	VSS
A24	DDR0CKE[3]	B24	DDR0CKE[1]	C24	DDR0CKE[2]
A25	DDR0RESET_N	B25	VSS	C25	DDR1CB[3]
A26	DDR0CB[3]	B26	DDR0CB[2]	C26	VDD1P5
A27	VSS	B27	DDR0CB[7]	C27	DDR1CB[7]
A28	----	B28	VDD1P5	C28	DDR0CB[6]
A29	----	B29	----	C29	VSS
D1	DDR0DQSN[13]	E1	DDR0DQSP[4]	F1	VSS
D2	DDR0DQSN[4]	E2	VSS	F2	DDR0DQ[39]
D3	VSS	E3	DDR0DQ[38]	F3	DDR0DQ[34]
D4	DDR0DQ[32]	E4	DDR0DQ[35]	F4	VSS
D5	DDR0CS_N[6]	E5	DDR1CS_N[2]	F5	DDR1DQ[37]
D6	VDD1P5	E6	DDR1CS_N[3]	F6	DDR1CS_N[7]
D7	DDR0ODT[0]	E7	DDR1ODT[3]	F7	VSS
D8	DDR1ODT[2]	E8	DDR1CS_N[5]	F8	DDR1CS_N[1]
D9	DDR1CS_N[4]	E9	VSS	F9	DDR1ODT[0]
D10	DDR1WE_N	E10	DDR1CAS_N	F10	DDR1A[13]
D11	VSS	E11	DDR1BA[0]	F11	DDR1EVENT_N

Table 4-4. Intel 7500/7510/7512 Scalable Memory Buffer Signals by Ball Number (Sheet 2 of 6)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
D12	DDR1A[0]	E12	DDR1PAR	F12	VDD1P5
D13	DDR0CLKP[0]	E13	DDR0CLKN[0]	F13	DDR1CLKN[0]
D14	DDR0CLKN[1]	E14	VDD1P5	F14	DDR1CLKP[0]
D15	NC	E15	NC	F15	DDR1A[2]
D16	VDD1P5	E16	DDR1A[3]	F16	DDR1A[1]
D17	DDR1CLKP[1]	E17	DDR1A[4]	F17	VSS
D18	DDR1CLKN[1]	E18	DDR1A[5]	F18	DDR1A[6]
D19	DDR1A[8]	E19	VSS	F19	DDR1A[7]
D20	NC	E20	DDR1A[11]	F20	NC
D21	VSS	E21	DDR1A[9]	F21	DDR1A[15]
D22	DDR1A[12]	E22	DDR1A[14]	F22	DDR1CKE[3]
D23	DDR1BA[2]	E23	VDD1P5	F23	DDR1CKE[2]
D24	DDR1RESET_N	E24	DDR1DQSP[8]	F24	DDR1DQSP[17]
D25	DDR1CB[2]	E25	DDR1DQSN[8]	F25	VDD1P5
D26	DDR1CB[6]	E26	VSS	F26	DDR1DQSN[17]
D27	VSS	E27	DDR0DQSN[17]	F27	DDR0DQ[27]
D28	DDR0DQSP[8]	E28	DDR0DQSP[17]	F28	VSS
D29	DDR0DQSN[8]	E29	VSS	F29	DDR0CB[1]
Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
G1	DDR0DQ[45]	H1	DDR0DQ[41]	J1	VSS
G2	DDR0DQ[44]	H2	VSS	J2	DDR0DQSP[14]
G3	VSS	H3	DDR0DQ[40]	J3	DDR1DQSP[4]
G4	DDR1DQ[33]	H4	DDR1DQSN[13]	J4	VDD1P5
G5	DDR1DQ[32]	H5	VSS	J5	DDR1DQSN[4]
G6	DDR1CS_N[6]	H6	DDR1DQSP[13]	J6	DDR1DQ[38]
G7	DDR1ODT[1]	H7	DDR1DQ[36]	J7	VDD1P5
G8	DDR1CS_N[0]	H8	VSS	J8	DDR1DQ[34]
G9	DDRCOMP[0]	H9	DDRCOMP[1]	J9	VSS
G10	VDD1P5	H10	NC	J10	VSS
G11	DDRCOMP[2]	H11	TDO	J11	NC
G12	VSS	H12	TRST_N	J12	VSS
G13	NC	H13	NC	J13	NC
G14	NC	H14	NC	J14	VSS
G15	NC	H15	LAIMODE_N	J15	NC
G16	NC	H16	LAISDA	J16	VSS
G17	DDR1ERR_N[0]	H17	LAISCL	J17	VCC1P1
G18	DDR1ERR_N[1]	H18	SA0	J18	VSS
G19	DDR1CKE[0]	H19	VSS	J19	RST_N
G20	VSS	H20	DDR1DQ[27]	J20	DDR1DQ[26]
G21	VDD1P5	H21	DDR1DQ[31]	J21	DDR1DQSP[3]
G22	DDR1CKE[1]	H22	DDR1DQ[30]	J22	VDD1P5

Table 4-4. Intel 7500/7510/7512 Scalable Memory Buffer Signals by Ball Number (Sheet 3 of 6)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
G23	DDR1CB[0]	H23	VSS	J23	DDR1DQSP[12]
G24	VSS	H24	DDR1CB[4]	J24	DDR1DQSN[12]
G25	DDR1CB[1]	H25	DDR1CB[5]	J25	VDD1P5
G26	DDR0DQ[26]	H26	VSS	J26	DDR0DQ[31]
G27	VSS	H27	DDR0DQ[30]	J27	DDR0DQSP[3]
G28	DDR0CB[0]	H28	DDR0CB[4]	J28	VSS
G29	DDR0CB[5]	H29	VDD1P5	J29	DDR0DQSN[3]
Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
K1	DDR0DQSN[14]	L1	DDR0DQSP[5]	M1	VDD1P5
K2	DDR0DQSN[5]	L2	VSS	M2	DDR0DQ[47]
K3	VSS	L3	DDR0DQ[46]	M3	DDR1DQ[42]
K4	DDR1DQSN[5]	L4	DDR1DQSP[5]	M4	VSS
K5	DDR1DQ[39]	L5	VSS	M5	DDR1DQ[47]
K6	VSS	L6	DDR1DQSN[14]	M6	DDR1DQ[46]
K7	DDR1DQ[40]	L7	DDR1DQSP[14]	M7	VSS
K8	DDR1DQ[35]	L8	VSS	M8	DDR1DQ[41]
K9	VDD1P5	L9	DDR1DQ[44]	M9	DDR1DQ[45]
K10	VDDPWRGOOD	L10	VCCPWRGOOD	M10	VSS
K11	TMS	L11	TDI	M11	TCK
K12	VCC1P1	L12	VSS	M12	VCC1P1
K13	VSS	L13	VCC1P1	M13	VSS
K14	VCC1P1	L14	VSS	M14	VCC1P1
K15	VSS	L15	VCC1P1	M15	VSS
K16	VCC1P1	L16	VSS	M16	VCC1P1
K17	VSS	L17	VCC1P1	M17	VSS
K18	VCC1P1	L18	VSS	M18	VCC1P1
K19	SDA	L19	SCL	M19	LAIEV[2]
K20	DDR1DQSN[3]	L20	VSS	M20	DDR1DQ[21]
K21	VSS	L21	DDR1DQ[17]	M21	DDR1DQ[16]
K22	DDR1DQ[28]	L22	DDR1DQSP[2]	M22	VDD1P5
K23	DDR1DQ[29]	L23	VSS	M23	DDR1DQSN[2]
K24	VSS	L24	DDR1DQ[19]	M24	DDR1DQ[18]
K25	DDR1DQ[25]	L25	DDR1DQ[24]	M25	VSS
K26	DDR0DQ[25]	L26	VDD1P5	M26	DDR0DQ[28]
K27	VSS	L27	DDR0DQ[29]	M27	DDR0DQ[19]
K28	DDR0DQSN[12]	L28	DDR0DQ[24]	M28	VSS
K29	DDR0DQSP[12]	L29	VSS	M29	DDR0DQ[18]
Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
N1	DDR0DQ[42]	P1	DDR0DQ[48]	R1	VSS
N2	DDR0DQ[43]	P2	VSS	R2	DDR0DQSP[15]
N3	VDD1P5	P3	DDR0DQ[53]	R3	DDR0DQ[49]

Table 4-4. Intel 7500/7510/7512 Scalable Memory Buffer Signals by Ball Number (Sheet 4 of 6)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
N4	DDR1DQ[48]	P4	DDR1DQ[49]	R4	VSS
N5	DDR1DQ[53]	P5	VSS	R5	DDR1DQSN[6]
N6	VDD1P5	P6	DDR1DQSP[15]	R6	DDR1DQSN[15]
N7	DDR1DQ[52]	P7	DDR1DQ[54]	R7	VDD1P5
N8	DDR1DQ[43]	P8	VSS	R8	DDR1DQ[50]
N9	VSS	P9	DDR1DQ[55]	R9	DDR1DQ[51]
N10	NC	P10	CLK133P	R10	VSS
N11	NC	P11	CLK133N	R11	FBDCDCMP
N12	VSS	P12	VCC1P1	R12	VSS
N13	VCC1P1	P13	VSS	R13	VCC1P1
N14	VSS	P14	VCC1P1	R14	VSS
N15	VCC1P1	P15	VSS	R15	VCC1P1
N16	VSS	P16	VCC1P1	R16	VSS
N17	VCC1P1	P17	VSS	R17	VCC1P1
N18	VSS	P18	VCC1P1	R18	VSS
N19	LAIEV[1]	P19	LAIEV[0]	R19	LAIEV[3]
N20	DDR1DQ[20]	P20	VSS	R20	DDR1DQ[12]
N21	VSS	P21	DDR1DQ[8]	R21	DDR1DQ[9]
N22	DDR1DQSP[11]	P22	DDR1DQSN[10]	R22	VDD1P5
N23	DDR1DQSN[11]	P23	VSS	R23	DDR1DQSN[1]
N24	VSS	P24	DDR1DQ[11]	R24	DDR1DQSP[1]
N25	DDR1DQ[23]	P25	DDR1DQ[10]	R25	VDD1P5
N26	DDR1DQ[22]	P26	VSS	R26	DDR1DQ[14]
N27	VSS	P27	DDR0DQSP[2]	R27	DDR1DQ[15]
N28	DDR0DQ[23]	P28	DDR0DQSN[2]	R28	VSS
N29	DDR0DQ[22]	P29	VSS	R29	DDR0DQSN[11]
T1	DDR0DQSN[15]	U1	DDR0DQSP[6]	V1	VSS
T2	DDR0DQSN[6]	U2	VSS	V2	DDR0DQ[55]
T3	VDD1P5	U3	DDR0DQ[54]	V3	DDR0DQ[50]
T4	DDR0DQ[52]	U4	DDR0DQ[51]	V4	VDD1P5
T5	DDR1DQSP[6]	U5	VSS	V5	DDR1DQSP[16]
T6	VSS	U6	DDR1DQ[57]	V6	DDR1DQSN[16]
T7	DDR1DQ[61]	U7	DDR1DQ[56]	V7	DDR1DQ[63]
T8	DDR1DQ[60]	U8	VSS	V8	NC
T9	VDD1P5	U9	MB1_ID	V9	FBDSBIP[1]
T10	NC	U10	NC	V10	VCCFBD1P1
T11	NC	U11	NC	V11	NC
T12	VCC1P1	U12	VSS	V12	VCCFBD1P1
T13	VSS	U13	VCC1P1	V13	FBDSBIP[4]
T14	VCC1P1	U14	VSS	V14	VCCFBD1P1
T15	VSS	U15	VCC1P1	V15	FBDSBIP[9]

Table 4-4. Intel 7500/7510/7512 Scalable Memory Buffer Signals by Ball Number (Sheet 5 of 6)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
T16	VCC1P1	U16	VSS	V16	VCCFBD1P1
T17	VSS	U17	VCC1P1	V17	FBDSBIN[6]
T18	VCC1P1	U18	VSS	V18	VCCFBD1P1
T19	NC	U19	VCCFBD1P1	V19	NC
T20	DDR1DQ[13]	U20	NC	V20	VSS
T21	DDR1DQ[3]	U21	VSS	V21	FBDSBIN[10]
T22	DDR1DQSP[10]	U22	DDR1DQ[7]	V22	VSS
T23	DDR1DQ[2]	U23	DDR1DQSP[0]	V23	DDR1DQSN[9]
T24	VSS	U24	DDR1DQ[6]	V24	DDR1DQSN[0]
T25	DDR0DQ[11]	U25	DDR0DQ[15]	V25	VSS
T26	DDR0DQ[10]	U26	VDD1P5	V26	DDR0DQ[14]
T27	VSS	U27	DDR0DQ[16]	V27	DDR0DQSP[1]
T28	DDR0DQSP[11]	U28	DDR0DQ[21]	V28	VSS
T29	DDR0DQ[17]	U29	VDD1P5	V29	DDR0DQ[20]
W1	DDR0DQ[60]	Y1	DDR0DQ[56]	AA1	VDD1P5
W2	DDR0DQ[61]	Y2	VSS	AA2	DDR0DQSP[16]
W3	VSS	Y3	DDR0DQ[57]	AA3	DDR0DQSN[16]
W4	DDR1DQSN[7]	Y4	DDR1DQ[62]	AA4	VSS
W5	DDR1DQSP[7]	Y5	VSS	AA5	DDR0DQ[62]
W6	DDR1DQ[59]	Y6	DDR1DQ[58]	AA6	VSS
W7	VSS	Y7	VDD1P5	AA7	FBDNBOP[0]
W8	FBDSBIP[0]	Y8	FBDSBIN[0]	AA8	VSS
W9	FBDSBIN[1]	Y9	VSS	AA9	FBDNBOP[2]
W10	FBDSBIN[2]	Y10	FBDSBIP[2]	AA10	VSS
W11	NC	Y11	VSS	AA11	FBDNBOP[4]
W12	FBDSBIN[3]	Y12	FBDSBIP[3]	AA12	VSS
W13	FBDSBIN[4]	Y13	VSS	AA13	FBDNBOP[13]
W14	FBDSBICLKN	Y14	FBDSBICLKP	AA14	VSS
W15	FBDSBIN[9]	Y15	VSS	AA15	FBDNBON[12]
W16	FBDSBIP[5]	Y16	FBDSBIN[5]	AA16	VSS
W17	FBDSBIP[6]	Y17	VSS	AA17	FBDNBON[7]
W18	FBDSBIN[7]	Y18	FBDSBIP[7]	AA18	VSS
W19	NC	Y19	VSS	AA19	FBDNBON[9]
W20	FBDSBIP[8]	Y20	FBDSBIN[8]	AA20	VSS
W21	FBDSBIP[10]	Y21	VSS	AA21	NC
W22	VSS	Y22	DDR1DQ[5]	AA22	VSS
W23	DDR1DQSP[9]	Y23	DDR1DQ[0]	AA23	DDR1DQ[4]
W24	VDD1P5	Y24	DDR1DQ[1]	AA24	DDR0DQ[0]
W25	DDR0DQ[13]	Y25	DDR0DQ[12]	AA25	VSS
W26	DDR0DQ[8]	Y26	VSS	AA26	DDR0DQSP[0]
W27	VSS	Y27	DDR0DQ[3]	AA27	DDR0DQ[7]

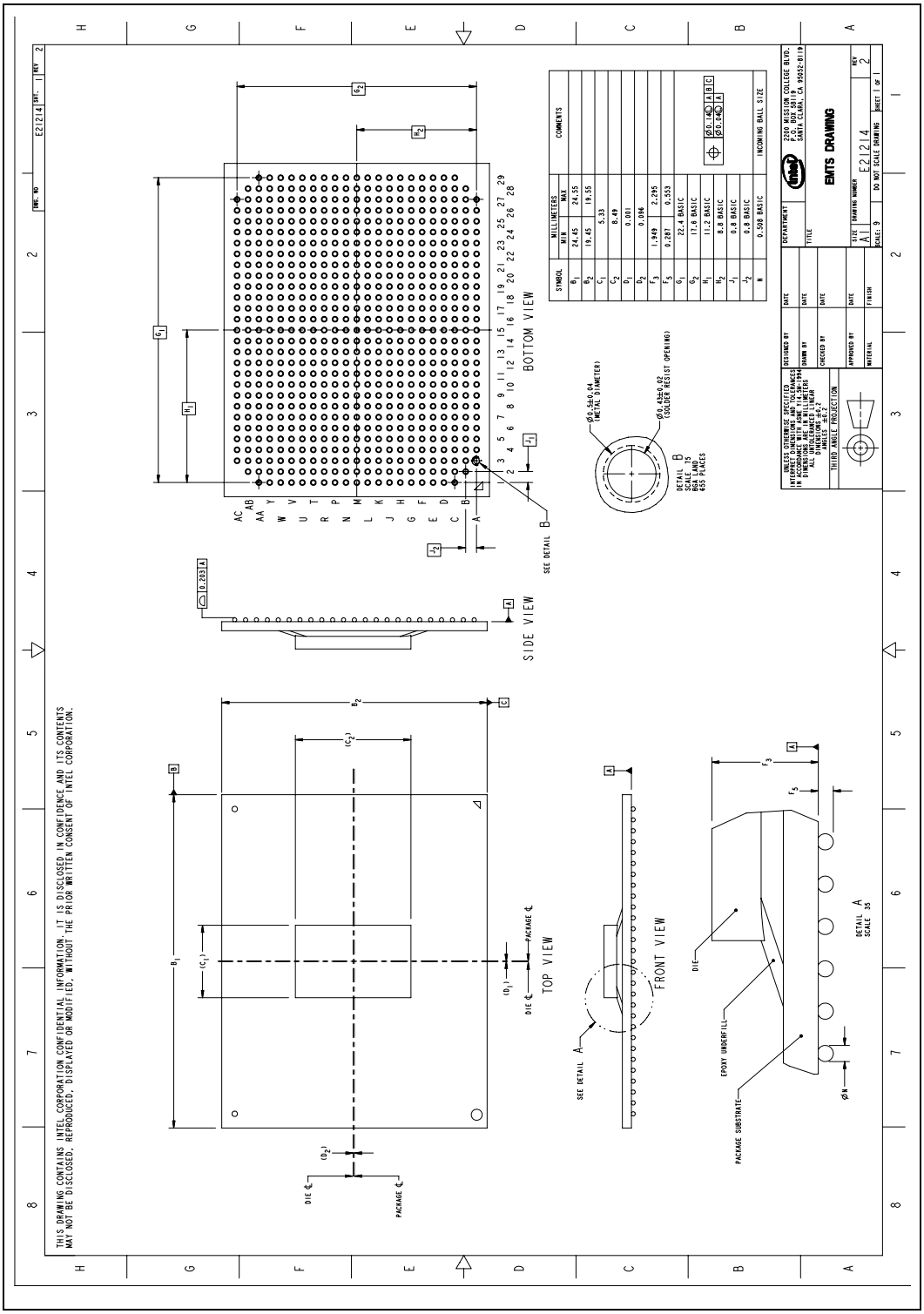
Table 4-4. Intel 7500/7510/7512 Scalable Memory Buffer Signals by Ball Number (Sheet 6 of 6)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
W28	DDR0DQSN[1]	Y28	DDR0DQSP[10]	AA28	DDR0DQ[2]
W29	DDR0DQSN[10]	Y29	DDR0DQ[9]	AA29	VSS
AB1	----	AC1	----		
AB2	VSS	AC2	----		
AB3	DDR0DQSN[7]	AC3	VDD1P5		
AB4	DDR0DQSP[7]	AC4	DDR0DQ[63]		
AB5	DDR0DQ[58]	AC5	DDR0DQ[59]		
AB6	NC	AC6	VSS		
AB7	FBDNBON[0]	AC7	VSS		
AB8	FBDNBOP[1]	AC8	FBDNBON[1]		
AB9	FBDNBON[2]	AC9	VSS		
AB10	FBDNBOP[3]	AC10	FBDNBON[3]		
AB11	FBDNBON[4]	AC11	VSS		
AB12	FBDNBOP[5]	AC12	FBDNBON[5]		
AB13	FBDNBON[13]	AC13	VSS		
AB14	FBDNBOCLKP	AC14	FBDNBOCLKN		
AB15	FBDNBOP[12]	AC15	VSS		
AB16	FBDNBON[6]	AC16	FBDNBOP[6]		
AB17	FBDNBOP[7]	AC17	VSS		
AB18	FBDNBON[8]	AC18	FBDNBOP[8]		
AB19	FBDNBOP[9]	AC19	VSS		
AB20	FBDNBON[10]	AC20	FBDNBOP[10]		
AB21	NC	AC21	VSS		
AB22	FBDNBON[11]	AC22	FBDNBOP[11]		
AB23	VSS	AC23	VREG1P8		
AB24	DDR0DQ[4]	AC24	DDR0DQ[5]		
AB25	DDR0DQSP[9]	AC25	DDR0DQ[1]		
AB26	DDR0DQSN[0]	AC26	DDR0DQSN[9]		
AB27	DDR0DQ[6]	AC27	VSS		
AB28	VDD1P5	AC28	----		
AB29	----	AC29	----		

4.3 Package information

Intel 7500/7510/7512 Scalable Memory Buffer uses a 655-ball FPGA, with 0.8 mm pitch.

Figure 4-1. Package Information



4.4 Intel 7512 Scalable Memory Buffer Split Rail Implementation (Low Power SKU)

Starting with the non-split rail ballout as shown in Section 4.2, the following changes are needed to implement a split rail solution to support Intel 7512 Scalable Memory Buffer. Split rail means 1 VR is used to generate VCC1P1, VCCTTA1P1 and a second VR is used to generate the VCCFBD1P1 rail.

1. All VCC1P1 balls except J17 need to be connected to P0V9 digital rail. J17 needs to be connected to VCCFBD1P1 rail (1.1 V rail).
2. V16, V18, U19 need to be connected to VCCTTA1P1.

   V10, V12, V14 need to be connected to 1.1 V VR (VCCFBD1P1; no change).

   The P0V9 (digital rail) and VCCTTA1P1 (analog rail) come from the same VR. The two rails have been split as close to the VR and routed the two rails separately to keep noise from coupling between these two rails.
3. Following pull-ups which used to be connected to 1.1 V (VCC1P1) now need to be connected to P0V9 digital rail.
   a. MA_event.
   b. JTAG: TMS, TDI, TDO need to be pulled to P0V9 rail.
   c. RST_N, SA0, also need to be P0V9V compatible.
4. Other notes:
   a. LAISCL, LAISDA are 1.1 V tolerant as long as these signals are pulled (not driven) high. Resistor pull ups to either P0V9 rail or 1.1 V are acceptable. The reference Schematic shows the pull-ups (3.3 K; 5%,1/16 W) to be connected to 1.1 V.
   b. SCL, SDA are 1.1 V tolerant as long as these signals are pulled (not driven) high.The PCA9517 component does not drive these signals to high and lets the external resistors pull up to the high level, it is ok to pull-up these signals to 1.1 V. Reference schematic shows the pull-up (2.2 K, 5%, 1/16 W) to 1.1 V.
   c. VCCPWRGOOD and VDDPWRGOOD are pulled-up to 1.1 V (VCCFBD1P1).

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