

Silicon Epicap Diodes

Designed for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q with Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Available in Surface Mount Package

MBV109T1
MMBV109LT1 *
MV209 *

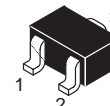
* Motorola Preferred Devices

26–32 pF
VOLTAGE VARIABLE
CAPACITANCE DIODES

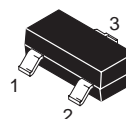


MAXIMUM RATINGS

Rating	Symbol	MBV109T1	MMBV109LT1	MV209	Unit
Reverse Voltage	V_R	30			Vdc
Forward Current	I_F	200			mAdc
Forward Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	280 2.8	200 2.0	200 1.6	mW mW/°C
Junction Temperature	T_J	+125			°C
Storage Temperature Range	T_{stg}	-55 to +150			°C



CASE 419-02, STYLE 3
SC-70/SOT-323



CASE 318-08, STYLE 6
SOT-23 (TO-236AB)



CASE 182-02, STYLE 1
TO-92 (TO-226AC)

DEVICE MARKING

MBV109T1 = J4A, MMBV109LT1 = M4A, MV209 = MV209

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage ($I_R = 10 \mu\text{Adc}$)	$V_{(BR)R}$	30	—	—	Vdc
Reverse Voltage Leakage Current ($V_R = 25 \text{ Vdc}$)	I_R	—	—	0.1	μAdc
Diode Capacitance Temperature Coefficient ($V_R = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	TC_C	—	300	—	ppm/°C

Device	C_t , Diode Capacitance $V_R = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$ pF			Q , Figure of Merit $V_R = 3.0 \text{ Vdc}$ $f = 50 \text{ MHz}$	C_R , Capacitance Ratio C_3/C_{25} $f = 1.0 \text{ MHz}$ (Note 1)	
	Min	Nom	Max	Min	Min	Max
MBV109T1, MMBV109LT1, MV209	26	29	32	200	5.0	6.5

1. C_R is the ratio of C_t measured at 3 Vdc divided by C_t measured at 25 Vdc.

MMBV109LT1 is also available in bulk packaging. Use **MMBV109L** as the device title to order this device in bulk.

Thermal Clad is a trademark of the Bergquist Company

Preferred devices are Motorola recommended choices for future use and best overall value.

(Replaces MMBV109LT1/D)



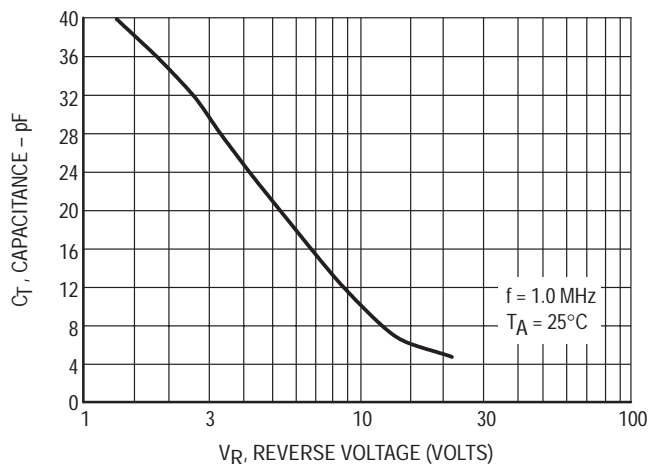


Figure 1. DIODE CAPACITANCE

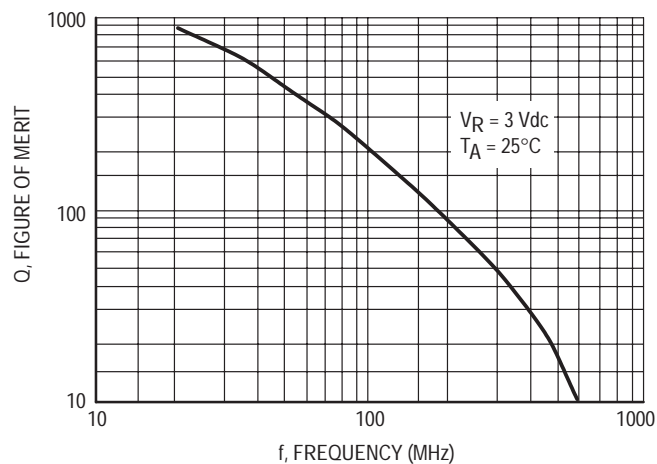


Figure 2. FIGURE OF MERIT

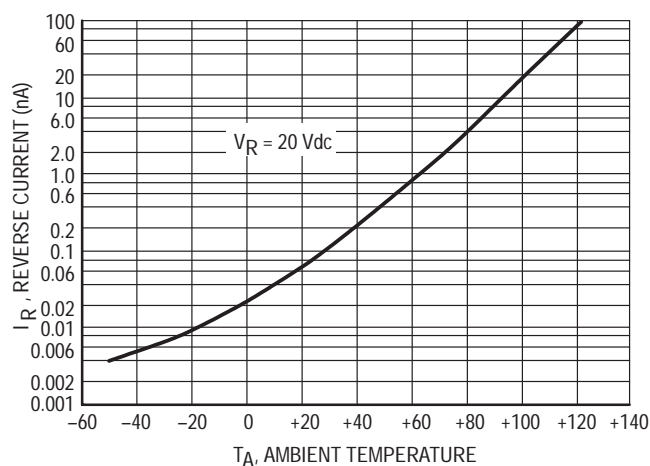


Figure 3. LEAKAGE CURRENT

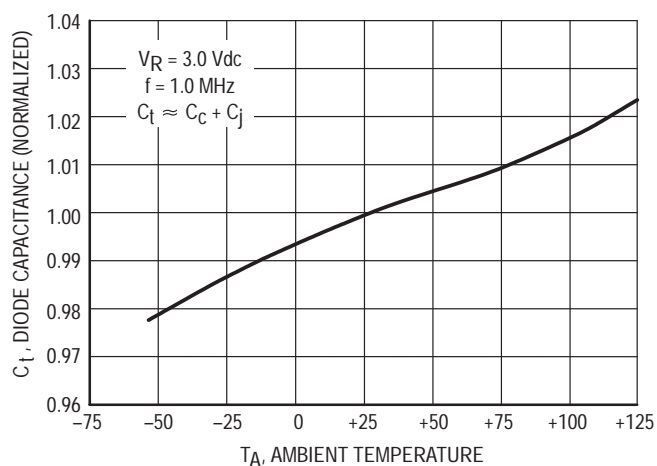


Figure 4. DIODE CAPACITANCE

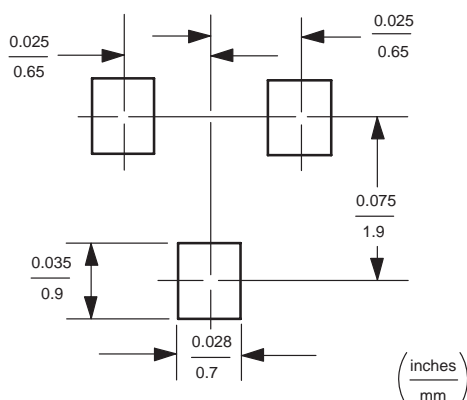
NOTES ON TESTING AND SPECIFICATIONS

1. C_R is the ratio of C_T measured at 3.0 Vdc divided by C_T measured at 25 Vdc.

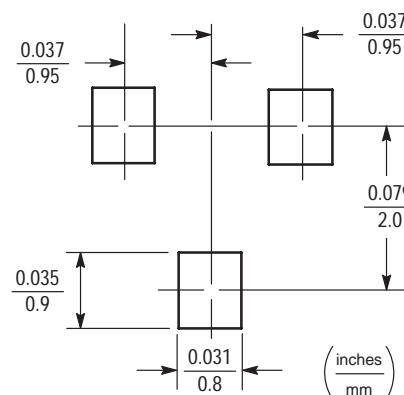
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SC-70/SOT-323



SOT-23

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the pad size. These can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A . Using the values provided on the data sheet, P_D can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT-23 device, P_D is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{556^\circ\text{C/W}} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT-23 assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.

- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches.

The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 5 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the

actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

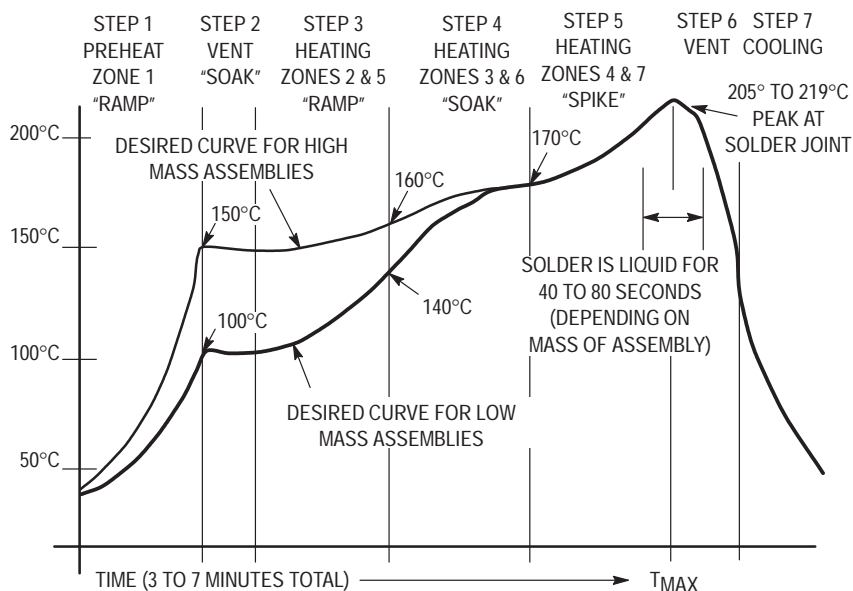
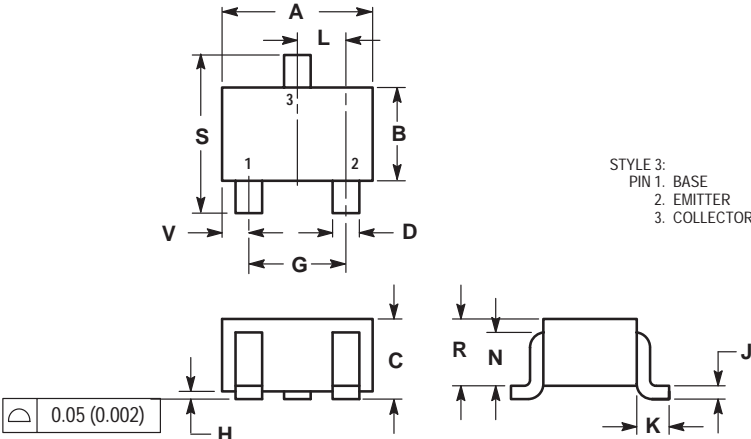


Figure 5. Typical Solder Heating Profile

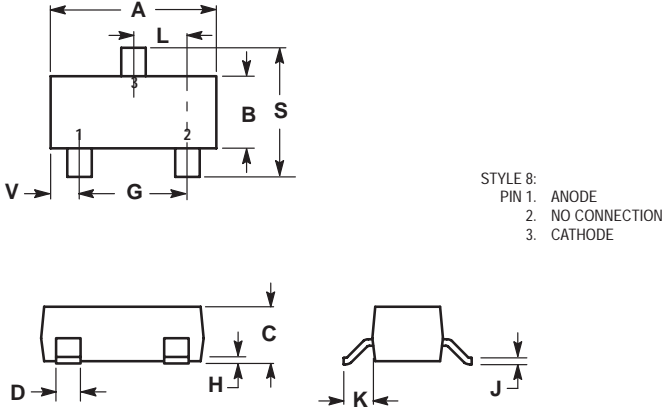
PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.035	0.049	0.90	1.25
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
R	0.031	0.039	0.80	1.00
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

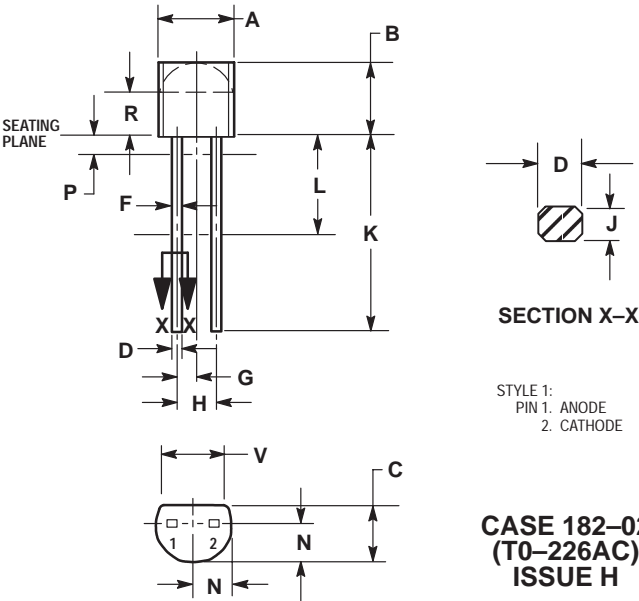
CASE 419-02
ISSUE E
SC-70/SOT-323



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

CASE 318-08
ISSUE AE
SOT-23 (TO-236AB)




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
 4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIM K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.21
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.49
D	0.016	0.022	0.41	0.56
F	0.016	0.019	0.407	0.482
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		3.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.03	2.66
P	---	0.050	---	1.27
R	0.115	---	2.93	---
V	0.135	---	3.43	---

CASE 182-02
(TO-226AC)
ISSUE H

NOTES

NOTES

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