

SN54LS590, SN54LS591, SN74LS590, SN74LS591 8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

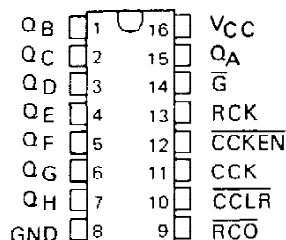
SDLS003

D2632, JANUARY 1981 — REVISED MARCH 1988

- 8-Bit Counter with Register
- Parallel Register Outputs
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency: DC to 20 MHz

SN54LS590, SN54LS591 . . . J OR W PACKAGE
SN74LS590, SN74LS591 . . . N PACKAGE

(TOP VIEW)



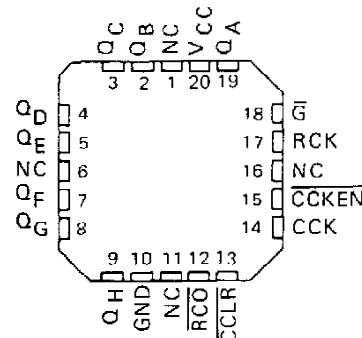
description

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

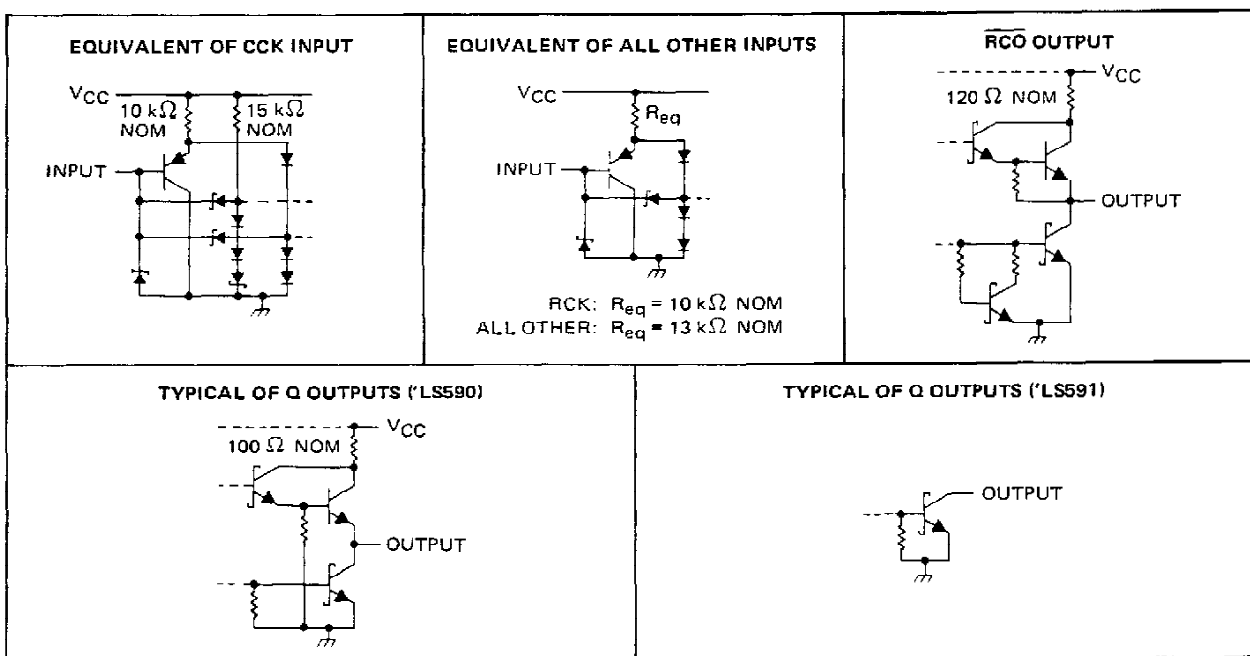
SN54LS590, SN54LS591 . . . FK PACKAGE

(TOP VIEW)



schematics of inputs and outputs

NC - No internal connection



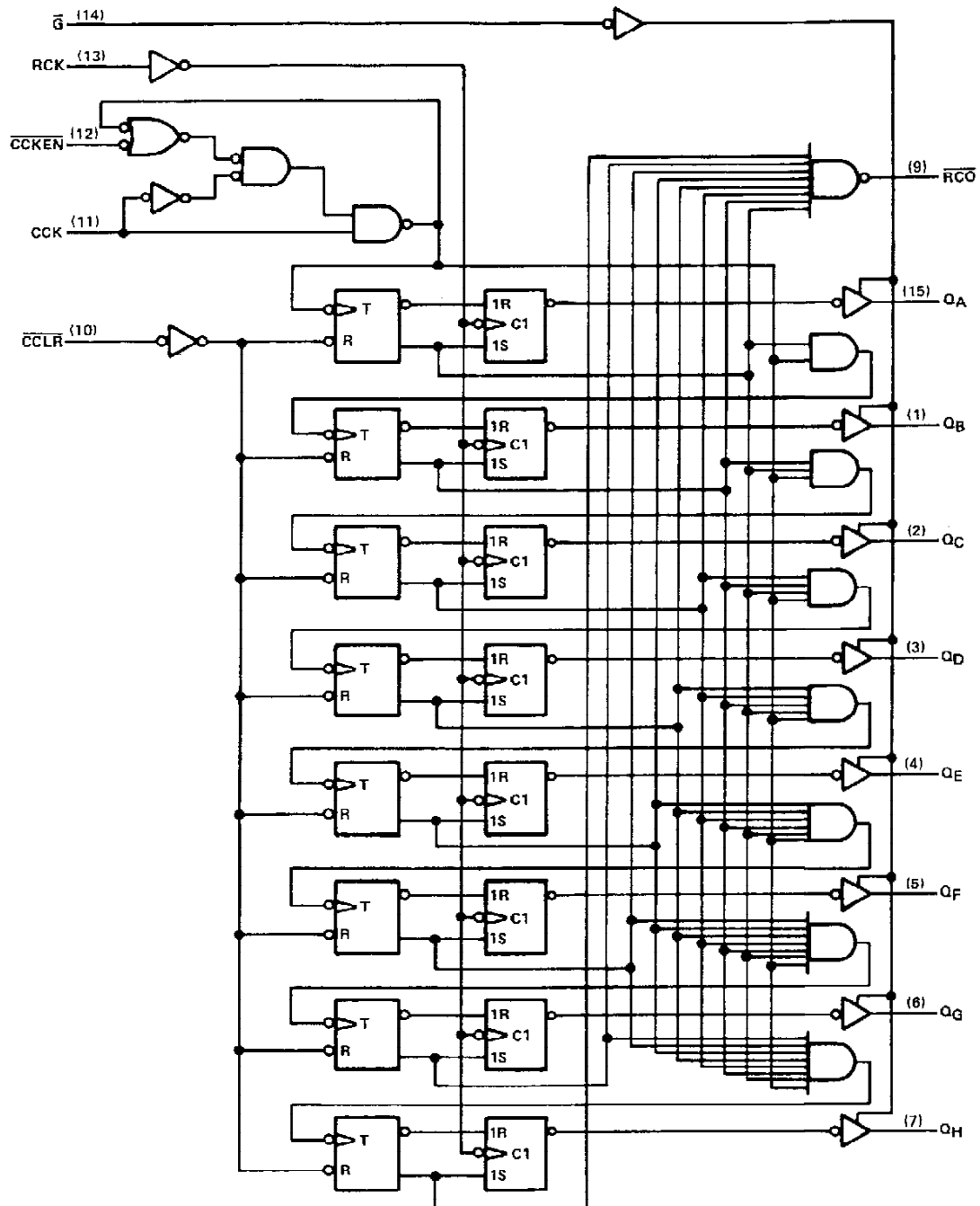
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS590, SN54LS591, SN74LS590, SN74LS591
8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

logic diagram (positive logic)



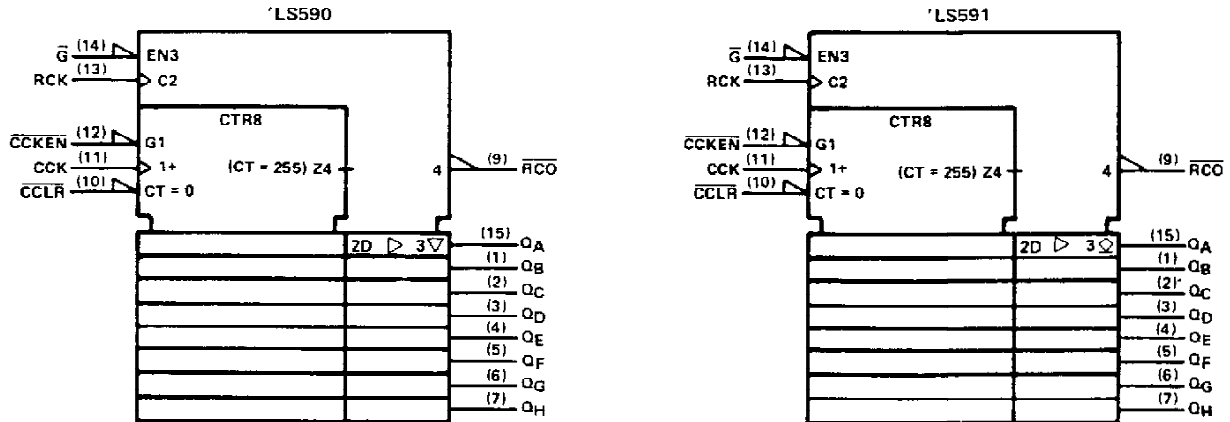
Pin numbers shown are for J, N and W packages.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS590, SN54LS591, SN74LS590, SN74LS591 8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591	-55°C to 125°C
SN74LS590, SN74LS591	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS*			SN74LS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage	Q, *LS591 only		5.5	5.5			V
I_{OH}	High-level output current	RCO		-1	-1			mA
		Q, *LS590 only		-1	-2.6			
I_{OL}	Low-level output current	RCO		8	16			mA
		Q		12	24			
f_{CCK}	Counter clock frequency	0		20	0		20	MHz
f_{RCK}	Register clock frequency	0		25	0		25	MHz
$t_w(CCK)$	Duration of counter clock pulse	25			25			ns
$t_w(CCLR)$	Duration of counter clear pulse	20			20			ns
$t_w(RCK)$	Duration of register clock pulse	20			20			ns
t_{su}	Setup time	CCKEN low before CCK†		20	20			ns
		CCLR inactive before CCK†		20	20			
		CCK before RCK† (see Note 2)		40	40			
t_h	Hold time	CCKEN low after CCK†		0	0			ns
T_A	Operating free-air temperature	-55		125	0		70	$^{\circ}\text{C}$

NOTE 2: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS590, SN54LS591, SN74LS590, SN74LS591

8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS*		SN74LS*		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN.	I _I = - 18 mA	- 1.5		- 1.5		V
V _{OH}	'LS590 Q	V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V,	I _{OH} = - 1 mA				V
	I _{OH} = - 2.6 mA			2.4 3.1				
	I _{OH} = - 1 mA			2.4 3.2				
R _{CO}								
I _{QH}	'LS591 Q	V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V, V _{OH} = 5.5 V,	0.1		0.1		mA
V _{OL}	Q	V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V,	I _{OL} = 12 mA		0.25 0.4		V
	I _{OL} = 24 mA			0.35 0.5				
	I _{OL} = 8 mA			0.25 0.4				
	I _{OL} = 16 mA			0.35 0.5				
R _{CO}								
I _{OZH}	'LS590 Q	V _{CC} = MAX, V _O = 2.7 V	V _{IH} = 2 V, V _{IL} = MAX,	20		20		μA
I _{OZL}	'LS590 Q	V _{CC} = MAX, V _O = 0.4 V	V _{IH} = 2 V, V _{IL} = MAX,	- 20		- 20		μA
I _I		V _{CC} = MAX,	V _I = 7 V	0.1		0.1		mA
I _{IH}		V _{CC} = MAX,	V _I = 2.7 V	20		20		μA
I _{IL}	CCK	V _{CC} = MAX,	V _I = 0.4 V	- 0.8		- 0.8		mA
	All others			- 0.2		- 0.2		
I _{OS} §	'LS590 Q	V _{CC} = MAX,	V _O = 0 V	- 30 - 130		- 30 - 130		mA
	R _{CO}			- 20 - 100		- 20 - 100		
I _{CC}	'LS590	V _{CC} = MAX, All possible inputs grounded, All outputs open		I _{CCH}		33 55		mA
				I _{CCL}		44 65		
				I _{CCZ}		46 65		
	'LS591			I _{CCH}		35 55		
				I _{CCL}		42 65		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V.}, T_A = 25^\circ\text{C}$

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V.}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS590			'LS591			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	RCK	Q	$R_L = 667 \Omega, C_L = 45 \text{ pF}$	20	35		20	35		MHz
t_{PLH}	CCK†	RCO	$R_L = 1 \text{ k}\Omega, C_L = 30 \text{ pF}$	14	22		16	24		ns
t_{PHL}	CCK†	RCO		20	30		25	38		ns
t_{PLH}	CCLR†	RCO		30	45		32	48		ns
t_{PLH}	RCK†	Q	$R_L = 667 \Omega, C_L = 45 \text{ pF}$	12	18		25	38		ns
t_{PHL}	RCK†	Q		22	33		28	42		ns
t_{PZH}	$\bar{G}_1$	Q		25	38					ns
t_{PZL}	$\bar{G}_1$	Q		30	45					ns
t_{PHZ}	$\bar{G}_1$	Q	$R_L = 667 \Omega, C_L = 5 \text{ pF}$	20	30					ns
t_{PLZ}	$\bar{G}_1$	Q		25	38					ns
t_{PLH}	$\bar{G}_1$	Q	$R_L = 667 \Omega, C_L = 45 \text{ pF}$				34	50		ns
t_{PHL}	$\bar{G}_1$	Q					32	48		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87517012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87517012A SNJ54LS 590FK
5962-8751701EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J
5962-8751701EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J
SN54LS590J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS590J
SN54LS590J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS590J
SN54LS590J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS590J
SN54LS590J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS590J
SN74LS590D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590
SN74LS590D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590
SN74LS590D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590
SN74LS590D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590
SN74LS590N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS590N
SN74LS590N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS590N
SN74LS590N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS590N
SN74LS590N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS590N
SN74LS590NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590
SN74LS590NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590
SN74LS590NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590
SN74LS590NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590
SNJ54LS590FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87517012A SNJ54LS 590FK
SNJ54LS590FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87517012A SNJ54LS 590FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS590FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87517012A SNJ54LS 590FK
SNJ54LS590FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87517012A SNJ54LS 590FK
SNJ54LS590J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J
SNJ54LS590J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J
SNJ54LS590J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J
SNJ54LS590J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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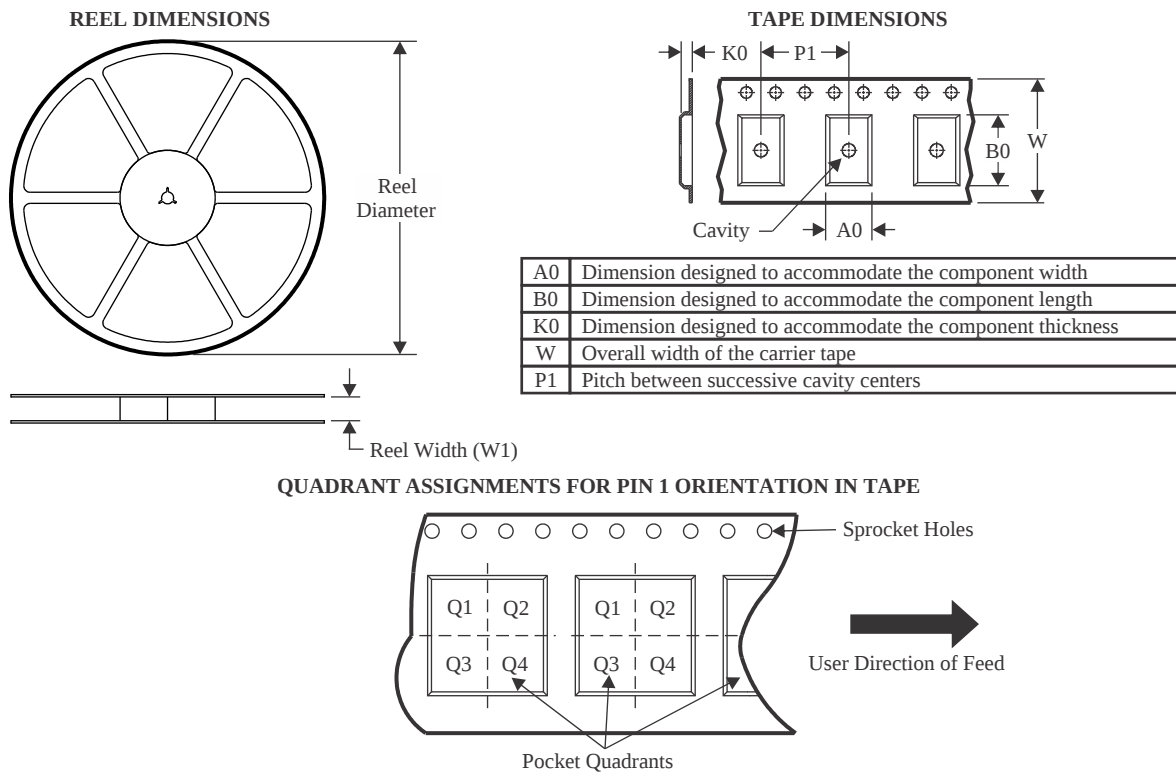
OTHER QUALIFIED VERSIONS OF SN54LS590, SN74LS590 :

- Catalog : [SN74LS590](#)
- Military : [SN54LS590](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

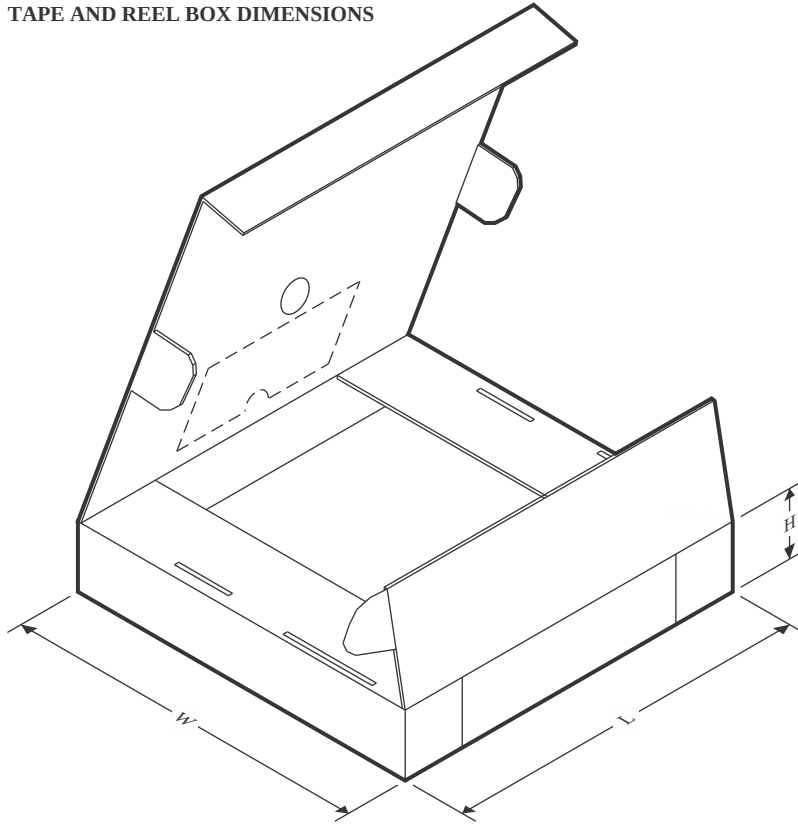
TAPE AND REEL INFORMATION



*All dimensions are nominal

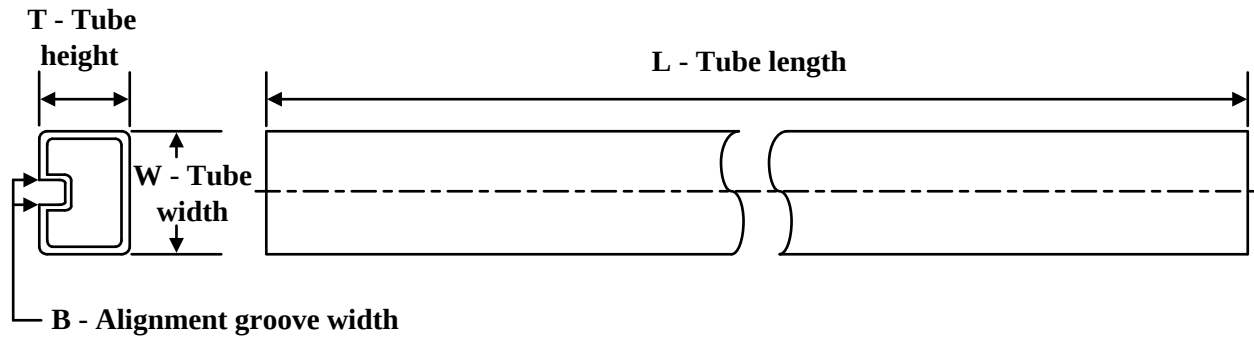
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS590NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS590NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87517012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74LS590D	D	SOIC	16	40	507	8	3940	4.32
SN74LS590D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS590N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS590N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS590N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS590N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS590FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS590FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

GENERIC PACKAGE VIEW

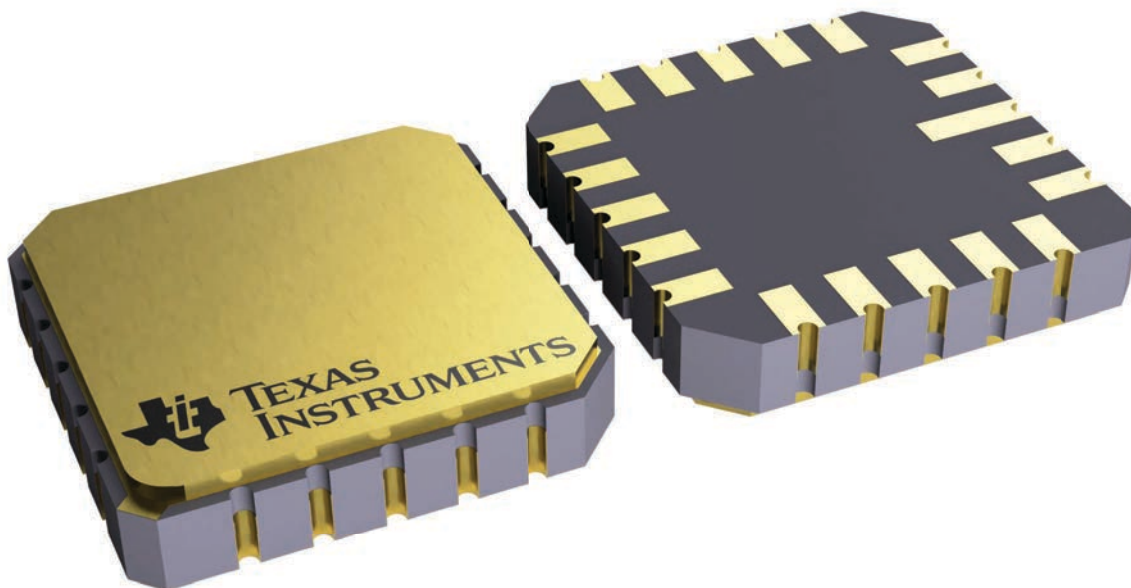
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



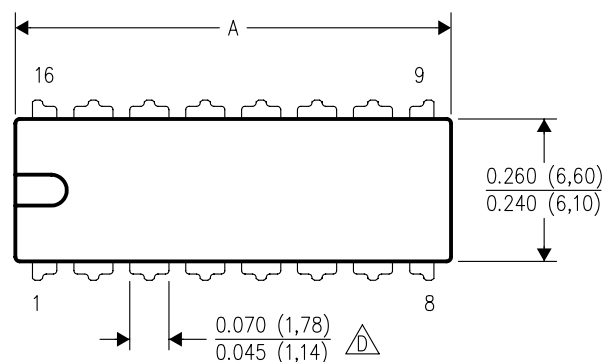
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

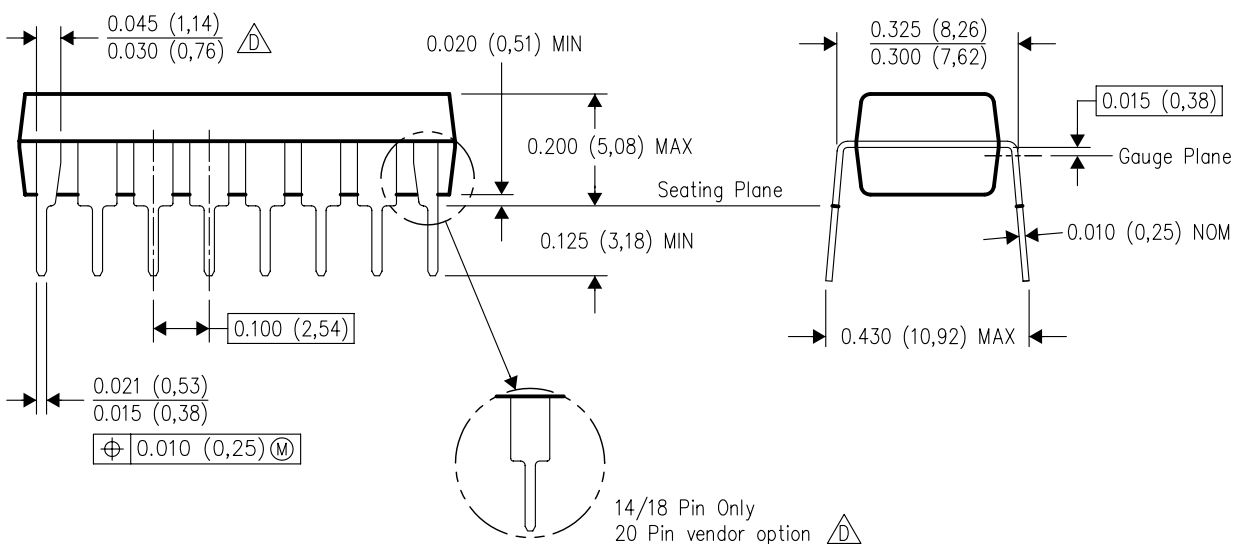
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



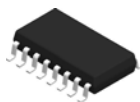
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

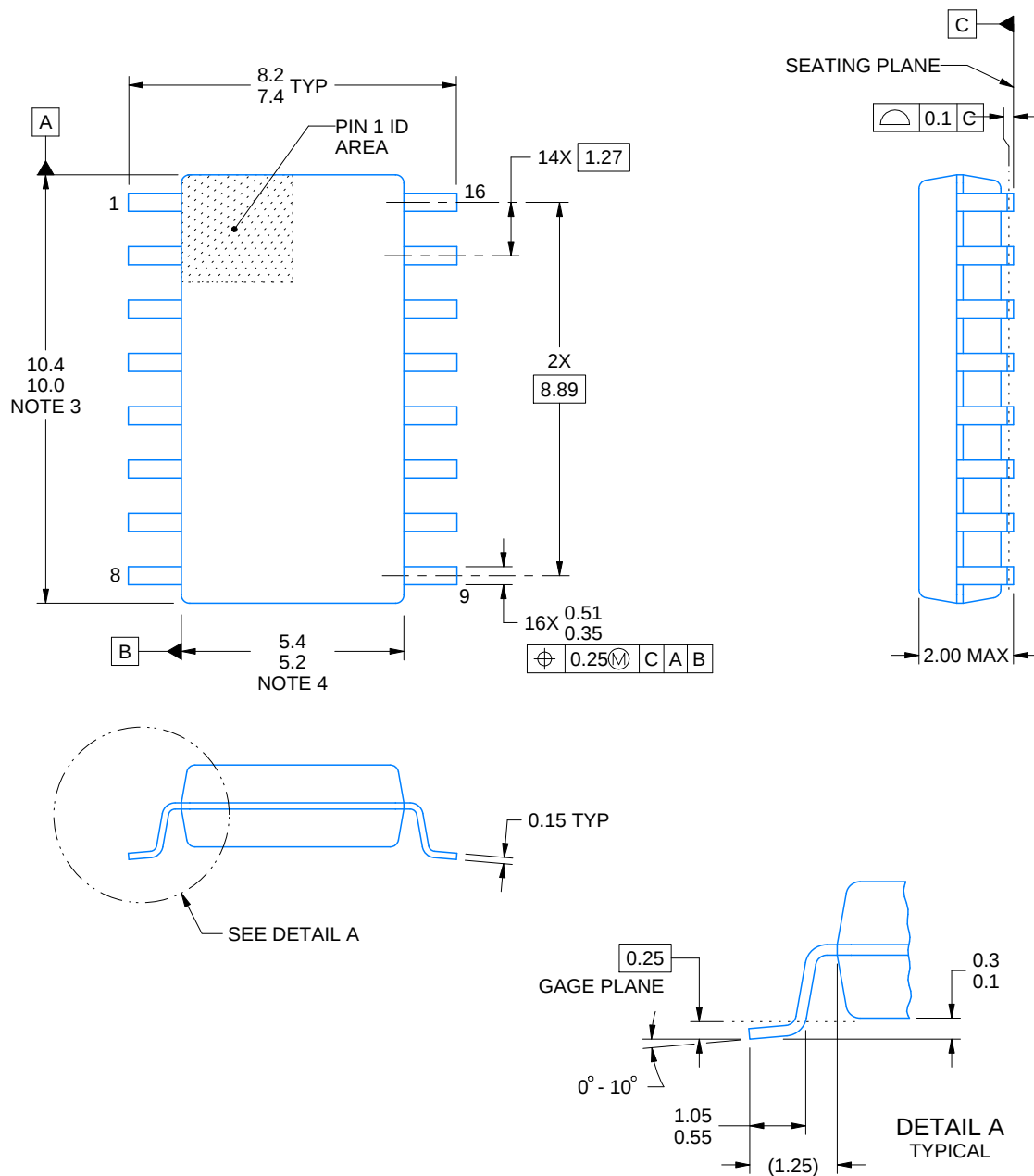


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

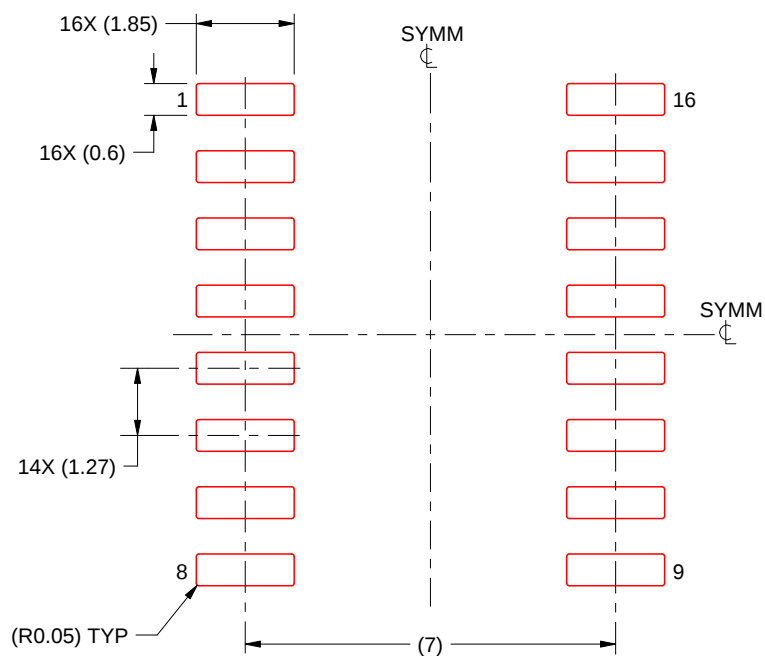
SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

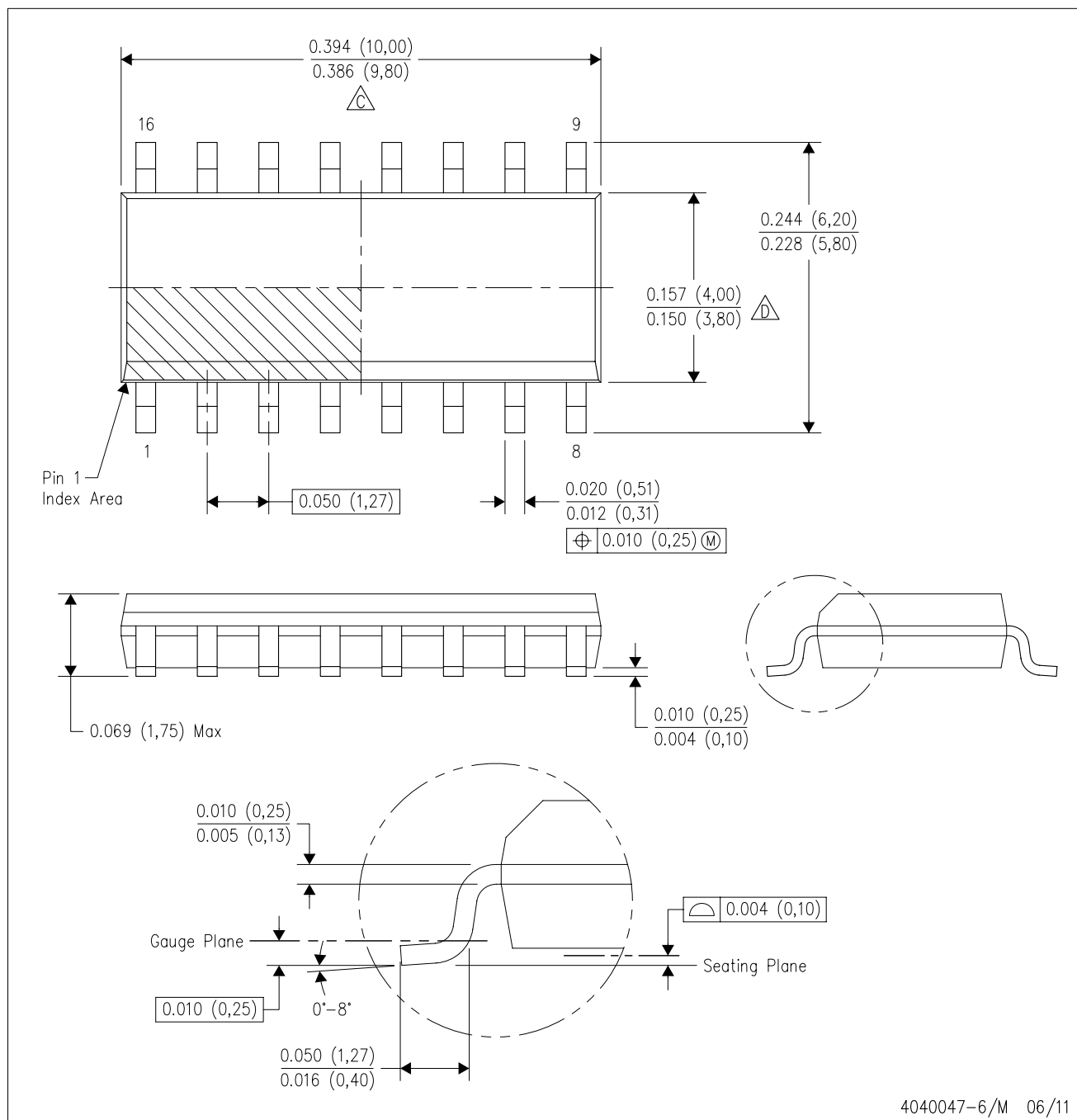
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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