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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM62V16256C Series

4 M SRAM (256-kword $\times$ 16-bit)



ADE-203-1099G (Z)

Rev. 4.0

Jul. 31, 2002

Description

The Hitachi HM62V16256C Series is 4-Mbit static RAM organized 262,144-word $\times$ 16-bit. HM62V16256C Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

Features

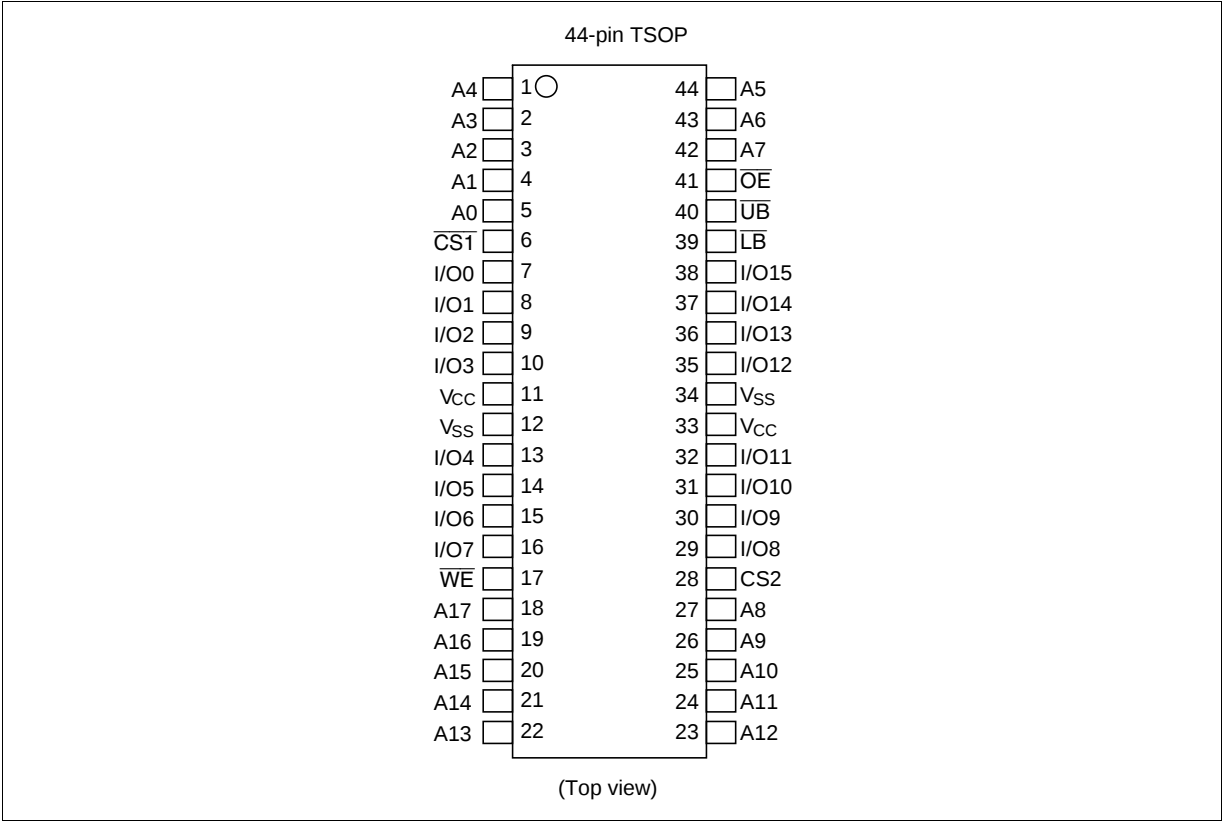
- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 55 ns (max)
- Power dissipation:
 - Active: 5.0 mW/MHz (typ) ($V_{CC} = 2.5$ V)
: 6.0 mW/MHz (typ) ($V_{CC} = 3.0$ V)
 - Standby: 2 μ W (typ) ($V_{CC} = 2.5$ V)
: 2.4 μ W (typ) ($V_{CC} = 3.0$ V)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup

HM62V16256C Series

Ordering Information

Type No.	Access time	Package
HM62V16256CLTT-5	55 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB)
HM62V16256CLTT-5SL	55 ns	

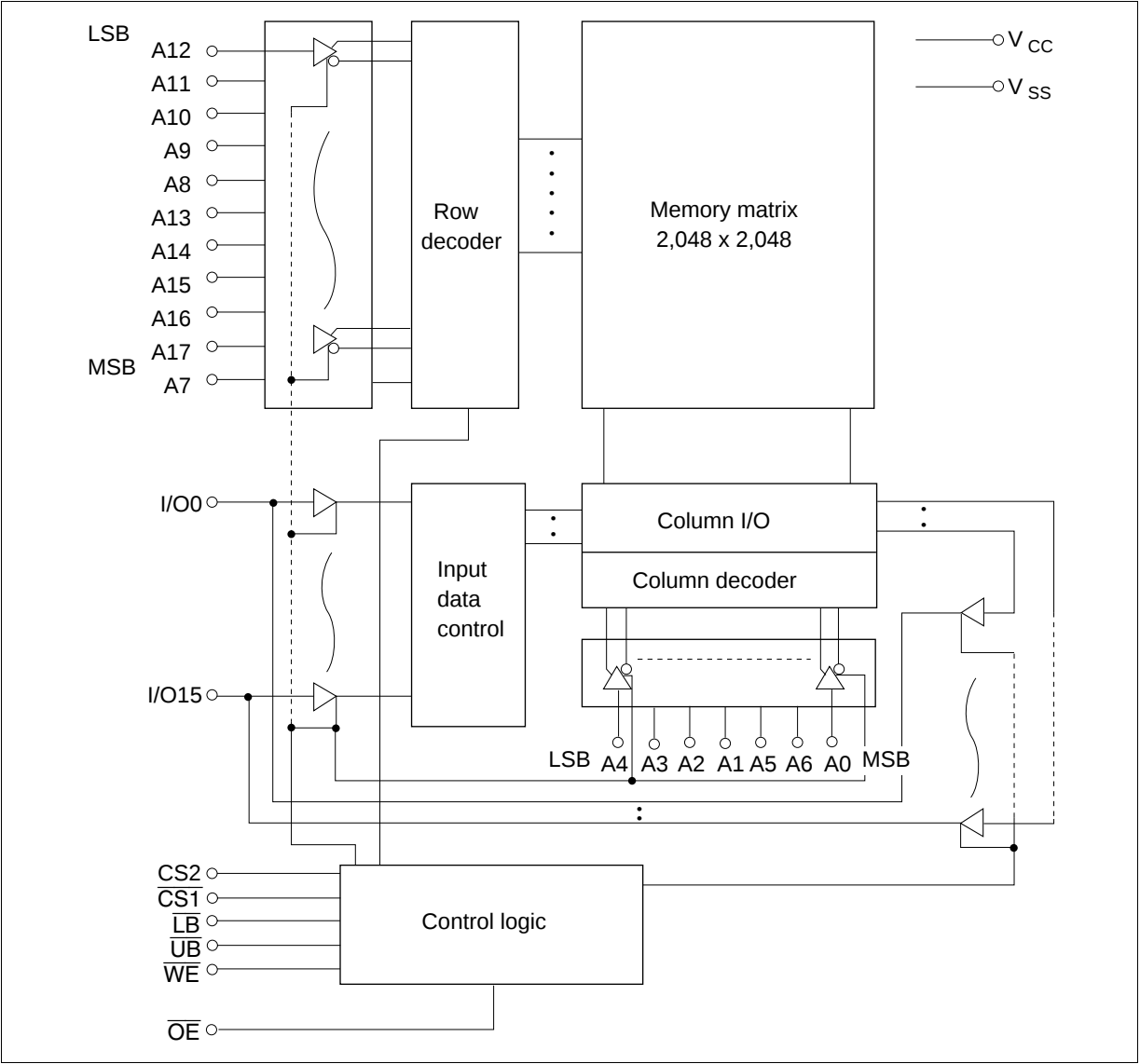
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
$\overline{CS2}$	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Operation Table

CS1	CS2	WE	OE	UB	LB	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-20 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.2	2.5/3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	$V_{CC} = 2.2$ V to 2.7 V	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
	$V_{CC} = 2.7$ V to 3.6 V	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{CC} = 2.2$ V to 2.7 V	V_{IL}	-0.2	—	0.4	V 1
	$V_{CC} = 2.7$ V to 3.6 V	V_{IL}	-0.3	—	0.6	V 1
Ambient temperature range	Ta	-20	—	70	°C	

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$, $V_{IO} = V_{SS}$ to V_{CC}
Operating current	I_{CC}	—	5	20	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL} , $I_{IO} = 0$ mA
Average operating current	I_{CC1}	—	8	25	mA	Min. cycle, duty = 100%, $I_{IO} = 0$ mA, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2	5	mA	Cycle time = 1 μs , duty = 100%, $I_{IO} = 0$ mA, $\overline{CS1} \leq 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	I_{SB}	—	0.1	0.3	mA	$CS2 = V_{IL}$
Standby current	I_{SB1}^{*2}	—	0.5	20	μA	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$ or (3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 \text{ V}$ $CS2 \geq V_{CC} - 0.2 \text{ V}$ $\overline{CS1} \leq 0.2 \text{ V}$
	I_{SB1}^{*3}	—	0.5	10	μA	
Output high voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$ V_{OH}	2.0	—	—	V	$I_{OH} = -0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ V_{OH}	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$ V_{OH}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100 \mu\text{A}$
Output low voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$ V_{OL}	—	—	0.4	V	$I_{OL} = 0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ V_{OL}	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$ V_{OL}	—	—	0.2	V	$I_{OL} = 100 \mu\text{A}$

Notes: 1. Typical values are at $V_{CC} = 2.5 \text{ V}/3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

Capacitance ($T_a = +25^{\circ}\text{C}$, $f = 1.0\text{ MHz}$)

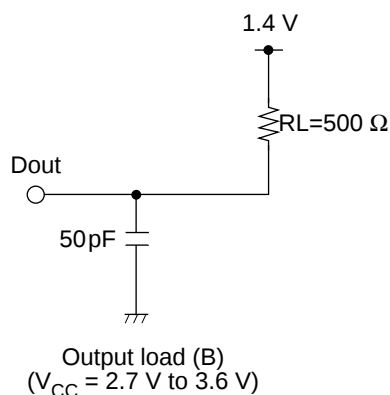
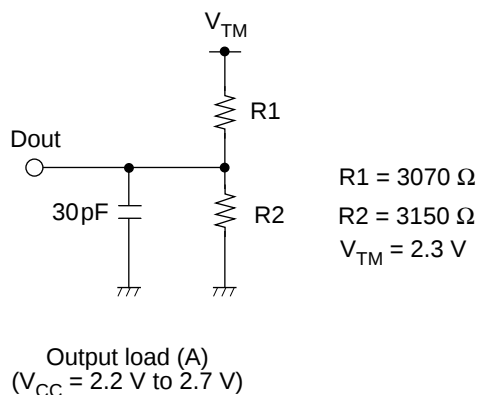
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{i/o}$	—	—	10	pF	$V_{i/o} = 0\text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = -20 to +70°C, V_{CC} = 2.2 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.0 V (V_{CC} = 2.2 V to 2.7 V)
V_{IL} = 0.4 V, V_{IH} = 2.2 V (V_{CC} = 2.7 V to 3.6 V)
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.1 V (V_{CC} = 2.2 V to 2.7 V)
- Output timing reference levels: 1.1 V (V_{CC} = 2.2 V to 2.7 V)
- Input timing reference levels: 1.4 V (V_{CC} = 2.7 V to 3.6 V)
- Output timing reference levels: 1.4 V (V_{CC} = 2.7 V to 3.6 V)
- Output load: See figures (Including scope and jig)



Read Cycle

		HM62V16256C			
		-5			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	ns	
Address access time	t _{AA}	—	55	ns	
Chip select access time	t _{ACS1}	—	55	ns	
	t _{ACS2}	—	55	ns	
Output enable to output valid	t _{OE}	—	35	ns	
Output hold from address change	t _{OH}	10	—	ns	
$\overline{LB}$, $\overline{UB}$ access time	t _{BA}	—	55	ns	
Chip select to output in low-Z	t _{CLZ1}	10	—	ns	2, 3
	t _{CLZ2}	10	—	ns	2, 3
$\overline{LB}$, $\overline{UB}$ enable to low-z	t _{BLZ}	5	—	ns	2, 3
Output enable to output in low-Z	t _{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t _{CHZ1}	0	20	ns	1, 2, 3
	t _{CHZ2}	0	20	ns	1, 2, 3
$\overline{LB}$, $\overline{UB}$ disable to high-Z	t _{BHZ}	0	20	ns	1, 2, 3
Output disable to output in high-Z	t _{OHZ}	0	20	ns	1, 2, 3

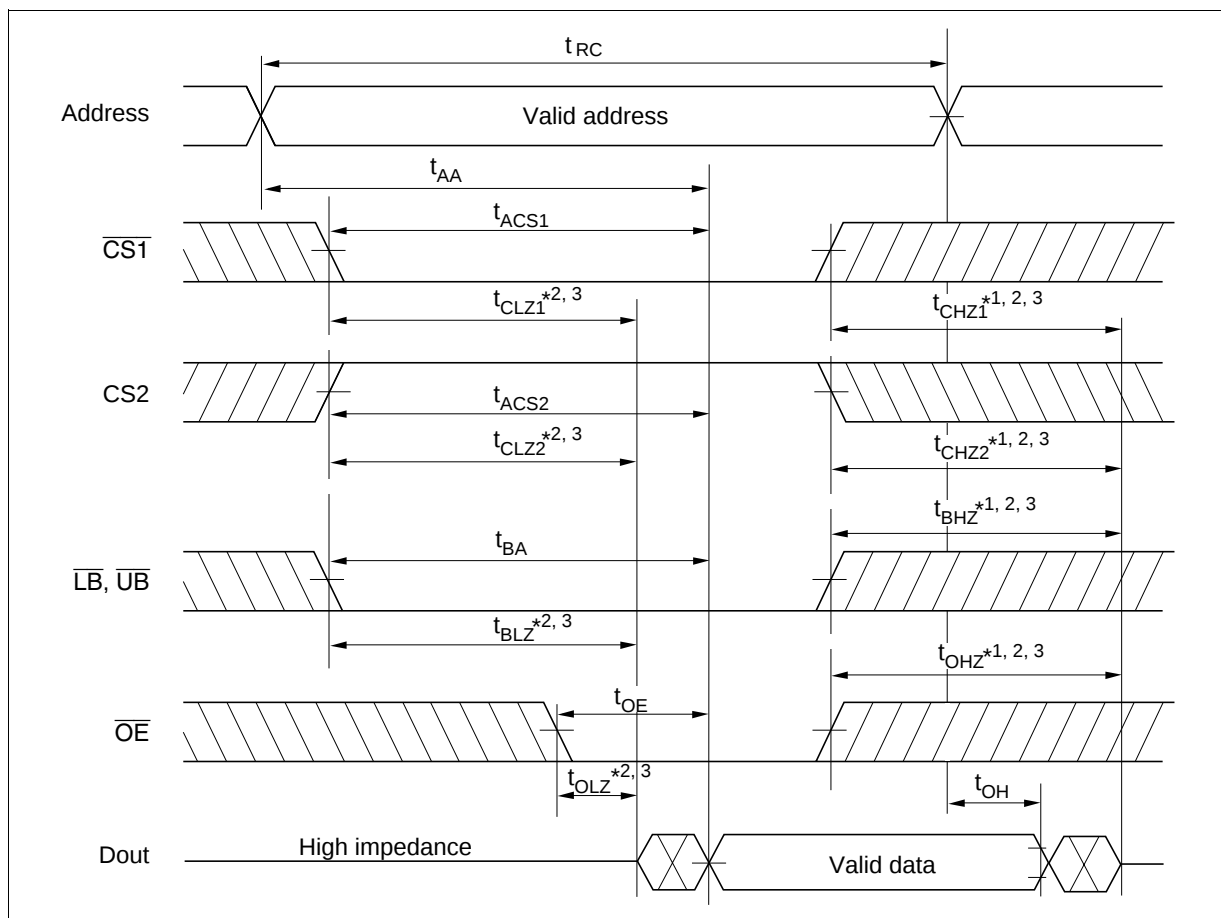
Write Cycle

		HM62V16256C			
		-5			
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	ns	
Address valid to end of write	t _{AW}	50	—	ns	
Chip selection to end of write	t _{CW}	50	—	ns	5
Write pulse width	t _{WP}	40	—	ns	4
$\overline{LB}$, $\overline{UB}$ valid to end of write	t _{BW}	50	—	ns	
Address setup time	t _{AS}	0	—	ns	6
Write recovery time	t _{WR}	0	—	ns	7
Data to write time overlap	t _{DW}	25	—	ns	
Data hold from write time	t _{DH}	0	—	ns	
Output active from end of write	t _{OW}	5	—	ns	2
Output disable to output in High-Z	t _{OHZ}	0	20	ns	1, 2
Write to output in high-Z	t _{WHZ}	0	20	ns	1, 2

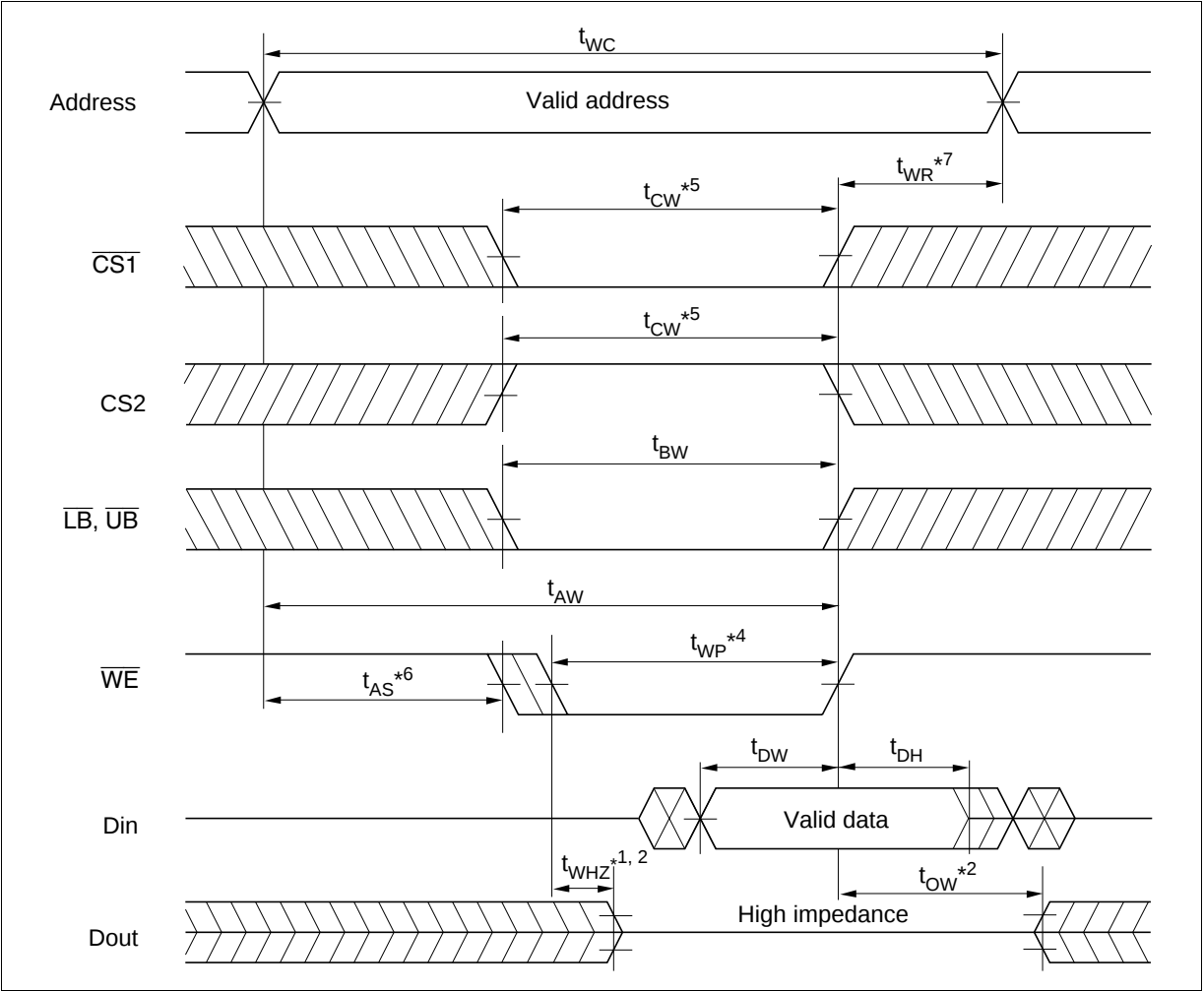
- Notes:
1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$, a low $\overline{WE}$ and a low $\overline{LB}$ or a low $\overline{UB}$. A write begins at the latest transition among $\overline{CS1}$ going low, $CS2$ going high, $\overline{WE}$ going low and $\overline{LB}$ going low or $\overline{UB}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low, $\overline{WE}$ going high and $\overline{LB}$ going high or $\overline{UB}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of $\overline{CS1}$ going low or $CS2$ going high to the end of write.
 6. t_{AS} is measured from the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or $CS2$ going low to the end of write cycle.

Timing Waveform

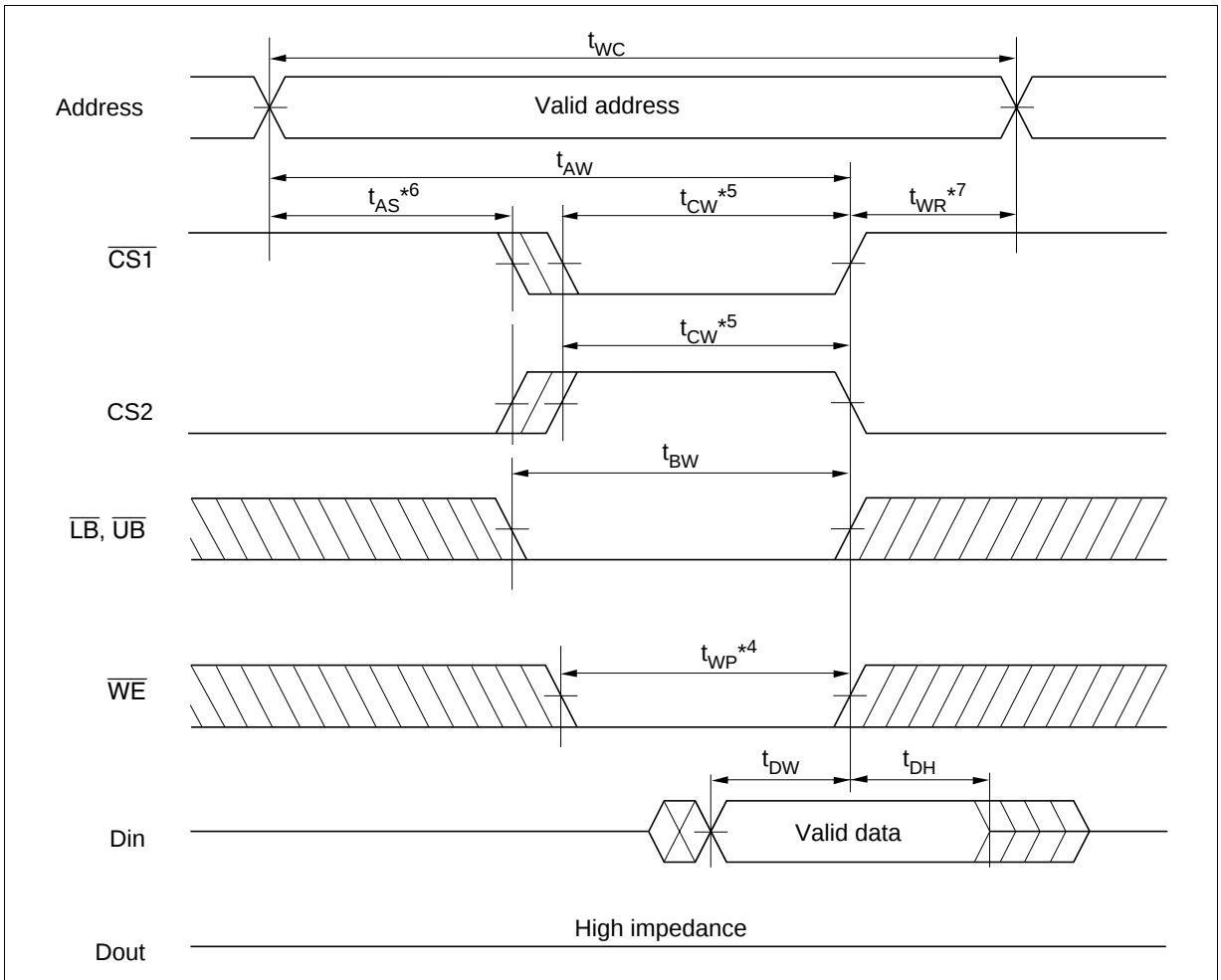
Read Cycle



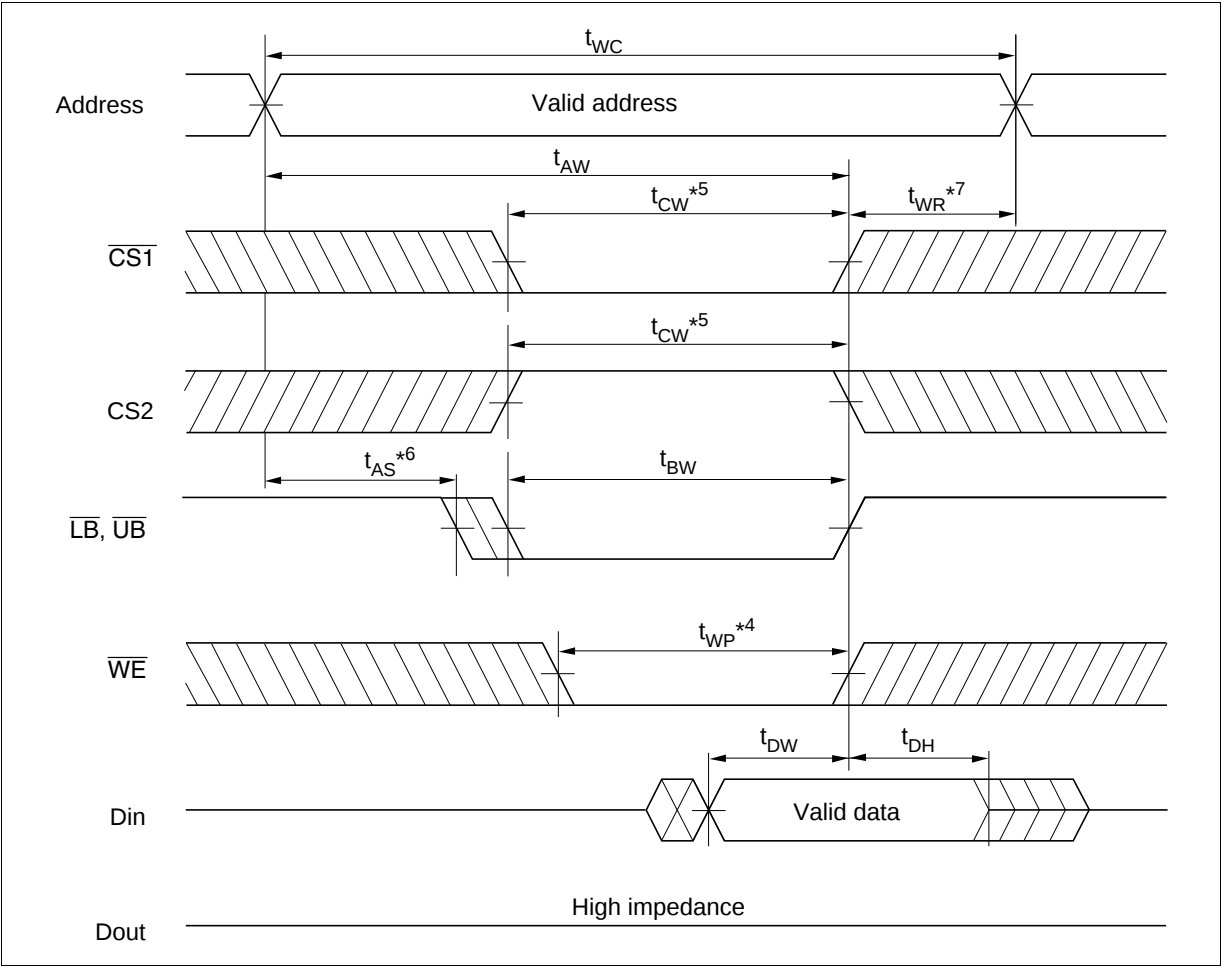
Write Cycle (1) ($\overline{\text{WE}}$ Clock)



Write Cycle (2) ($\overline{\text{CS}}$ Clock, $\overline{\text{OE}} = V_{\text{IH}}$)



Write Cycle (3) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Clock, $\overline{\text{OE}} = V_{\text{IH}}$)

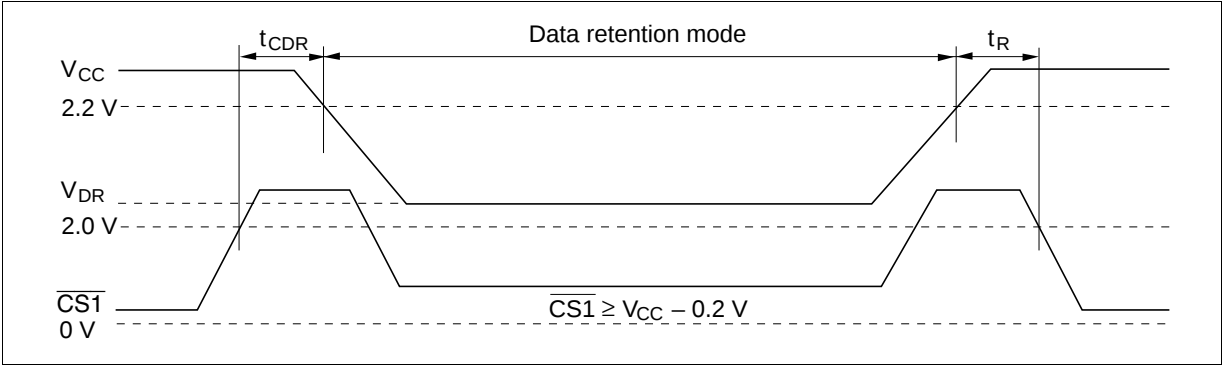


Low V_{CC} Data Retention Characteristics ($T_a = -20$ to $+70^{\circ}\text{C}$)

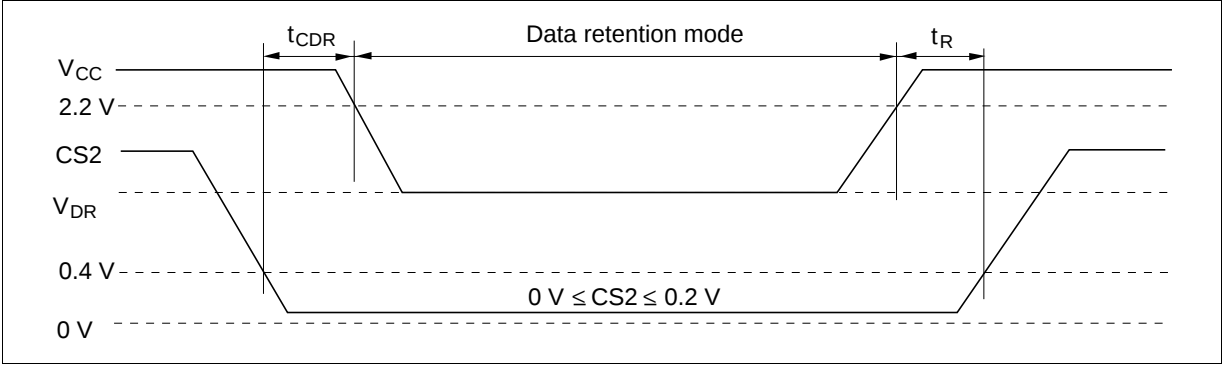
Parameter	Symbol	Min	Typ ^{*4}	Max	Unit	Test conditions ^{*3}
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	$V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \leq 0.2\text{V}$
Data retention current	I_{CCDR}^{*1}	—	0.5	20	μA	$V_{CC} = 3.0\text{V}$, $V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \leq 0.2\text{V}$
	I_{CCDR}^{*2}	—	0.5	10	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*5}	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L-version, 10 μA max. at $T_a = -20$ to $+40^{\circ}\text{C}$.
 2. This characteristic is guaranteed only for L-SL version, 3 μA max. at $T_a = -20$ to $+40^{\circ}\text{C}$.
 3. CS2 controls address buffer, $\overline{\text{WE}}$ buffer, $\overline{\text{CS1}}$ buffer, $\overline{\text{OE}}$ buffer, $\overline{\text{LB}}$, $\overline{\text{UB}}$ buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CS1}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, I/O) can be in the high impedance state. If $\overline{\text{CS1}}$ controls data retention mode, CS2 must be $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$. The other input levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0\text{V}$, $T_a = +25^{\circ}\text{C}$ and not guaranteed.
 5. t_{RC} = read cycle time.

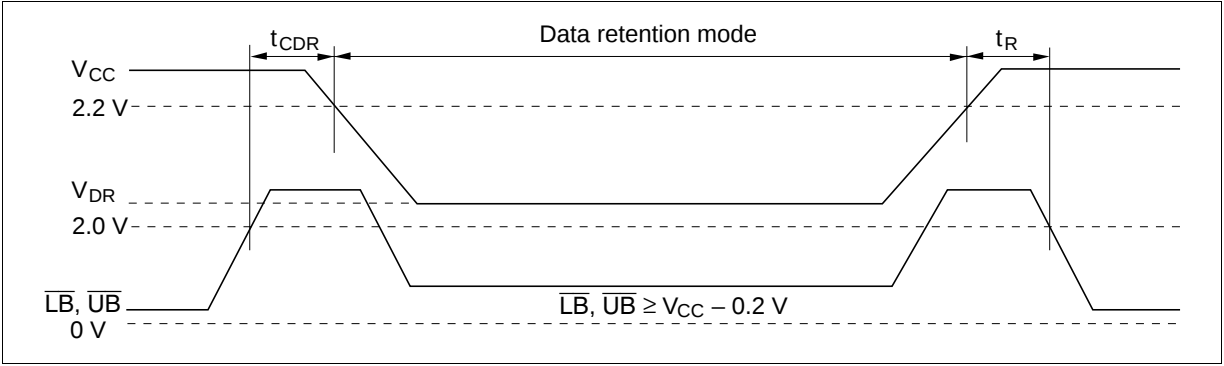
Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) ($CS2$ Controlled)



Low V_{CC} Data Retention Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



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