

High-Current VCOM Drive Op Amps for TFT LCDs

General Description

The MAX9650/MAX9651 are single- and dual-channel VCOM amplifiers with rail-to-rail inputs and outputs. The MAX9650/MAX9651 can drive up to 1300mA of peak current per channel and operate up to 20V.

The MAX9650/MAX9651 are designed to source and sink a high current quickly to hold the VCOM voltage stable in large TFT-LCD panels.

The MAX9650/MAX9651 feature 40V/ μ s slew rate and 35MHz bandwidth to quickly settle outputs for 120Hz frame rate and full HD television.

The MAX9650/MAX9651 feature output short-circuit protection and thermal shutdown. These devices are available in exposed pad packages for excellent heat dissipation.

Applications

TFT-LCD Panels

Instrument Control Voltage Sources

Features

- ◆ 1300mA Peak Output Current
- ◆ Rail-to-Rail Inputs and Outputs
- ◆ Operates Up to 20V
- ◆ 40V/ μ s Slew Rate
- ◆ 35MHz Bandwidth
- ◆ 5mA Quiescent Current per Channel
- ◆ Excellent Heat Dissipation (Exposed Pad)

Ordering Information

PART	AMPS PER PACKAGE	PIN-PACKAGE	TOP MARK
MAX9650AZK+	1	5 SOT23	ADSI
MAX9650AZK/V+	1	5 SOT23	ADSK
MAX9650AUA+	1	8 μ MAX-EP*	AABI
MAX9650ATA+	1	8 TDFN-EP*	BKX
MAX9651AUA+	2	8 μ MAX-EP*	AABH
MAX9651ATA+	2	8 TDFN-EP*	BKY

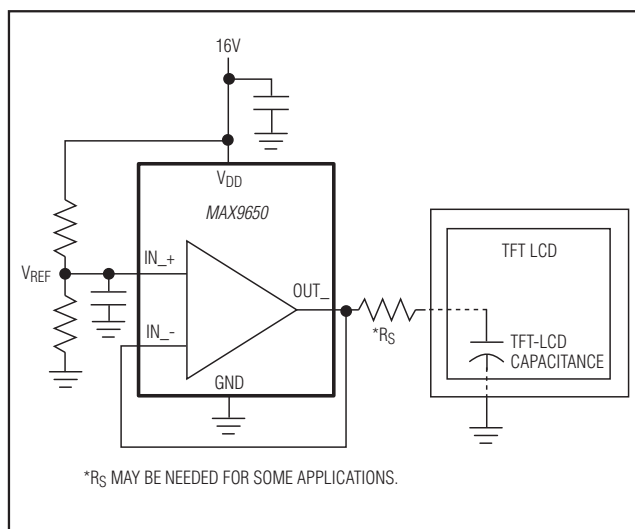
Note: All devices are specified over the -40°C to +125°C operating range.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

*EP = Exposed pad.

Typical Operating Circuit



MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to GND) -0.3V to +22V
Any Other Pin to GND -0.3V to (V_{DD} + 0.3V)
 I_{N+}/I_{N-} (current) ± 20 mA
 I_{OUT-} (current) 1.3A
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 SOT23 (derate 3.7mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 297.4mW
 $\mu\text{MAX-EP}$ (derate 12.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 1030.9mW
 TDFN-EP (derate 23.8mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 1951.2mW

Operating Temperature Range -40°C to $+125^\circ\text{C}$
Junction Temperature $+150^\circ\text{C}$
Storage Temperature Range -65°C to $+150^\circ\text{C}$
Lead Temperature (soldering, 10s) $+300^\circ\text{C}$
Soldering Temperature (reflow) $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 19\text{V}$, $V_{GND} = 0\text{V}$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR	6		20	V
Quiescent Current	I_{DD}	Per channel		3.7	8	mA
High Output Voltage	V_{OH}	$I_H = +5\text{mA}$, $V_{IN} = V_{DD}$	$V_{DD} - 0.30$	$V_{DD} - 0.05$		V
Low Output Voltage	V_{OL}	$I_L = -5\text{mA}$, $V_{IN} = 0\text{V}$		0.05	0.30	V
Input Offset Voltage	V_{OS}	$T_A = +25^\circ\text{C}$	-14	3.5	+14	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-17		+17	
Load Regulation	LR	$I_{OUT} = 0\text{mA}$ to -80mA		+0.2		mV/mA
		$I_{OUT} = 0\text{mA}$ to $+80\text{mA}$		-0.2		
Input Bias Current	I_{FB}	At $V_{IN} = 9.5\text{V}$		0.01	1	μA
Voltage Gain	A_V	$R_L = 10\text{k}\Omega$, $C_L = 50\text{pF}$	0.99		1.01	V/V
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 6\text{V}$ to 20V , $V_{CM} = V_{OUT} = 3\text{V}$	70	95		dB
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test	0.5		$V_{DD} - 0.5$	V
Common-Mode Rejection Ratio	CMRR	$0.5\text{V} \leq V_{CM} \leq V_{DD} - 0.5\text{V}$	60	80		dB
Continuous Output Current	I_O	$V_{OUT} = 9.5\text{V}$ (Note 2)				mA
		MAX9650AZK+	20			
		MAX9650AUA+	80			
		$V_{DD} = 15\text{V}$, $V_{OUT} = 7.5\text{V}$				
		MAX9650ATA+		± 350		
Transient Peak Output Current	I_{PK}	(Note 3)		± 1.3		A
Bandwidth	BW	-3dB		35		MHz
Slew Rate	SR	4V step, $C_L = 50\text{pF}$, $R_L = 10\text{k}\Omega$, $A_V = +1\text{V/V}$		40		V/ μs
Settling Time	t_S	Settling to 0.1% of V_{OUT} , $I_L = 0$ to 1000mA , $R_S = 2.2\Omega$, $C_S = 0.1\mu\text{F}$ (Figure 1)		2.0		μs

MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 19V$, $V_{GND} = 0V$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Load Capacitance	C_{LOAD}	(Note 4)		150		nF
Noninverting Input Resistance	R_{IN+}	(Note 5)		100		$M\Omega$
Inverting Input Resistance	R_{IN-}	(Note 5)		100		$M\Omega$
Input Capacitance	C_{IN}			3		pF
Thermal Shutdown				+170		$^\circ C$
Thermal Shutdown Hysteresis				15		$^\circ C$

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

Note 2: Continuous output current is tested with one output at a time.

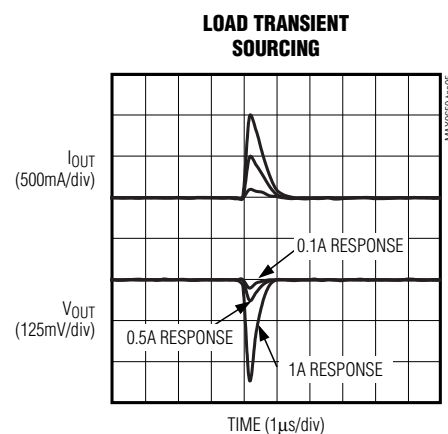
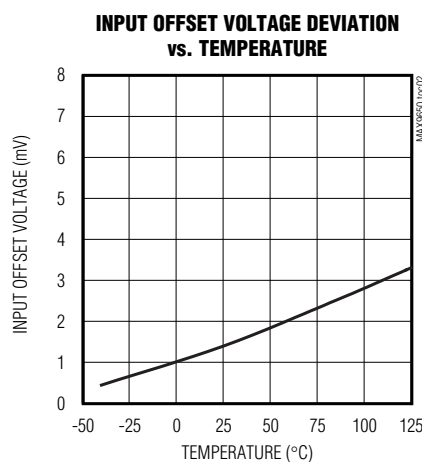
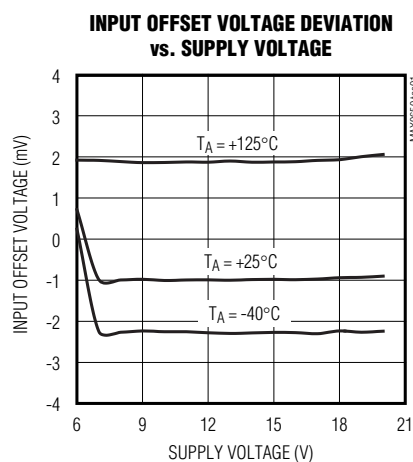
Note 3: See the *Thermal Shutdown with Temperature Hysteresis* section.

Note 4: A series resistor can extend load capacitance range. The settling time can be optimized by a small series resistance. See the *Applications Information* section for more information.

Note 5: Inputs are protected by back-to-back diodes.

Typical Operating Characteristics

($V_{DD} = 19V$, $GND = 0$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise specified.)

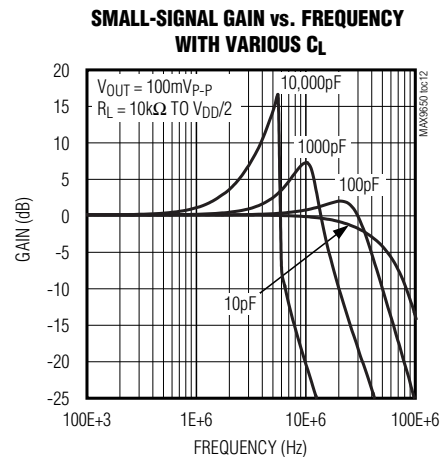
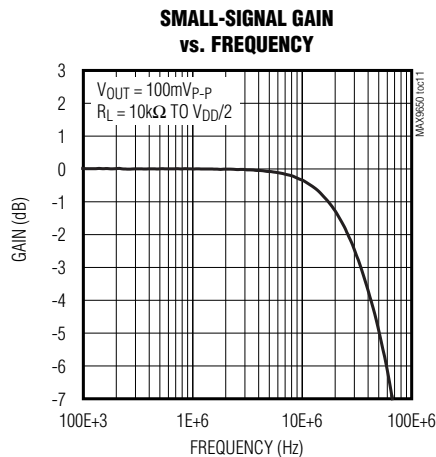
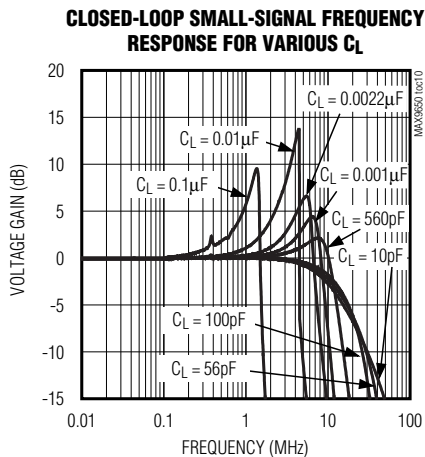
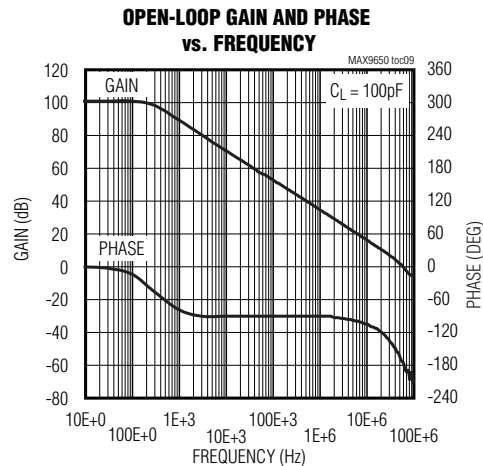
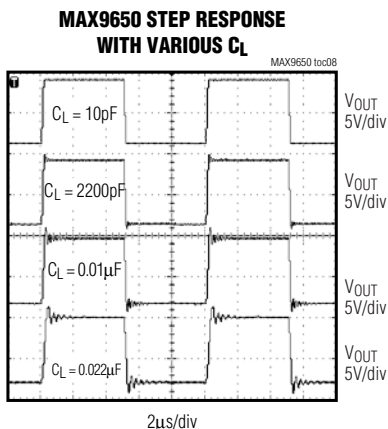
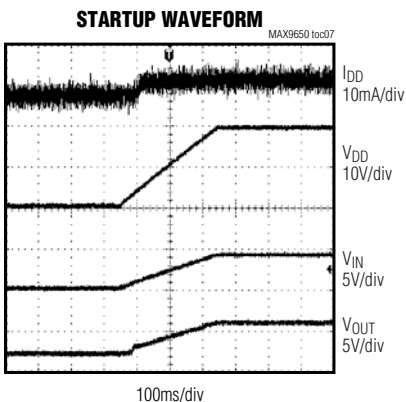
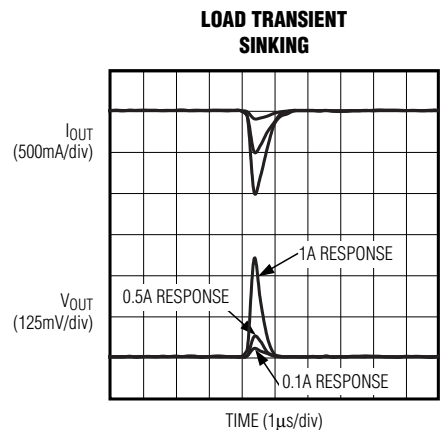
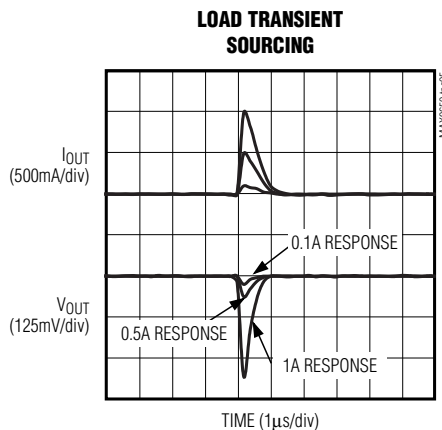
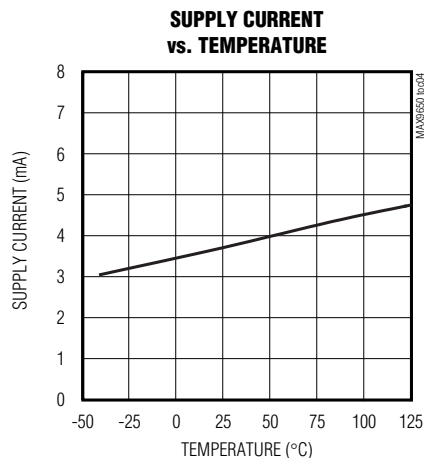


MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

Typical Operating Characteristics (continued)

($V_{DD} = 19V$, $GND = 0$, $V_{CM} = V_{OUT} = V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise specified.)



MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

Pin Description

PIN			NAME	FUNCTION
SOT23	MAX9650 μMAX-EP, TDFN-EP	MAX9651 (μMAX-EP, TDFN-EP)		
1	6	1	OUTA	VCOM Output A
2	4	4	GND	Ground
3	3	3	INA+	Positive Input A
4	2	2	INA-	Negative Input A
5	7	8	V _{DD}	Positive-Supply Input. Bypass V _{DD} to GND with a 0.1μF capacitor as close as possible to the device.
—	—	5	INB+	Positive Input B
—	—	6	INB-	Negative Input B
—	—	7	OUTB	VCOM Output B
—	1, 5, 8	—	N.C.	No Connection. Not internally connected.
—	—	—	EP	Exposed Pad (μMAX and TDFN Only). EP is internally connected to GND. Connect EP to GND.

Detailed Description

The MAX9650/MAX9651 operational rail-to-rail input/output amplifiers hold the VCOM voltage stable while providing the ability to source and sink a high current quickly (1.3A) into a capacitive load such as the backplane of a TFT-LCD panel.

Thermal Shutdown with Temperature Hysteresis

The MAX9650/MAX9651 are capable of high output currents and feature thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +170°C, the device shuts down. When the die cools down by 15°C, the device turns on again. In a TFT-LCD application, the duty cycle is very low. Even with high values of voltage and current, the power dissipation is low and the chip does not shut down.

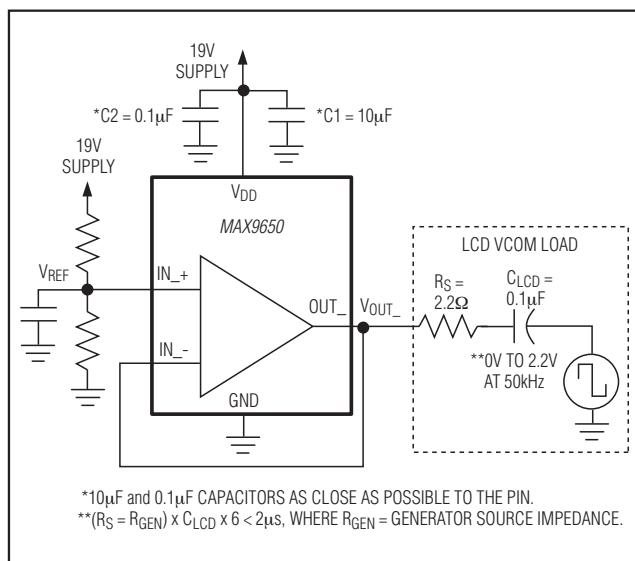


Figure 1. Settling Time Test Circuit

MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

Applications Information

Output Load

The MAX9650/MAX9651 are designed to drive capacitive loads. A small value of series resistance improves the performance of the device to ensure stability and fast settling with very large or very small capacitive loads. In many cases, this resistance is already present due to connection resistance in the wiring and no additional physical resistor is necessary. For minimum series resistance required for stability with capacitive loading, see Figure 2.

Power Supplies and Bypass Capacitors

The MAX9650/MAX9651 operate from a 6V to 20V single supply or from $\pm 4.5\text{V}$ to $\pm 10\text{V}$ dual supplies. Proper supply bypassing ensures stability while driving high

transient loads. The MAX9650/MAX9651 require a minimum $10\mu\text{F}$ (C1) and $0.1\mu\text{F}$ (C2) power-supply bypass capacitors placed as close as possible to the power-supply pin (V_{DD}). See Figure 3. For dual-supply operation, use $10\mu\text{F}$ and $0.1\mu\text{F}$ bypass capacitors on both supplies (V_{DD} and GND) with each capacitor placed as close as possible to V_{DD} and GND.

Layout and Grounding

The exposed pad on the $\mu\text{MAX}^{\circledR}$ and TDFN packages provide a low thermal resistance for heat dissipation. Solder the exposed pad to a ground plane for best thermal performance. Do not route traces under these packages. For dual-supply operation, the exposed pad (EP) can be electrically connected to the negative supply or it can be left unconnected.

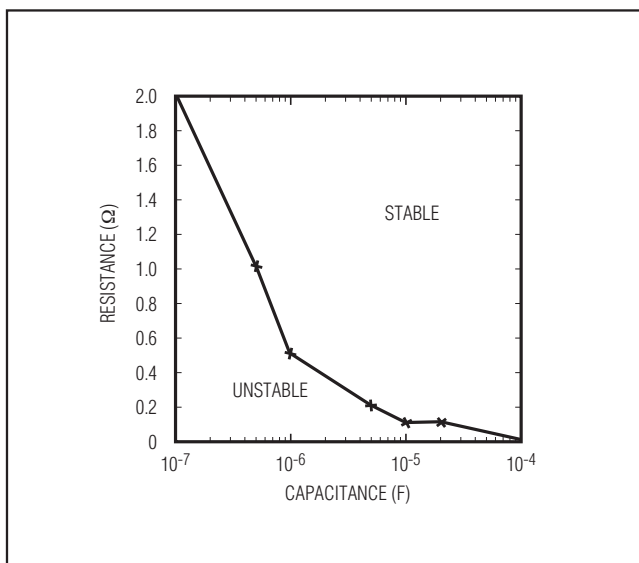


Figure 2. Minimum Combined ESR/Series/Trace Resistance Required for Stability of the MAX9650 in Response to Capacitive Loads

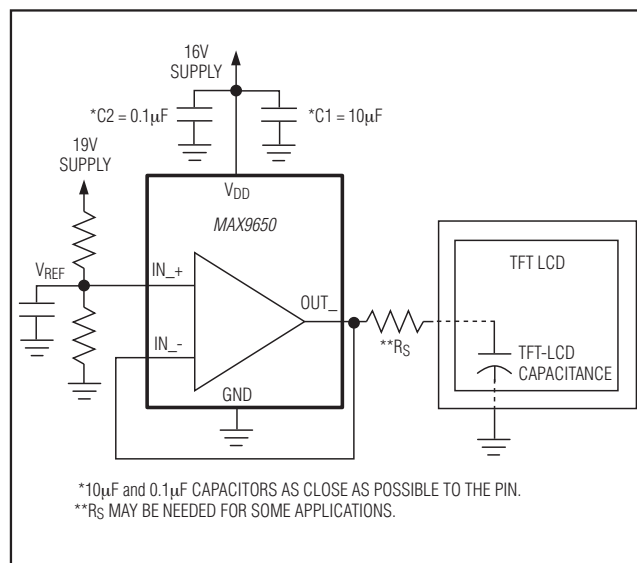


Figure 3. Typical TFT-LCD Backplane Drive Circuit

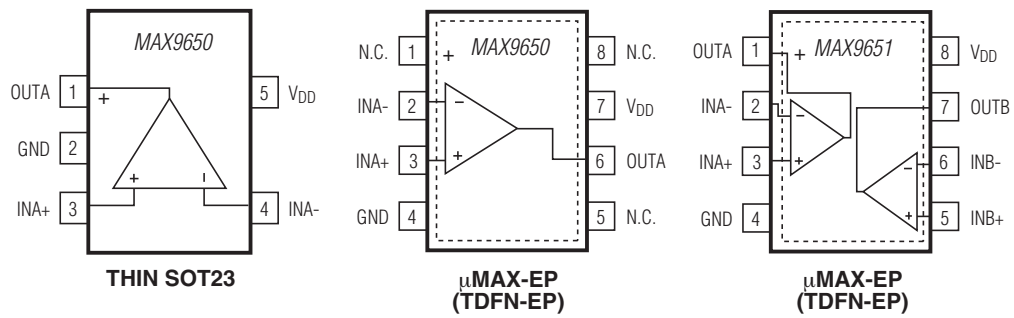
Chip Information

PROCESS: BiCMOS

MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

Pin Configurations



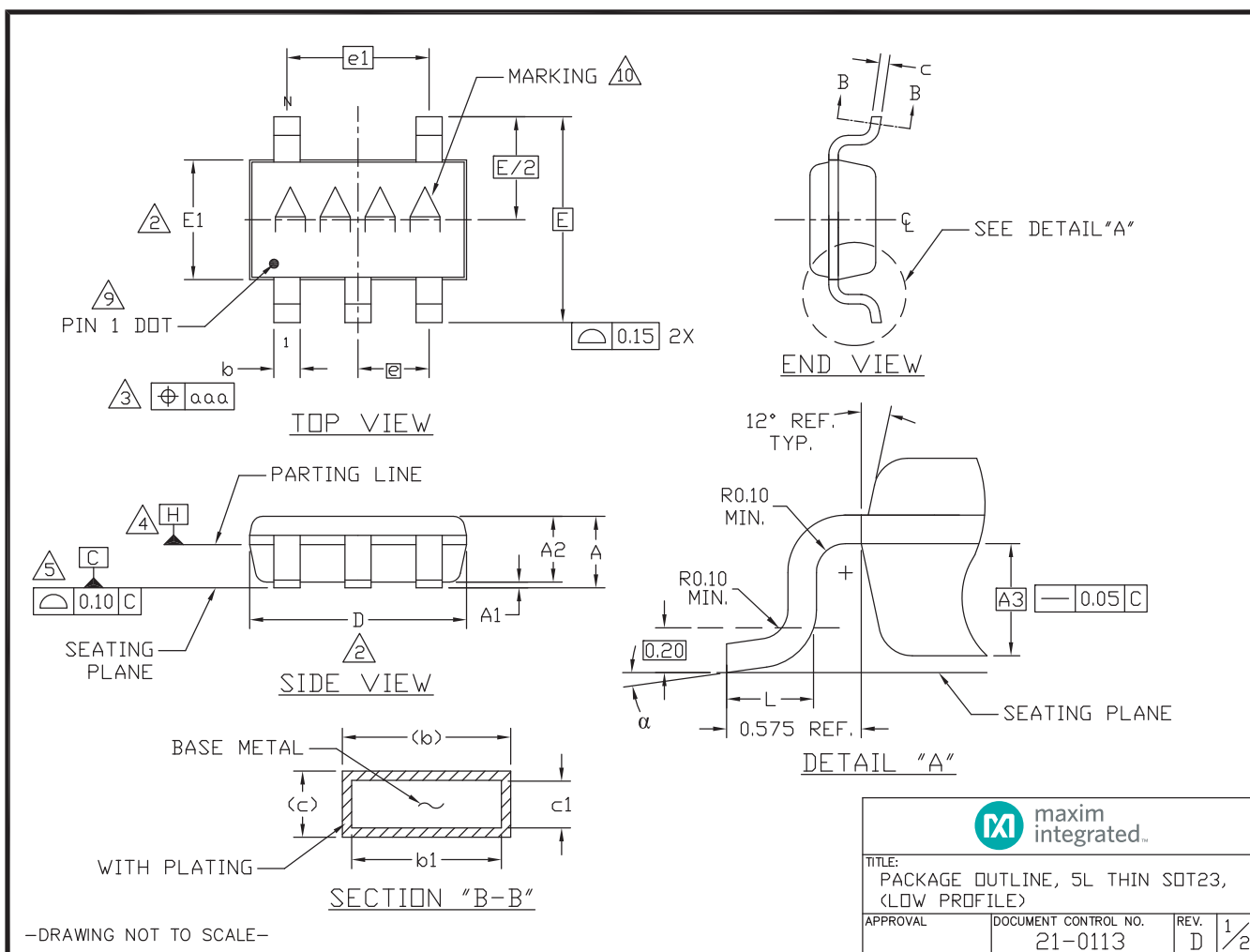
MAX9650/MAX9651

High-Current VCOM Drive Op Amps for TFT LCDs

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	Z5+2	21-0113	90-0241
8 μ MAX	U8E+2	21-0107	90-0145
8 TDFN-EP	T833+2	21-0137	90-0059



MAX9650/MAX9651

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Package Information (continued)

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.

2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.

3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

4. DATUM PLANE $\square\square$ LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.

5. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM $\square\square$ AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM $\square\square$ IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.

6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.

7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.

8. WARPAGE SHALL NOT EXCEED 0.10mm.

9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

11. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.

12. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

DIMENSIONS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3	0.50 BSC		
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E	2.75 BSC		
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1	1.90 BSC		
e	0.95 BSC		
α	0°	4°	8°
aaa	0.20		
PKG CODE	Z5-1, Z5-2, Z5-3		

-DRAWING NOT TO SCALE-



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(LOW PROFILE)

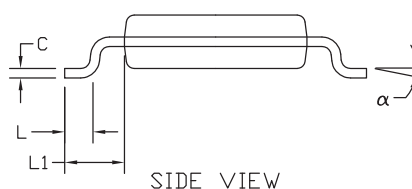
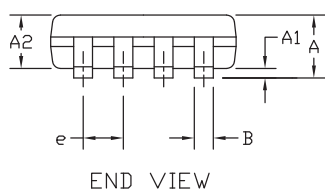
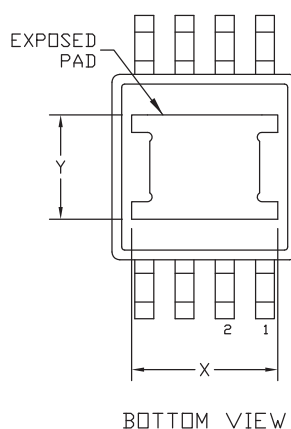
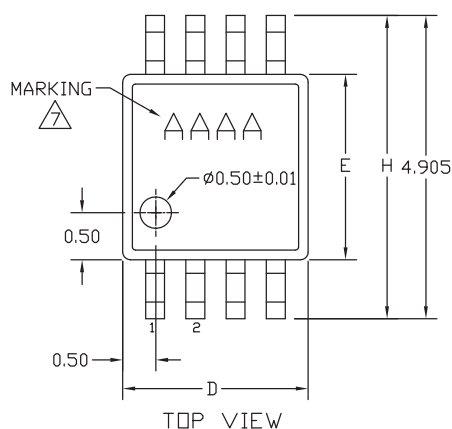
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MAX9650/MAX9651

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Package Information (continued)

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	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.043	0.940	1.100
A1	0.000	0.006	0.000	0.150
A2	0.030	0.037	0.750	0.950
B	0.010	0.014	0.250	0.360
C	0.005	0.007	0.130	0.180
D	0.116	0.120	2.950	3.050
e	0.0256	BSC	0.65	BSC
E	0.116	0.120	2.950	3.050
H	0.188	0.198	4.780	5.030
L	0.016	0.026	0.410	0.660
L1	0.037	REF.	0.940	REF.
α	0°	6°	0°	6°
X	0.087	0.099	2.210	2.515
Y	0.059	0.074	1.500	1.880

NOTES

1. DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
4. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006") PER SIDE.
5. MEETS JEDEC OUTLINE MO-187.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
8. COPLANARITY SHALL NOT EXCEED 0.10mm.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.
10. PKG CODE: UBE-2

-DRAWING NOT TO SCALE-



TITLE:
PACKAGE OUTLINE, 8L uMAX/uSQP,
3x3mm BODY, EXPOSED PAD

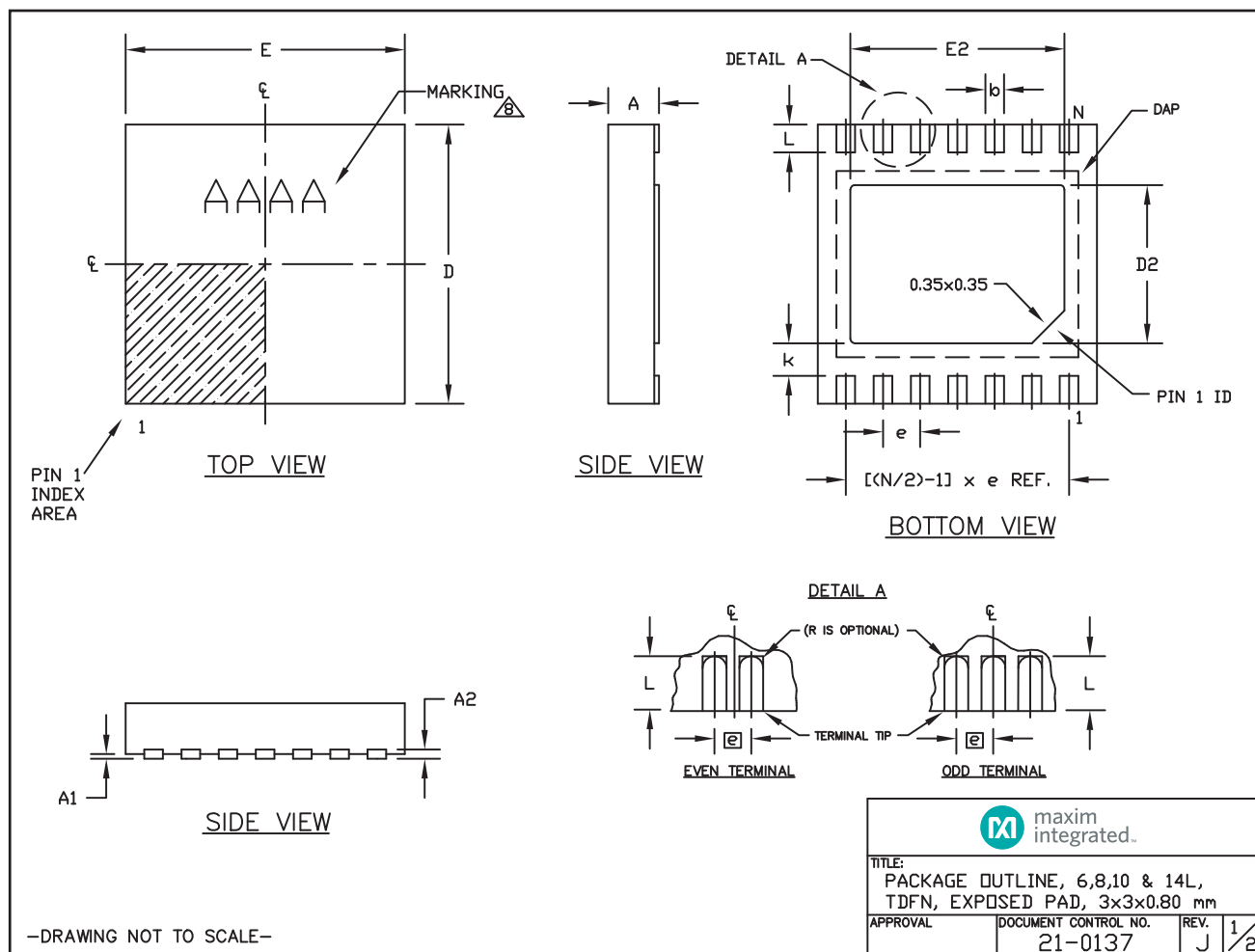
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Package Information (continued)

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COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

 maxim integrated.		
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0137	REV. J 2/2

DS1086L

3.3V Spread-Spectrum EconOscillator

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	10/08	Updated slew rate and added TDFN-EP package	1, 2, 6, 10, 11
2	5/09	Updated continuous output current specification	2
3	2/10	Added automotive part to <i>Ordering Information</i> , corrected units for input offset voltage, and added figure for minimum series resistance	1, 2, 5, 6
4	7/10	Removed extraneous information in the Electrical Characteristics table and corrected typo in TOC 5	2, 4
5	11/12	Corrected lead pattern number	8



Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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13