

Differential PECL Crystal Clock Oscillators [PECL Outputs]

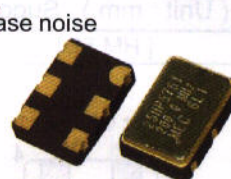
" HPF " series , F group characteristics

" HPW " series , W group characteristics

" HPA " series , A group characteristics



- HPA series (non-PLL) uses third overtone crystal to achieve ultra low jitter and phase noise
- HPF and HPW use high-Q fundamental crystal and low jitter multiplier circuit.
- HPA and HPF offer <1 ps phase jitter. "HPW" offers moderate jitter and low cost.



General Specifications

Model	" HPF " series		" HPW " series		" HPA " series	
Technology	High Q fundamental crystal + low jitter multiplier circuit		High Q fundamental crystal + multiplier circuit		Third overtone crystal (non-PLL)	
Output Logic	LVPECL					
Available Frequency Range	38.0 MHz ~ 640.0 MHz		750 KHz ~ 800.0 MHz		60.0 MHz ~ 320.0 MHz	
Supply Voltage V _{DD}	+2.5 V _{DD} ± 5%	+3.3 V _{DD} ± 5%	+3.3 V _{DD} ± 5%		+2.5 V _{DD} ± 5%	+3.3 V _{DD} ± 5%
Supply Voltage Code	" 25 "	" 3 "	" 3 "		" 25 "	" 3 "
Output Logic " High " , " 1 "	V _{DD} -1.025 min. Termination: R _L =50 Ω to (V _{DD} -2.0V). See test circuit below.					
Output Logic " Low " , " 0 "	V _{DD} -1.620 max. Termination: R _L =50 Ω to (V _{DD} -2.0V). See test circuit below.					
Integrated Phase Jitter (12 KHz to 20 MHz)	0.4 ps typical; 0.5 ps max. For 156.250 MHz		2.6 ps typical; 4 ps max. For 155.520 MHz		0.25 ps typical; 4 ps max. For 155.520 MHz	
Period Jitter RMS ; Decoupling capacitor between V _{DD} and ground	3 ps typical ; 5 ps max. For 156.250 MHz		4.3 ps typical. For 155.520 MHz		2.5 ps typical. For 155.520 MHz	
Period Jitter (peak-to-peak ; Decoupling capacitor between V _{DD} and ground)	20 ps typical ; 30 ps max. For 156.250 MHz		27 ps typical. For 155.520 MHz		21 ps typical. For 155.520 MHz	
Current Consumption (15 pF load)	38 MHz ~ 100 MHz: 65 mA max 100.01 MHz ~ 320 MHz: 80 mA max. 320.01 MHz ~ 640 MHz: 90 mA		< 24 MHz: 25 mA max 24.01 MHz ~ 96 MHz: 65 mA max. 96.01 MHz~700 MHz: 100 mA		75 mA max. for 212.5 MHz	
Rise Time / Fall Time	0.4 ns typical , 0.55 ns max. (20%↔80% of the PECL wave form)		0.6 ns typical , 1.5 ns max. (20%↔80% of the PECL wave form)		0.4 ns typical , 0.7 ns max. (20%↔80% of the PECL wave form)	
Frequency Stability ⁽¹⁾ Codes	Frequency Stability over Operating Temperature Range		± 25 ppm	± 50 ppm	± 100 ppm	If non-standard please enter the desired stability after the " C " or " I " represents (e.g. "C20" ±20 ppm over 0°C to +70°C ; " I20 " represents ± 20 ppm over -40°C to +85°C)
	Commercial (-10°C to +70°C)		A	B	C	
	Industrial (-40°C to +85°C)		D	E	F	
Load	R _L =50 Ω to (V _{DD} -2.0V). See test circuit below.					
Start-up Time	10 m sec. (max.)					
Duty Cycle	50% ± 5% (measured at V _{DD} -1.3V)					
Input Static Discharge Protection	2 KV (min.)					
Storage Temperature	-55°C to + 150°C					
Aging at Ta = +25°C	± 3 ppm max. first year ; ± 2 ppm max. per year thereafter					
Supply Voltage V _{DD}	+ 4.6 V D.C. (max.)					
Input Voltage Vi	V _{SS} -0.5 (min.) ; V _{DD} + 0.5V (max.)					
Input Voltage Vo	V _{SS} -0.5 (min.) ; V _{DD} + 0.5V (max.)					
Absolute Maximum Rating (permanent damage may be created if operate beyond limits specified.)						
Tri - State Function. 5761 on pad No. 1 5762 on pad No. 2	No Connection	Differential PECL and complimentary PECL outputs .				
	Disable	Both outputs are disabled (high impedance) when the Tri-state pad taken below 0.45*Vcc referenced to ground (threshold) Oscillator is always On . Only buffer stage is disabled . Disable current : 50 uA max. (at 0.0V) , Disable time : 10 ns (max.)				
	Enable	At disabled mode , both outputs are enabled when Tri-state pad is taken above 0.45*Vcc referenced to ground (threshold) ; Enable time : 10ns + one period of the output frequency (max.)				
SSB Phase Noise (dBc / Hz)	Offset	Frequency: 156.250 MHz	Frequency: 155.520 MHz		Frequency: 212.500 MHz	
	10 Hz	-62 dBc / Hz	-62 dBc / Hz		-72 dBc / Hz	
	100 Hz	-92 dBc / Hz	-95 dBc / Hz		-100 dBc / Hz	
	1 KHz	-120 dBc / Hz	-120 dBc / Hz		-130 dBc / Hz	
	10 KHz	-132 dBc / Hz	-125 dBc / Hz		-140 dBc / Hz	
	100 KHz	-128 dBc / Hz	-121 dBc / Hz		-142 dBc / Hz	
	1 MHz	-140 dBc / Hz	-120 dBc / Hz		-147 dBc / Hz	
	10 MHz	-150 dBc / Hz	-140 dBc / Hz		-150 dBc / Hz	

⁽¹⁾ Inclusive of 25°C tolerance, operating temperature range, $\pm 10\%$ input voltage variation, load change, aging shock and vibration

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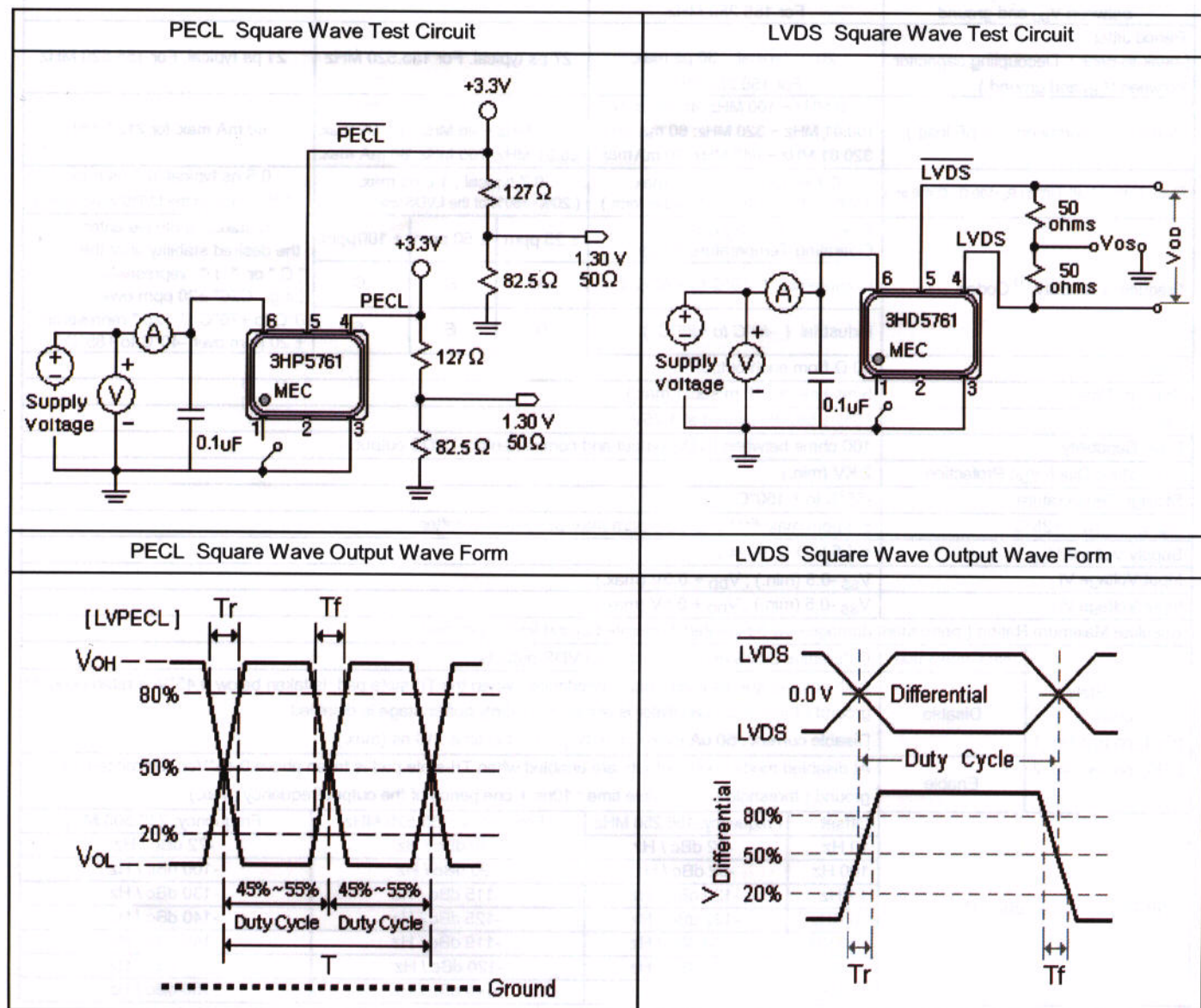
Part Number Format and Examples :

[1]	[2]	[3]	[4]	[5]	[6]
Voltage	Type 1 Type 2	G ---	Stability ---	Frequency ---	Customer spec.

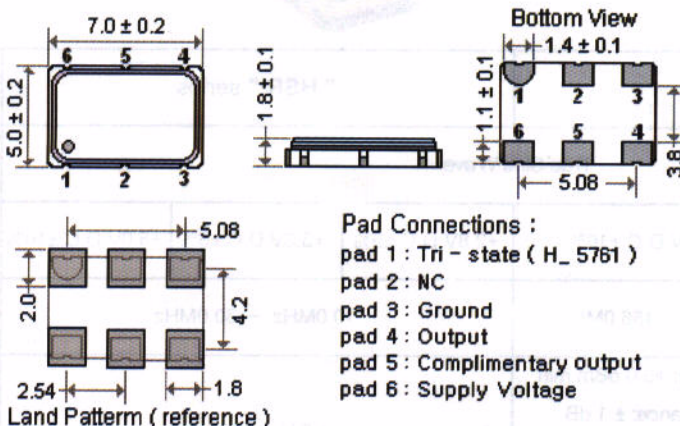
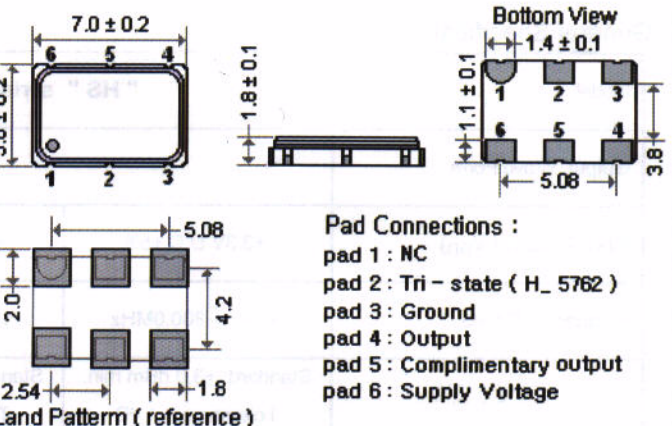
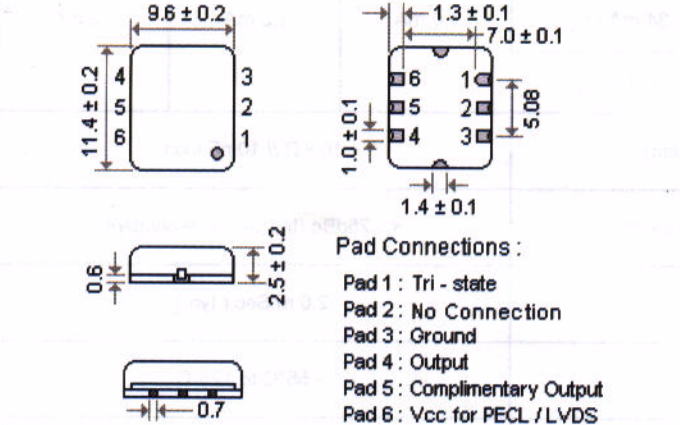
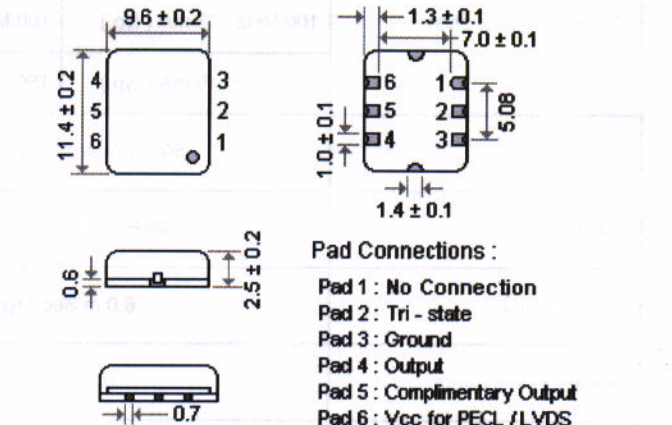
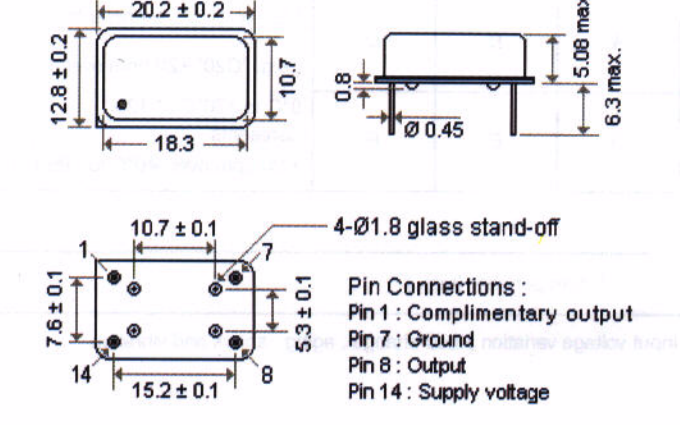
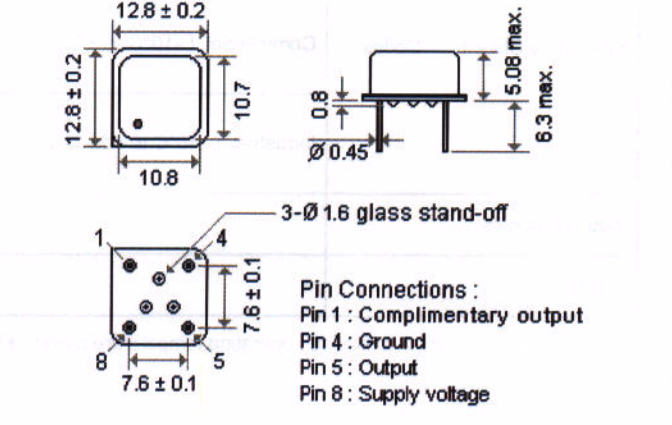
[1]	Supply voltage , " 25 " for +2.5V , " 3 " for +3.3V
[2]	" 1 " : Tri-state function on pad # 1 , " 2 " : Tri-state function on pad # 2
[3]	Please add " G " after the " type code " for RoHS compliance (H_576_ series are not included)
[4]	Frequency Stability Code: Please see previous page [Frequency Stability ⁽¹⁾]
[5]	Frequency in MHz
[6]	Assigned by Mercury if custom spec

Ex (1) : 3HPA5762 - A - 100.000 represents +3.3V input voltage , LVPECL output wave , group A Characteristics , 100.000MHz
7.0*5.0*1.8mm package, 6 pads SMD type ,Tri-state function on pad # 2 , ± 25 ppm from -10°C to 70°C ,

Ex (2) : 3HDW621G - E - 200.000 represents +3.3V input voltage , LVDS output wave , group W Characteristics , 200.000MHz , RoHS ,
11.4*9.6*2.5mm package, 6 pads SMD type ,Tri-state function on pad # 1 , ± 50 ppm from -40°C to 85°C ,



Outline Dimensions (Unit : mm) , Suggested Pad Layout

[HPF5761 , HPW5761 , HPA5761] , [HDF5761 , HDW5761 , HDA5761]  Bottom View Pad Connections : pad 1 : Tri - state (H_ 5761) pad 2 : NC pad 3 : Ground pad 4 : Output pad 5 : Complimentary output pad 6 : Supply Voltage Land Pattern (reference)	[HPF5762 , HPW5762 , HPA5762] , [HDF5762 , HDW5762 , HDA5762]  Bottom View Pad Connections : pad 1 : NC pad 2 : Tri - state (H_ 5762) pad 3 : Ground pad 4 : Output pad 5 : Complimentary output pad 6 : Supply Voltage Land Pattern (reference)
[HPF621 , HPW621 , HPA621] , [HDF621 , HDW621 , HDA621]  Bottom View Pad Connections : Pad 1 : Tri - state Pad 2 : No Connection Pad 3 : Ground Pad 4 : Output Pad 5 : Complimentary Output Pad 6 : Vcc for PECL / LVDS	[HPF622 , HPW622 , HPA622] , [HDF622 , HDW622 , HDA622]  Bottom View Pad Connections : Pad 1 : No Connection Pad 2 : Tri - state Pad 3 : Ground Pad 4 : Output Pad 5 : Complimentary Output Pad 6 : Vcc for PECL / LVDS
[HPF14 , HPW14 , HPA14] , [HDF14 , HDW14 , HDA14]  Bottom View Pin Connections : Pin 1 : Complimentary output Pin 7 : Ground Pin 8 : Output Pin 14 : Supply voltage	[HPF8 , HPW8 , HPA8] , [HDF8 , HDW8 , HDA8]  Bottom View Pin Connections : Pin 1 : Complimentary output Pin 4 : Ground Pin 5 : Output Pin 8 : Supply voltage