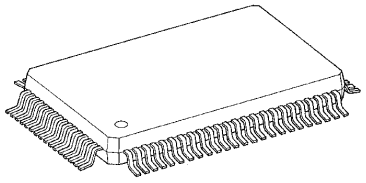
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9323F

SINGLE-CHIP DTS MICROCONTROLLER (DTS-20)

The TC9323F is a 4-bit CMOS microcontroller for single-chip digital tuning systems, containing prescalers operating at frequencies up to 150MHz, a PLL, and an LCD driver.
The CPU provides 4-bit parallel addition and subtraction instructions (such as AI and SI), logic operation instructions (such as OR and AN), and multi-bit judgment and comparison instructions (such as TM and SL), plus timebase functions.
The package is an 80-pin miniflat package, with a large number of I/O ports and key input ports that are controlled by a powerful I/O instructions (IN1 to 3, OUT1 to 3).
Other numerous features that recommend the TC9323F for use digital tuning systems include interrupt handling facilities, a buzzer, 6-bit A/D and D/A converters, a serial interface, and an IF counter.



QFP80-P-1420-0.80A

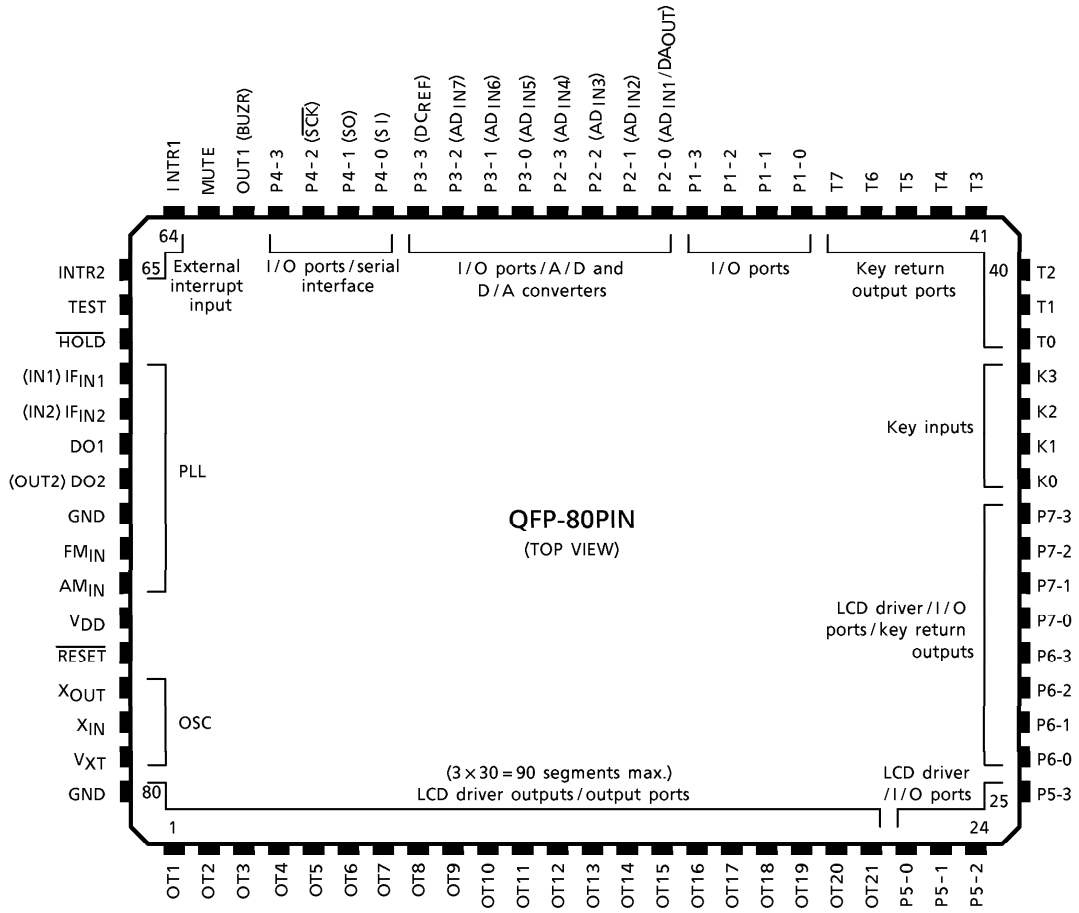
Weight : 1.57g (Typ.)

FEATURES

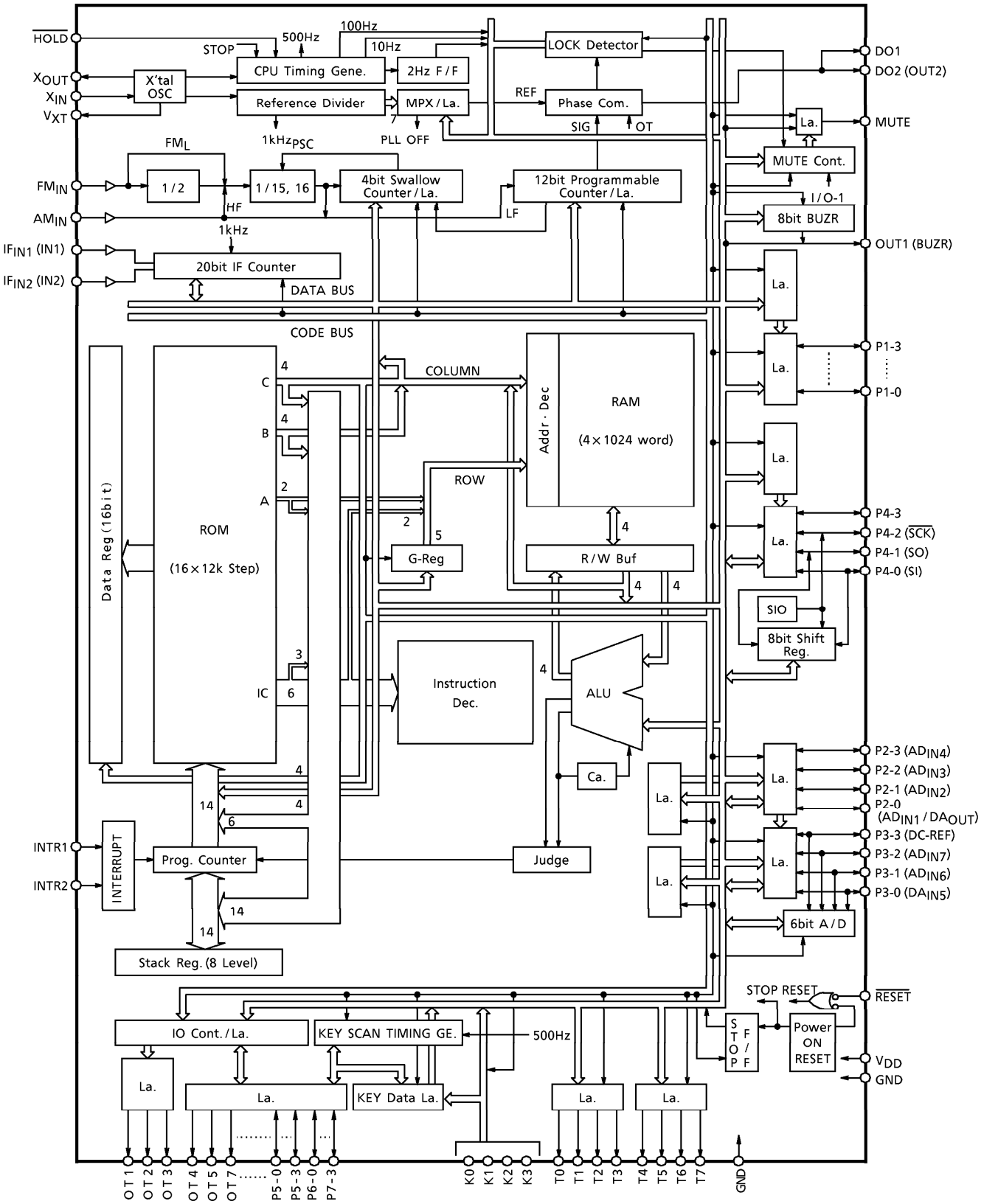
- 4-bit microcontroller for single-chip digital tuning systems
- Operating supply voltage V_{DD} = 4.5 to 5.5V, operating temperature range Ta = −40 to 85°C, CMOS structure for low-power consumption
- Built-in prescalers (1/2 fixed divider +2 modular prescalers : fmax ≧ 150MHz)
- Data memory (RAM), easing port backups
- Program memory (ROM) : 16 bits × 12,288 steps
- Data memory : 4 bits × 1,024 words

- Powerful repertoire of 57 different instructions (all single-word instructions)
- Instruction execution time : 1.78μs (connected to a 4.5MHz crystal oscillator) and 3.56μs (MVGS and DAL instructions only)
- Numerous addition and subtraction instructions (4 different addition instructions and another 4 different subtraction instructions)
- Powerful complex decision instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Instruction for transmitting data between addresses on the same row address (MVSR)
- Register-to-register indirect transfer instructions (MVGD, MVGS)
- 16 powerful general registers (located in RAM)
- Stack level : 8
- Program memory (ROM) free from page and field concepts, allowing unrestricted branches within 12,288 steps (JUMP instruction)
- Free reference to the 16-bit contents of any address in 1,024 steps in program memory (ROM)
- Built-in 20-bit general-purpose IF counter, counting intermediate frequencies over each band to detect broadcasting stations during auto-tuning
- Independent frequency input pins (FM_{IN}, AM_{IN}) for FM and AM, and two phase comparator outputs (DO1, DO2)
- Program-selectable 11 different reference frequencies
- Program-selectable between pulse swallow and direct demultiplication methods to suit reception bands
- IF correction over the FM band (IF offset internal port)
- Built-in powerful serial interface facilities
- Powerful I/O instructions (IN1 to 3, OUT1 to 3)
- Input-only ports (K0 to K3) dedicated to key inputs
- 59 I/O ports (including 28 that are programmable as input or output bit by bit, and 31 output-only ports). Programming allows $IF_{IN1/2}$ and DO2 to used as IN1/2 (input-only ports) and OUT2 (output-only port), respectively. OT1-OT21 ports are build in the increment function for external memory access.
- Built-in interrupt handling facilities implemented by 2 external interrupt input pins, an 8-bit timer, and a serial interface
- Dedicated interrupt instructions (RNI, EI, DI)
- Instruction-set backup mode (CPU operation, crystal oscillation only, oscillation stop)
- Built-in 2Hz timer F/F and 10/100/500Hz interval pulse output (timebase internal support)
- PLL lock detection (PLL lock detection internal port)
- Built-in buzzer output circuit selectable from combinations of four different output modes and eight different frequencies
- Built-in 7-channel 6-bit A/D converter and 1-channel 6-bit D/A converter
- OTP product : TC93P23F

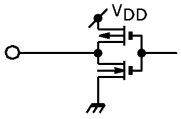
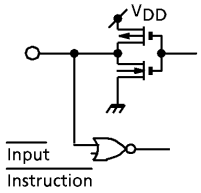
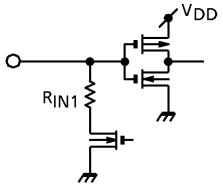
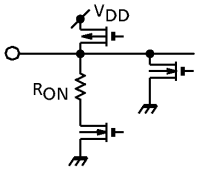
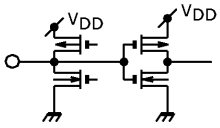
PIN ASSIGNMENT

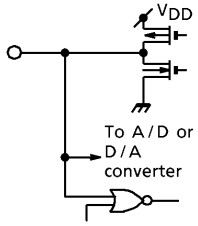
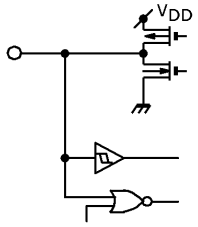


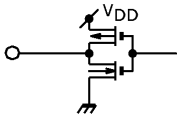
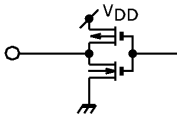
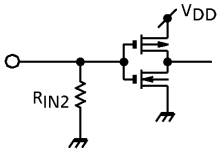
BLOCK DIAGRAM

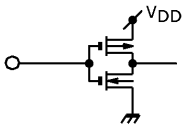


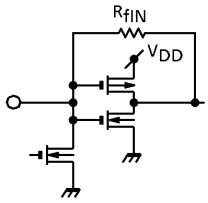
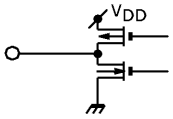
DESCRIPTION OF PIN FUNCTION

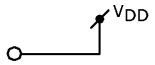
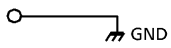
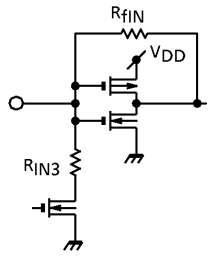
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1~21	OT1 ~ OT21	General-purpose outputs	21-bit output ports. These ports are built-in the increment function. These ports are able to use as the address signal for external memory.	
22~33	P5-0 ~ P7-3	General-purpose I/O ports	12-bit (P5-0~P7-3) I/O ports. I/O designation for every bit can be made for these ports.	
34~37	K0~K3	Key input ports	Key matrix input 4-bit input ports, which permit maximum data input of 4×8=32 keys in combination with the key return timing outputs (KR0 to KR7). A pull-down resistor is built in. A key matrix can also be composed in combination with the key timing output ports (T0 to T7).	
38~45	T0~T7	Key timing output ports	Key matrix timing signal output ports. A load resistor is built in N-ch to form a key matrix, saving a matrix diode when push keys are connected to these ports.	
46~49	P1-0~P1-3	I/O ports 1	4-bit I/O ports. Programmable as input or output bit by bit.	

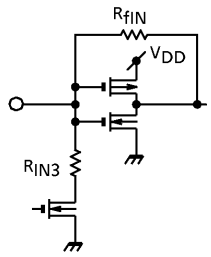
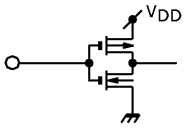
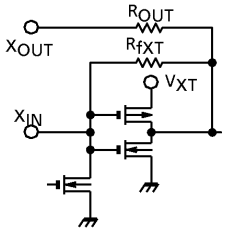
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
50~57	P2-0 / AD_{IN1} / DA_{OUT} P2-1 / AD_{IN2} ~ P2-3 / AD_{IN4} P3-0 / AD_{IN5} ~ P3-2 / AD_{IN7} P3-3 / DC_{REF}	I/O port 2/A/D analog voltage input/D/A analog voltage output I/O port 2/A/D analog voltage input I/O port 3/A/D analog voltage input I/O port 3/ reference voltage input	8-bit I/O ports. Programmable as input or output bit by bit. Pins P2-0 to P3-2 serve as analog I/O to and from the built-in 6-bit A/D or D/A converter. Running on a principle of software-controlled successive approximation, the built-in A/D converter permits required pins to be programmed as A/D or D/A analog I/O bit by bit. P3-3 is programmable as reference voltage input. Further, a reference voltage can be derived from the internal power supply (V_{DD}). The D/A converter generates an analog voltage through an operational amplifier by sharing the circuit used by the A/D converter for generating a comparative voltage. When the D/A converter is used concurrently with the A/D converter, its output is set in a high-impedance state by programming at A/D conversion to use it on a time-division basis. An analog voltage holding capacitor must be connected to the D/A output pins at this time. The A/D and D/A converters and all these controls are implemented by programming.	 Input instruction
58~61	P4-0 / SI P4-1 / SO P4-0 / $\overline{SCK}$ P4-3	I/O port 4 /Serial data input /Serial data output /Serial clock I/O I/O port 4	4-bit I/O ports. Programmable as input or output bit by bit. Pins P4-0 to P4-2 serve as I/O to and from the serial interface circuit (SI0). SIO produces serial output of 4- or 8-bit data on the SI pin at edges of the clock on the $\overline{SCK}$ pin. The serial operation clock ($\overline{SCK}$) is selectable between internal and external and between leading and trailing shifts. The SO pin can be switched to serial input (SI) to facilitate the jobs of controlling various LSIs and communicating between controllers. All inputs to SIO contain a Schmidt circuit. SIO and all its controls are programmable.	 Input instruction

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
62	OUT1 / BUZR	General-purpose port / Buzzer output	1-bit output port, which serves as built-in buzzer output. Buzzer output can be used to produce an acknowledgment tone at key operation or in the tuning scan mode or an alarm beep. The kind of buzzer is selectable from combinations of four different output modes and eight different frequencies.	
63	MUTE	Muting output port	1-bit output port. Normally, it is used as muting control signal output. The internal MUTE bit can be set to 1 by using changes in the I / O port "1" input. MUTE bit output logic change and PLL phase difference output are possible.	
64 65	INTR1 INTR2	External interrupt inputs	External interrupt input pins, which can be used, for example, as remote control signal input. Programmable as general-purpose input ports.	
66	TEST	Test mode control input	Test mode control input pin. A "H" on this pin enables the test mode. A "L" enables a normal operation. It is normally used at the low level or in an NC state (with a built-in pulldown resistor).	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
67	$\overline{\text{HOLD}}$	Hold mode control input	Input pin to select or clear the hold state. Normally, it is used as radio mode selection signal input or battery detection signal input. The hold state is divided into the clock stop mode (crystal oscillation stop) and the wait mode (CPU stop). This setting is entered by executing the CKSTP or WAIT instruction. When the CKSTP instruction is executed, the hold state is requested or cleared depending on the status of the internal MODE bit. When the MODE bit is "0" (MODE-0), the CPU stops and enters the memory backup state if the CKSTP instruction is executed while there is a low on the HOLD pin. When the MODE bit is "1" (MODE-1), the CPU enters the memory backup state if the CKSTP instruction is executed, regardless of whether the $\overline{\text{HOLD}}$ pin is high or low. This state is cleared when a low to high transition occurs on the $\overline{\text{HOLD}}$ pin in MODE-0 or when a change in the input to the $\overline{\text{HOLD}}$ pin occurs in MODE-1. The hold state that has been set by executing the WAIT instruction is cleared by a change in the input to the $\overline{\text{HOLD}}$ pin. In the memory backup state, all output pins (including display output and output ports) enters a low level automatically for lower-power dissipation (1μA or lower).	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
68 69	IF_{IN1} / IN1 IF_{IN2} / IN2	IF signal inputs / Input ports	IF signal inputs to an IF counter that counts occurrences of the FM or AM band IF signal to detect an auto-stop. With input frequencies of 0.3 to 12MHz ($0.2V_{p-p}$ min), the IF signal input pins contain an input amplifier, operating with a C-coupling low amplitude. The 20-bit IF counter offers a choice of four gating times – 1, 4, 16, and 64ms. The 20-bit data can be directly loaded into memory. Programming allows these input pins to be used as input ports (IN ports). The input pins receive CMOS input when used as IN ports.	
70 71	DO1 DO2 / OUT2	Phase comparator output Phase comparator output / Output port	PLL phase comparator output pins. Tristate output. If the divider output of the programmable counter is higher than the reference frequency, a high is output; if lower, a low is output ; and if equal, the pins enter a high-impedance state. As DO1 and DO2 are output in parallel, a filter constant can be optimized for each of the FM or AM bands. Further, programming allows the DO2 pin to be set in a high-impedance state or to be used as an output port (OUT2). Thus, using the two pins of DO1 and DO2 helps improve the lockup time or allows effective pin utilization.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
75	V_{DD}	Power input pins	Power input pins, to which V_{DD} = 4.5 to 5.5 is input. In the memory backup state (CKSTP instruction executed), the supply voltage can be reduced to 2.0V. The CPU can be stopped if the supply voltage falls to 2.6V or below to prevent it from malfunctioning (stop mode). The CPU restarts when the supply voltage rises above 3.5V. To enable the stop mode, set all the four bits of the internal test ports to 1. Set all to 0 to disable the stop mode (Initial condition). The entry of the CPU into the stop mode can be determined by referencing the STOP F/F bit. Initialize the CPU or correct the clock by programming as needed. When the input voltage to this pin rises from 0V to above 4.5V, a device system reset occurs, causing the program to start running at address 0 (power-on reset). (Note) Limit the device supply voltage rise duration to a range of 10 to 100ms to allow a power-on reset action to take place.	
72 80	GND			
73	FM_{IN}	FM local oscillator signal input	Programmable counter input pin for the FM band. Program-selectable between the 1/2 pulse swallow method (FMH mode) and the pulse swallow method (FML mode). In the FM mode, the input pin receives local oscillator output (VCO output) in a range of 10 to 150MHz ($0.2V_{p-p}$ min). It contains an input amplifier, operating with a C-coupling low amplitude. (Note) In the PLL off mode or when AM_{IN} input is set, the input is pulled down.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
74	AM_{IN}	AM local oscillator signal input	Programmable counter input pin for the AM band. Program-selectable between the pulse swallow method (HF mode) and the direct dividing method (LF mode). The input pin receives local oscillator output (VCO output) in a range of 0.5 to 60MHz ($0.2V_{p-p}$ min) in the HF mode or that in a range of 0.5 to 20MHz ($0.2V_{p-p}$ min) in the LF mode. (Note) In the PLL off mode or when FM_{IN} input is set, the input is pulled down.	
76	$\overline{RESET}$	Reset input	Device system reset signal input pin. A reset occurs while a low exists on $\overline{RESET}$. A low to high transition on $\overline{RESET}$ causes the program to start running at address 0. Since a system reset will normally occur when the input voltage to V_{DD} rises from 0V to above 4.5V (power-on reset), keep a "H" on this pin.	
77	X_{OUT}	Crystal oscillator pins	Crystal oscillator pins. Connect a reference 4.5MHz crystal oscillator to the X_{IN} and X_{OUT} pins. Oscillation stops while the CKSTP instruction is being executed. The V_{XT} pin is a crystal oscillator power supply. Connect a stabilization capacitor (0.47μF standard) to it.	
78	X_{IN}			
79	V_{XT}			

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Consumption	P_D	400	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−65~150	°C

ELECTRICAL CHARACTERISTICS (Ta = −40 to 85°C, V_{DD} = 4.5 to 5.5V, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Range Of Operating Supply Voltage	V_{DD1}	—	PLL, CPU operation	4.5	~	5.5	V
Range Of Operating Supply Voltage	V_{DD2}	—	PLL stop, CPU operation	3.5	~	5.5	
Range Of Memory Retention Voltage	V_{HD}	—	Crystal oscillation stopped (when the CKSTP instruction is executed)	2.0	~	5.5	
Operating Supply Current	I_{DD1}	—	Normal operation, no output load, V_{DD} = 5V, Ta = 25°C FM_{IN} = 150MHz input	—	8.0	20	mA
	I_{DD2}	—	Only CPU running, V_{DD} = 5V, Ta = 25°C (PLL off, display lit)	—	1	2	
	I_{DD3}	—	Standby mode, V_{DD} = 5V, Ta = 25°C (PLL off, crystal oscillation only)	—	0.2	0.4	
Memory Retention Current	I_{HD}	—	Crystal oscillation stopped (when the CKSTP instruction is executed)	—	0.1	10	μA
Crystal Oscillation Frequency	f_{XT}	—	V_{DD} = 4.5~5.5V	—	4.5	—	MHz

Programmable Counter and IF Counter Operating Frequency Ranges

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
FM_{IN}	f_{FM}	—	V_{DD} = 4.5~5.5V V_{IN} = 0.2V_{p-p} input	10	~	150	MHz
AM_{IN} (HF mode)	f_{HF}	—	V_{DD} = 4.5~5.5V V_{IN} = 0.2V_{p-p} input	0.5	~	60	
AM_{IN} (LF mode)	f_{LF}	—	V_{DD} = 4.5~5.5V V_{IN} = 0.2V_{p-p} input	0.5	~	20	
IF_{IN1}, IF_{IN2}	f_{IF}	—	V_{DD} = 4.5~5.5V V_{IN} = 0.2V_{p-p} input	0.3	~	12	

Programmable Counter and IF Counter Input Amplitude Ranges

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
FM_{IN}	f_{FM}	—	f_{IN} = 10 to 150MHz input V_{DD} = 4.5~5.5V	0.2	~	V_{DD} – 0.5	V_{p-p}
AM_{IN} (HF mode)	f_{HF}	—	f_{IN} = 0.5 to 60MHz input V_{DD} = 4.5~5.5V	0.2	~	V_{DD} – 0.5	
AM_{IN} (LF mode)	f_{LF}	—	f_{IN} = 0.5 to 20MHz input V_{DD} = 4.5~5.5V	0.2	~	V_{DD} – 0.5	
IF_{IN1}, IF_{IN2}	f_{IF}	—	f_{IN} = 0.3 to 12MHz input V_{DD} = 4.5~5.5V	0.2	~	V_{DD} – 0.5	

General-Purpose Outputs (OT1 to OT21)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current	"H" Level	I_{OH2}	—	V_{LCD} = 5V, V_{OH} = 4.5V	– 0.5	– 1.0	—	mA
	"L" Level	I_{OL2}	—	V_{LCD} = 5V, V_{OH} = 0.5V	0.5	1.0	—	

Key Input Ports (K0 to K3)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH1}	—	—	V_{DD} × 0.6	~	V_{DD}	V
	"L" Level	V_{IL1}	—	—	0	~	V_{DD} × 0.2	
Input Pulldown Resistance		R_{IN1}	—	—	50	100	200	kΩ

Key Return Output Input Ports (T0 to T7)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current	"H" Level	I_{OH1}	—	V_{DD} = 5V, V_{OH} = 4.5V	− 1.0	− 2.0	—	mA
N-ch Load Resistance		I_{LI}	—	V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V	50	100	200	kΩ

$\overline{HOLD}$ Input Port

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Leak Current		I_{LI}	—	V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH3}	—	—	V_{DD} × 0.8	~	V_{DD}	V
	"L" Level	V_{IL3}	—	—	0	~	V_{DD} × 0.4	

A / D Converter (AD_{IN1} to AD_{IN7}, DC-REF)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Input Voltage Range	V_{AD}	—	AD_{IN} to AD_{IN7}	0	~	V_{DD}	V
Analog Reference Voltage Range	V_{REF}	—	DC-REF	2.0	~	V_{DD}	V
Resolution	V_{RES}	—	—	—	6	—	bit
Overall Conversion Error	—	—	—	—	± 2.0	± 3.0	LSB
Analog Input Leak Current	I_{LI}	—	V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V (AD_{IN} to AD_{IN7})	—	—	± 1.0	μA
Analog Reference Input Current	I_{REF}	—	V_{DD} = 5V, V_{IH} = 5V (DC-REF)	—	0.5	1.0	mA
Analog Output Voltage Range	V_{DA0}	—	DA OUT	0	—	V_{DD} − 1.0	V
Analog Output Voltage Fluctuation	V_{DA}	—	I_{DA} = ± 100μA, V_{DD} = 5V, Ta = 25°C	—	± 50	± 100	mV

DO1, DO2, MUTE, OUT1 and OUT2 Outputs

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current	"H" Level	I_{OH1}	—	V_{DD} = 5V, V_{OH} = 4.5V	− 1.0	− 2.0	—	mA
	"L" Level	I_{OL1}	—	V_{DD} = 5V, V_{OL} = 0.5V	1.0	2.0	—	
Output Off Leak Current		I_{TL}	—	V_{DD} = 5V, V_{TLH} = 5V, V_{TLL} = 0V (DO1, DO2)	—	—	± 1.0	μA

General-Purpose I/O Ports (P1-0 to P4-3)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current	"H" Level	I_{OH1}	—	V_{DD} = 5V, V_{OH} = 4.5V	− 1.0	− 2.0	—	mA
	"L" Level	I_{OL1}	—	V_{DD} = 5V, V_{OH} = 0.5V	1.0	2.0	—	
Input Leak Current		I_{TL}	—	V_{DD} = 5V, V_{TLH} = 5V, V_{TLL} = 0V (DO1, DO2)	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL2}	—	—	0	~	V_{DD} × 0.3	

General-Purpose I/O Ports (P5-0 to P7-3)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Current	"H" Level	I_{OH1}	—	V_{DD} = 5V, V_{OH} = 4.5V	− 0.5	− 1.0	—	mA
	"L" Level	I_{OL1}	—	V_{DD} = 5V, V_{OL} = 0.5V	0.5	1.0	—	
Input Leak Current		I_{LI}	—	V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL2}	—	—	0	~	V_{DD} × 0.3	

IN1, IN2, $\overline{\text{RESET}}$, INTR1 and INTR2 Input Ports

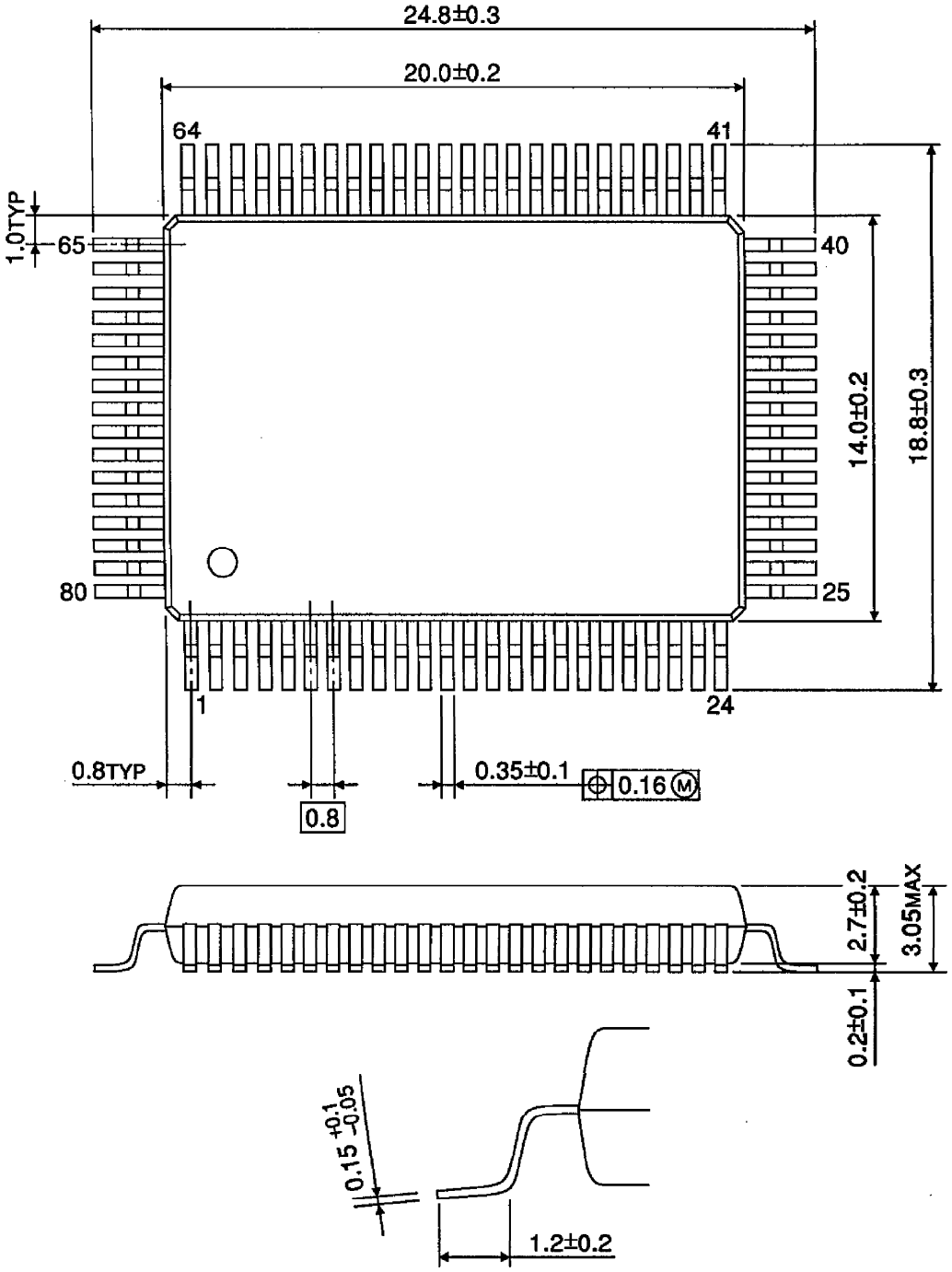
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Leak Current		I_{LI}	—	V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V	—	—	± 1.0	μA
Input Voltage	"H" Level	V_{IH2}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL2}	—	—	0	~	V_{DD} × 0.3	

Others

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Pulldown Resistance	R_{IN2}	—	(TEST)	25	50	100	kΩ
	R_{IN3}	—	(FM_{IN}, AM_{IN})	7.5	15	30	
X_{IN} Amplifier Feedback Resistance	Rf_{XT}	—	(X_{IN}-X_{OUT})	0.5	1.0	2.0	MΩ
Input Amplifier Feedback Resistance	Rf_{IN}	—	(FM_{IN}, AM_{IN}, IF_{IN1}, IF_{IN2})	250	500	1000	kΩ

PACKAGE DIMENSIONS

QFP80-P-1420-0.80A Unit : mm



Weight : 1.57g (Typ.)

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000707EBA

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