

# T1/E1 Clock Generator

## Features

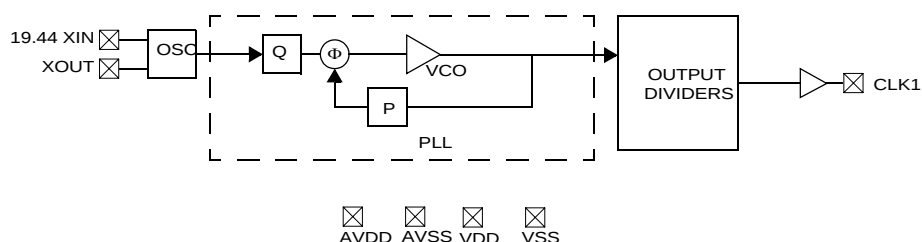
- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- 3.3V operation

## Benefits

- High-performance PLL tailored for T1/E1 clock generation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

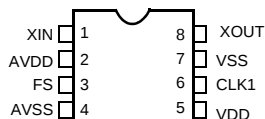
| Part Number | Outputs | Input Frequency Range | Output Frequencies               |
|-------------|---------|-----------------------|----------------------------------|
| CY26200     | 1       | 19.44 MHz             | 1.544 MHz/2.048 MHz (selectable) |

## Logic Block Diagram



## Pin Configuration

**CY26200  
8-pin SOIC**



**Table 1. CY26200 Frequency Select Option**

| Frequency Select | CLK1  | Unit |
|------------------|-------|------|
| 0                | 1.544 | MHz  |
| 1                | 2.048 | MHz  |

## Pin Summary

| Pin Name            | Pin Number | Pin Description                       |
|---------------------|------------|---------------------------------------|
| XIN                 | 1          | 19.44-MHz Reference Input             |
| AVDD                | 2          | Analog Voltage Supply                 |
| FS                  | 3          | Frequency Select – see <i>Table 1</i> |
| AVSS                | 4          | Analog Ground                         |
| VDD                 | 5          | Voltage Supply                        |
| CLK1                | 6          | 1.544-MHz/2.048-MHz Clock Output      |
| VSS                 | 7          | Ground                                |
| XOUT <sup>[1]</sup> | 8          | Reference Output                      |

## Absolute Maximum Conditions

| Parameter       | Description                                 | Min.                  | Max.                  | Unit |
|-----------------|---------------------------------------------|-----------------------|-----------------------|------|
| V <sub>DD</sub> | Supply Voltage                              | –0.5                  | 7.0                   | V    |
| T <sub>S</sub>  | Storage Temperature <sup>[2]</sup>          | –65                   | 125                   | °C   |
| T <sub>J</sub>  | Junction Temperature                        |                       | 125                   | °C   |
|                 | Digital Inputs                              | V <sub>SS</sub> – 0.3 | V <sub>DD</sub> + 0.3 | V    |
|                 | Digital Outputs Referred to V <sub>DD</sub> | V <sub>SS</sub> – 0.3 | V <sub>DD</sub> + 0.3 | V    |
|                 | Electrostatic Discharge                     | 2000                  |                       | V    |

## Recommended Operating Conditions

| Parameter                         | Description                                                                                                | Min.  | Typ.  | Max.  | Unit |
|-----------------------------------|------------------------------------------------------------------------------------------------------------|-------|-------|-------|------|
| V <sub>DD</sub> /AV <sub>DD</sub> | Operating Voltage                                                                                          | 3.135 | 3.3   | 3.465 | V    |
| T <sub>A</sub>                    | Ambient Temperature (Commercial)                                                                           | 0     |       | 70    | °C   |
| T <sub>A</sub>                    | Ambient Temperature (Industrial)                                                                           | –40   |       | +85   | °C   |
| C <sub>LOAD</sub>                 | Max. Load Capacitance                                                                                      |       |       | 15    | pF   |
| f <sub>REF</sub>                  | Reference Frequency                                                                                        |       | 19.44 |       | MHz  |
| t <sub>PU</sub>                   | Power-up time for all V <sub>DD</sub> s to reach minimum specified voltage (power ramps must be monotonic) | 0.05  |       | 500   | ms   |

## DC Electrical Characteristics (Commercial)

| Parameter       | Description           | Conditions                                                      | Min. | Typ. | Max. | Unit |
|-----------------|-----------------------|-----------------------------------------------------------------|------|------|------|------|
| I <sub>OH</sub> | Output High Current   | V <sub>OH</sub> = V <sub>DD</sub> – 0.5, V <sub>DD</sub> = 3.3V | 12   | 24   |      | mA   |
| I <sub>OL</sub> | Output Low Current    | V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V                   | 12   | 24   |      | mA   |
| C <sub>IN</sub> | Input Capacitance     |                                                                 |      |      | 7    | pF   |
| I <sub>IZ</sub> | Input Leakage Current |                                                                 |      | 5    |      | μA   |
| I <sub>DD</sub> | Supply Current        | Sum of Core and Output Current                                  |      |      | 20   | mA   |

## DC Electrical Characteristics (Industrial)

| Parameter       | Description           | Conditions                                                      | Min. | Typ. | Max. | Unit |
|-----------------|-----------------------|-----------------------------------------------------------------|------|------|------|------|
| I <sub>OH</sub> | Output High Current   | V <sub>OH</sub> = V <sub>DD</sub> – 0.5, V <sub>DD</sub> = 3.3V | 11   | 24   |      | mA   |
| I <sub>OL</sub> | Output Low Current    | V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V                   | 11   | 24   |      | mA   |
| C <sub>IN</sub> | Input Capacitance     |                                                                 |      |      | 7    | pF   |
| I <sub>IZ</sub> | Input Leakage Current |                                                                 |      | 5    |      | μA   |
| I <sub>DD</sub> | Supply Current        | Sum of Core and Output Current                                  |      |      | 25   | mA   |

### Notes:

1. Float XOUT if XIN is externally driven
2. Rated for 10 years

**AC Electrical Characteristics** ( $V_{DD} = 3.3V$ , Commercial)

| Parameter <sup>[3]</sup> | Description            | Conditions                                                 | Min. | Typ. | Max. | Unit |
|--------------------------|------------------------|------------------------------------------------------------|------|------|------|------|
| DC                       | Output Duty Cycle      | Duty Cycle is defined in <i>Figure 1</i> , 50% of $V_{DD}$ | 45   | 50   | 55   | %    |
| $t_3$                    | Rising Edge Slew Rate  | Output Clock Rise Time, 20% - 80% of $V_{DD}$              | 0.8  | 1.4  |      | V/ns |
| $t_4$                    | Falling Edge Slew Rate | Output Clock Fall Time, 80% - 20% of $V_{DD}$              | 0.8  | 1.4  |      | V/ns |
| $t_9$                    | Clock Jitter           | Peak to Peak period jitter                                 |      | 200  |      | ps   |
| $t_{10}$                 | PLL Lock Time          |                                                            |      |      | 3    | ms   |

**AC Electrical Characteristics** ( $V_{DD} = 3.3V$ , Industrial)

| Parameter <sup>[3]</sup> | Name                   | Description                                                | Min. | Typ. | Max. | Unit |
|--------------------------|------------------------|------------------------------------------------------------|------|------|------|------|
| DC                       | Output Duty Cycle      | Duty Cycle is defined in <i>Figure 1</i> , 50% of $V_{DD}$ | 45   | 50   | 55   | %    |
| $t_3$                    | Rising Edge Slew Rate  | Output Clock Rise Time, 20% - 80% of $V_{DD}$              | 0.8  | 1.4  |      | V/ns |
| $t_4$                    | Falling Edge Slew Rate | Output Clock Fall Time, 80% - 20% of $V_{DD}$              | 0.8  | 1.4  |      | V/ns |
| $t_9$                    | Clock Jitter           | Peak to Peak period jitter                                 |      | 200  |      | ps   |
| $t_{10}$                 | PLL Lock Time          |                                                            |      |      | 3    | ms   |

**Test Circuit**

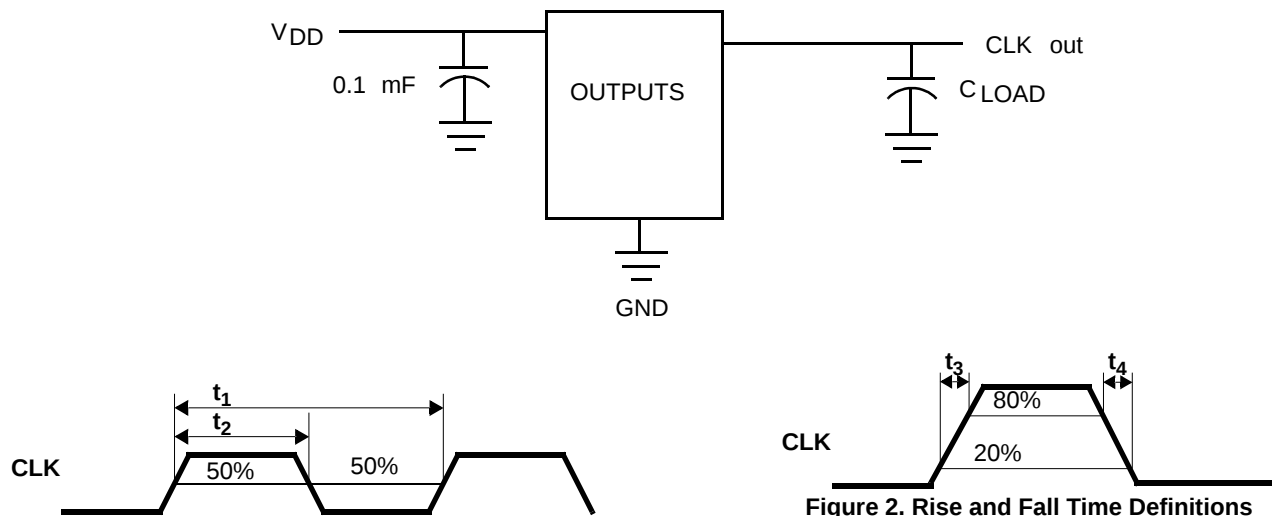


Figure 1. Duty Cycle Definition;  $DC = t_2/t_1$

Figure 2. Rise and Fall Time Definitions

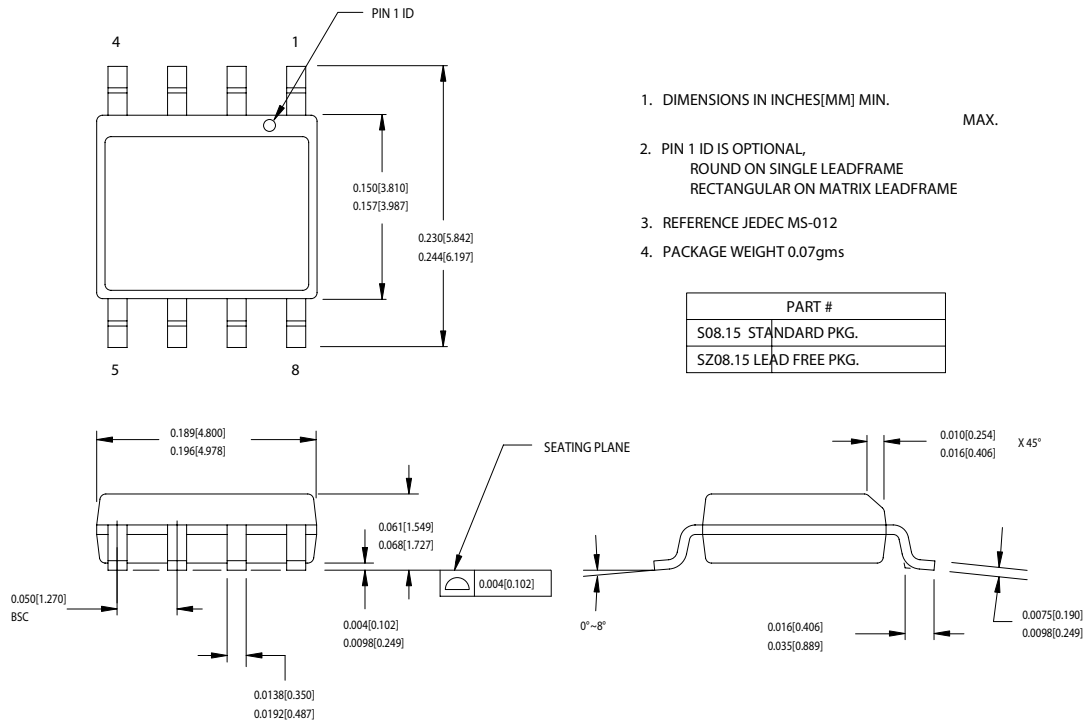
**Ordering Information**

| Ordering Code    | Package Type                | Operating Range | Operating Voltage |
|------------------|-----------------------------|-----------------|-------------------|
| CY26200SC        | 8-lead SOIC                 | Commercial      | 3.3V              |
| CY26200SCT       | 8-lead SOIC - Tape and Reel | Commercial      | 3.3V              |
| CY26200SI        | 8-lead SOIC                 | Industrial      | 3.3V              |
| CY26200SIT       | 8-lead SOIC - Tape and Reel | Industrial      | 3.3V              |
| <b>Lead-free</b> |                             |                 |                   |
| CY26200SXC       | 8-lead SOIC                 | Commercial      | 3.3V              |
| CY26200SXCT      | 8-lead SOIC - Tape and Reel | Commercial      | 3.3V              |
| CY26200SXI       | 8-lead SOIC                 | Industrial      | 3.3V              |
| CY26200SXIT      | 8-lead SOIC - Tape and Reel | Industrial      | 3.3V              |

Notes:  
3. Not 100% tested

## Package Diagram

### 8-lead (150-Mil) SOIC S8



51-85066-\*C

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**Document History Page**

| Document Title: CY26200 T1/E1 Clock Generator<br>Document Number: 38-07335 |         |            |                 |                                                                 |
|----------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------|
| REV.                                                                       | ECN No. | Issue Date | Orig. of Change | Description of Change                                           |
| **                                                                         | 111745  | 05/06/02   | CKN             | New Data Sheet                                                  |
| *A                                                                         | 121890  | 12/14/02   | RBI             | Power up requirements added to Operating Conditions Information |
| *B                                                                         | 400148  | See ECN    | RGL             | Added lead-free devices                                         |