MT90866

Flexible 4 K x 2.4 K Channel Digital Switch with H.110 Interface and 2.4 K x 2.4 K Local Switch

Data Sheet

January 2006

Features

- 2,432 x 2,432 non-blocking switching among local streams
- 4,096 x 2,432 blocking switching between backplane and local streams
- 2,048 x 2,048 non-blocking switching among backplane streams
- Rate conversion between backplane and local streams
- Rate conversion among local streams
- Backplane interface accepts data rates of 8.192 Mb/s or 16.384 Mb/s
- Local interface accepts data rates of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s
- Sub-rate switching (2 or 4 bits) configuration for local streams at a data rate of 2.048 Mb/s
- Meets all the key H.110 mandatory signal requirements including timing
- Per-channel variable or constant throughput delay
- Per-stream input delay, programmable for local streams on a per bit basis
- Per-stream output advancement, programmable for backplane and local streams
- Per-channel direction control for backplane streams
- Per-channel message mode for backplane and local streams
- Per-channel high impedance output control for backplane and local streams
- Compatible to Stratum 4 Enhanced clock switching standard
  - Integrated PLL conforms to Telcordia GR-1244-CORE Stratum 4 Enhanced switching standard -Holdover Mode with holdover frequency stability of 0.07 ppm
    - Jitter attenuation from 1.52 Hz.
    - Time interval error (TIE) correction
    - Master and Slave mode operation
- Non-multiplexed microprocessor interface

Ordering Information

MT90866AG	344 Ball PBGA	Trays
MT90866AG2	344 Ball PBGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Connection memory block-programming for fast device initialization
- Tristate-control outputs for external drivers
- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for backplane and local streams
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- 3.3 V operation with 5 V tolerant inputs and I/O's
- 5 V tolerant PCI driver on CT-Bus I/O's

Applications

- Carrier-grade VoIP Gateways
- IP-PBX and PABX
- Integrated Access Devices
- Access Servers
- CTI Applications/CompactPCI® Platforms
- H.110, H.100, ST-BUS and proprietary Backplane Applications

Description

The MT90866 Digital Switch provides switching capacities of 4,096 x 2,432 channels between backplane and local streams, 2,432 x 2,432 channels among local streams and 2,048 x 2,048 channels among backplane streams. The local connected serial inputs and outputs have 32, 64 and 128 64 kb/s channels per frame with data rates of 2.048, 4.096 and 8.192 Mb/s respectively. The backplane connected serial inputs and outputs have 128 and 256 64 kb/s channels per frame with data rates of 8.192 and 16.384 Mb/s respectively.

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

The MT90866 also offers a sub-rate switching configuration which allows 2-bit wide 16 kb/s or 4-bit wide 32 kb/s data channels to be switched within the device.

The device has features that are programmable on a per-stream or a per-channel basis including message mode, input delay offset, output advancement offset, direction control, and high impedance output control.

The MT90866 supports all three of the H.110 specification required clocking modes: Primary Master, Secondary Master and Slave.

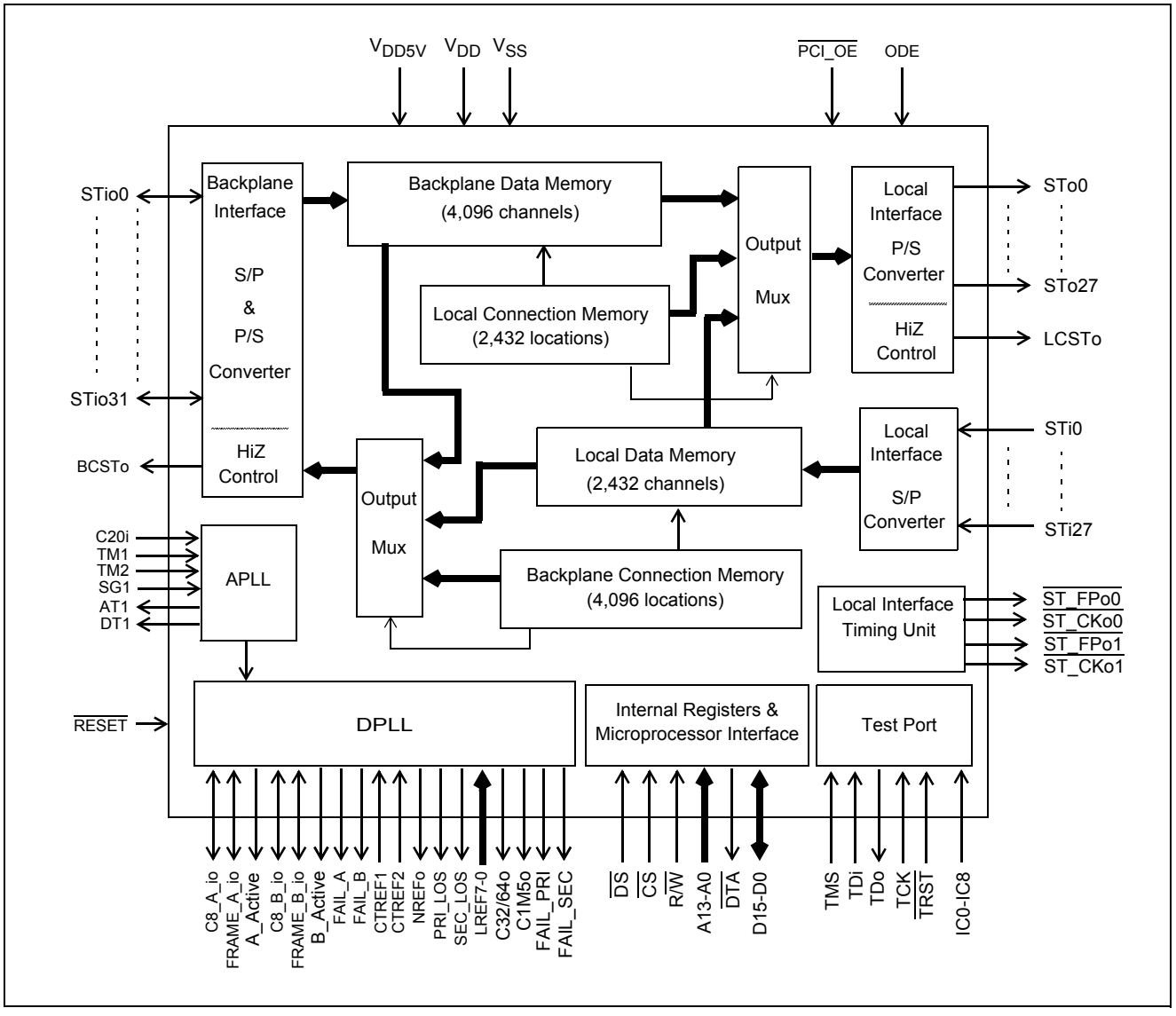

Figure 1 - Functional Block Diagram

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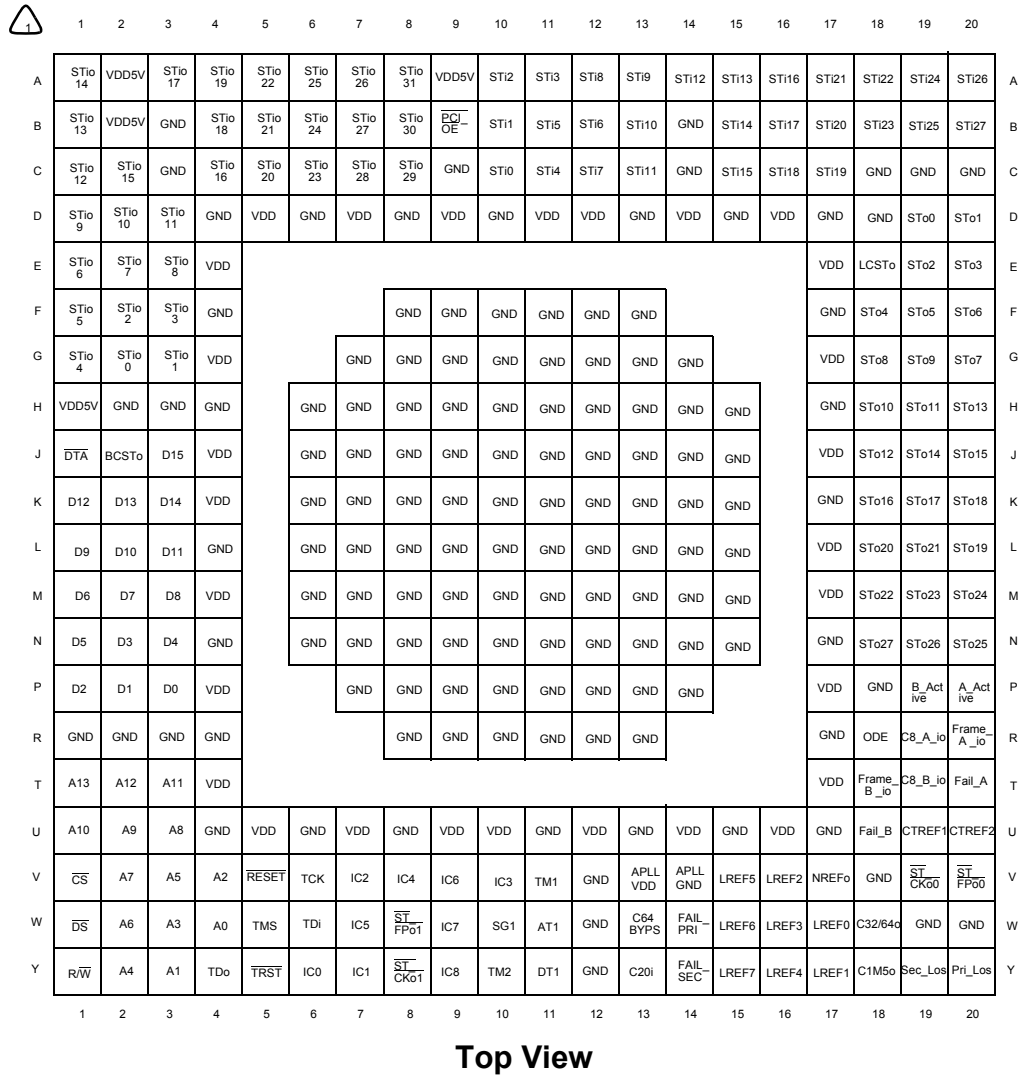
Changes Summary

The following table captures the changes from the September 2005 issue.

Page	Item	Change
9	Ball Signal Assignment	Added missing Ball signals.
11	Pin name: $\overline{\text{RESET}}$	Worst case 600 μs instead of 100 μs is specified for the delay that must be applied before performing the first microprocessor access after the release of $\overline{\text{RESET}}$ pin.
44	Section 20.0	The 600 μs delay requirement before performing the first microprocessor access after the release of $\overline{\text{RESET}}$ pin is added in this section for completeness.
80	Figure 40	Corrected 8 Mb/s stream channel to ch127

The following table captures the changes from the October 2003 issue.

Page	Item	Change
37, 58	Section 18.2 and Table 21	Added description clarifying that the MTIE reset must be set when the device is in the slave mode.
60	Table 22	Added MRST (bit 10) in MT90866 Mode Selection table
39, 41	Section 18.7 and Section 19.1	Deleted the intrinsic jitter descriptions in Section 18.7 and Section 19.1 and replaced them with “AC Electrical Characteristics†- Output Clock Jitter Generation (Unfiltered)” on page 76.
77, 78, 80	“AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 8 Mb/s” , “AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 16 Mb/s” and “AC Electrical Characteristics† - Local Serial Stream Input Timing” .	Input data sampling timings were updated for clarity purposes.



Top View

1 - A1 corner is identified by metallized markings.

Figure 2 - 27 mm x 27 mm PBGA (JEDEC MO-151) Pinout

Ball Signal Assignment

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	STIO14	C5	STIO20	F1	STIO5	H17	GND	L6	GND	N14	GND
A2	VDD5V	C6	STIO23	F2	STIO2	H18	STO10	L7	GND	N15	GND
A3	STIO17	C7	STIO28	F3	STIO3	H19	STO11	L8	GND	N17	GND
A4	STIO19	C8	STIO29	F4	GND	H20	STO13	L9	GND	N18	STO27
A5	STIO22	C9	GND	F8	GND	J1	$\overline{\text{DTA}}$	L10	GND	N19	STO26
A6	STIO25	C10	STI0	F9	GND	J2	BCSTO	L11	GND	N20	STO25
A7	STIO26	C11	STI4	F10	GND	J3	D15	L12	GND	P1	D2
A8	STIO31	C12	STI7	F11	GND	J4	VDD	L13	GND	P2	D1
A9	VDD5V	C13	STI11	F12	GND	J6	GND	L14	GND	P3	D0
A10	STI2	C14	GND	F13	GND	J7	GND	L15	GND	P4	VDD
A11	STI3	C15	STI15	F17	GND	J8	GND	L17	VDD	P7	GND
A12	STI8	C16	STI18	F18	STO4	J9	GND	L18	STO20	P8	GND
A13	STI9	C17	STI19	F19	STO5	J10	GND	L19	STO21	P9	GND
A14	STI12	C18	GND	F20	STO6	J11	GND	L20	STO19	P10	GND
A15	STI13	C19	GND	G1	STIO4	J12	GND	M1	D6	P11	GND
A16	STI16	C20	GND	G2	STIO0	J13	GND	M2	D7	P12	GND
A17	STI21	D1	STIO9	G3	STIO1	J14	GND	M3	D8	P13	GND
A18	STI22	D2	STIO10	G4	VDD	J15	GND	M4	VDD	P14	GND
A19	STI24	D3	STIO11	G7	GND	J17	VDD	M6	GND	P17	VDD
A20	STI26	D4	GND	G8	GND	J18	STO12	M7	GND	P18	GND
B1	STIO13	D5	VDD	G9	GND	J19	STO14	M8	GND	P19	B_ACTIVE
B2	VDD5V	D6	GND	G10	GND	J20	STO15	M9	GND	P20	A_ACTIVE
B3	GND	D7	VDD	G11	GND	K1	D12	M10	GND	R1	GND
B4	STIO18	D8	GND	G12	GND	K2	D13	M11	GND	R2	GND
B5	STIO21	D9	VDD	G13	GND	K3	D14	M12	GND	R3	GND
B6	STIO24	D10	GND	G14	GND	K4	VDD	M13	GND	R4	GND
B7	STIO27	D11	VDD	G17	VDD	K6	GND	M14	GND	R8	GND
B8	STIO30	D12	VDD	G18	STO8	K7	GND	M15	GND	R9	GND
B9	$\overline{\text{PCI\_OE}}$	D13	GND	G19	STO9	K8	GND	M17	VDD	R10	GND
B10	STI1	D14	VDD	G20	STO7	K9	GND	M18	STO22	R11	GND
B11	STI5	D15	GND	H1	VDD5V	K10	GND	M19	STO23	R12	GND
B12	STI6	D16	VDD	H2	GND	K11	GND	M20	STO24	R13	GND
B13	STI10	D17	GND	H3	GND	K12	GND	N1	D5	R17	GND
B14	GND	D18	GND	H4	GND	K13	GND	N2	D3	R18	ODE
B15	STI14	D19	STO0	H6	GND	K14	GND	N3	D4	R19	C8_A_IO
B16	STI17	D20	STO1	H7	GND	K15	GND	N4	GND	R20	FRAME_A_IO
B17	STI20	E1	STIO6	H8	GND	K17	GND	N6	GND	T1	A13
B18	STI23	E2	STIO7	H9	GND	K18	STO16	N7	GND	T2	A12
B19	STI25	E3	STIO8	H10	GND	K19	STO17	N8	GND	T3	A11
B20	STI27	E4	VDD	H11	GND	K20	STO18	N9	GND	T4	VDD
C1	STIO12	E17	VDD	H12	GND	L1	D9	N10	GND	T17	VDD
C2	STIO15	E18	LCSTO	H13	GND	L2	D10	N11	GND	T18	FRAME_B_IO
C3	GND	E19	STO2	H14	GND	L3	D11	N12	GND	T19	C8_B_IO
C4	STIO16	E20	STO3	H15	GND	L4	GND	N13	GND	T20	FAIL_A

Ball	Signal	Ball	Signal
U1	A10	W6	TDi
U2	A9	W7	IC5
U3	A8	W8	$\overline{\text{ST\_FPo1}}$
U4	GND	W9	IC7
U5	VDD	W10	SG1
U6	GND	W11	AT1
U7	VDD	W12	GND
U8	GND	W13	C64BYPS
U9	VDD	W14	FAIL_PRI
U10	VDD	W15	LREF6
U11	GND	W16	LREF3
U12	VDD	W17	LREF0
U13	GND	W18	C32/64o
U14	VDD	W19	GND
U15	GND	W20	GND
U16	VDD	Y1	R/$\overline{\text{W}}$
U17	GND	Y2	A4
U18	FAIL_B	Y3	A1
U19	CTREF1	Y4	TDo
U20	CTREF2	Y5	$\overline{\text{TRST}}$
V1	$\overline{\text{CS}}$	Y6	IC0
V2	A7	Y7	IC1
V3	A5	Y8	$\overline{\text{ST\_CKo1}}$
V4	A2	Y9	IC8
V5	$\overline{\text{RESET}}$	Y10	TM2
V6	TCK	Y11	DT1
V7	IC2	Y12	GND
V8	IC4	Y13	C20I
V9	IC6	Y14	FAIL_SEC
V10	IC3	Y15	LREF7
V11	TM1	Y16	LREF4
V12	GND	Y17	LREF1
V13	APLLVDD	Y18	C1M5O
V14	APLLGND	Y19	SEC_LOS
V15	LREF5	Y20	PRI_LOS
V16	LREF2		
V17	NREFo		
V18	GND		
V19	$\overline{\text{ST\_CKo0}}$		
V20	$\overline{\text{ST\_FPo0}}$		
W1	$\overline{\text{DS}}$		
W2	A6		
W3	A3		
W4	A0		
W5	TMS		

Pin Description

PBGA Ball Number	Name	Description
D5, D7, D9, D11, D12, D14, D16, E4, E17, G4, G17, J4, J17, K4, L17, M4, M17, P4, P17, T4, T17,U5, U7, U9, U10, U12, U14, U16	V_{DD}	**+3.3 Volt Power Supply**.
A2,A9,B2,H1	V_{DD5V}	**+5.0 V/+3.3 V Power Supply**. If 5 V power supply is tied to these pins, STio0-31 pins will meet 5 V PCI requirements. If 3.3 V power supply is tied to these pins, STio0-31 pins will meet 3.3 V PCI requirements.
B3, B14,C3, C9, C14, C18, C19, C20, D4, D6, D8, D10, D13, D15, D17, D18, F4, F8-F13, F17, G7-G14, H2, H3, H4, H6-H15, H17, J6-J15, K6-K15, K17, L4, L6-L15, M6-M15, N4, N6-15, N17, P7-P14, P18, R1, R2, R3, R4, R8-R13, R17, U4, U6, U8, U11, U13, U15, U17, V12, V18, W12, W19, W20, Y12	V_{SS}	**Ground**.
V13	$APLLV_{DD}$	**+3.3 Volt Analog PLL Power Supply**. No special filtering is required for this pin.
V14	$APLLV_{ss}$	**Analog PLL Ground**
V5	$\overline{RESET}$	**Device Reset (5 V Tolerant Input).** This input (active low) puts the device in its reset state; this state clears the device's internal counters and registers. To ensure proper reset action, the reset pin must be low for longer than 400 ns. To ensure proper operation, a delay of 600 µs must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high. The device reset also tristates STo0-27 and STio0-31, and sets the LCSTo and BCSTo pins. When in a $\overline{RESET}$ condition, the C8_A_io, FRAME_A_io, C8_B_io, and FRAME_B_io signals are tri-stated.
G2, G3, F2, F3, G1, F1, E1, E2, E3, D1, D2, D3, C1, B1, A1, C2	STio0-3, STio4-7, STio8-11, STio12-15	**Serial Input/Output Streams 0 - 15 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept serial TDM data streams at 8.192 Mb/s with 128 channels per stream. In the 16 Mb/s mode, these pins accept serial TDM data streams at 16.384 Mb/s with 256 channels per stream respectively.

Pin Description (continued)

PBGA Ball Number	Name	Description
C4, A3, B4, A4, C5, B5, A5, C6, B6, A6, A7, B7, C7, C8, B8, A8	STio16 - 19, STio20 - 23, STio24 - 27, STio28 - 31	**Serial Input/Output Streams 16 - 31 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept serial TDM data streams at 8.192 Mb/s with 128 channels per stream. In the 16 Mb/s mode, these pins are tristated internally and should be connected to ground.
C10, B10, A10, A11	STi0-3	**Serial Input Streams 0 - 3 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8Mb/s mode, these inputs accept data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
C11, B11, B12, C12	STi4 - 7	**Serial Input Streams 4 - 7 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these inputs accept data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
A12, A13, B13, C13	STi8 - 11	**Serial Input Streams 8 - 11 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these inputs accepts data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
A14, A15, B15, C15	STi12 - 15	**Serial Input Streams 12 - 15 (5 V Tolerant Inputs).** In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these inputs accept data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these inputs accept a data rate of 2.048 Mb/s.
A16, B16, C16, C17, B17, A17, A18, B18, A19, B19, A20, B20	STi16 - 27	**Serial Input Streams 16 - 27 (5 V Tolerant Inputs)**. In 2 Mb/s mode, these inputs accept data rates of 2.048 Mb/s with 32 channels per stream respectively. In 4 Mb/s or 8 Mb/s mode, the STi16 - 18 inputs accept data rates of 4.096 or 8.192 Mb/s with 64 or 128 channels per stream respectively. In 4 Mb/s or 8 Mb/s mode the STi19 - 27 inputs should be driven low. No sub-rate switching mode is offered for STi16-27.
D19, D20, E19, E20	STo0 - 3	**Serial Output Streams 0 - 3 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.
F18, F19, F20, G20	STo4 - 7	**Serial Output Streams 4 - 7 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.
G18, G19, H18, H19	STo8 - 11	**Serial Output Streams 8 - 11 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.
J18, H20, J19, J20	STo12 - 15	**Serial Output Streams 12 - 15 (5 V Tolerant Tri-State Outputs)**. In 2 Mb/s, 4 Mb/s or 8 Mb/s mode, these outputs have data rates of 2.048, 4.096 or 8.192 Mb/s with 32, 64 or 128 channels per stream respectively. In the 2-bit and 4-bit sub-rate modes, these outputs have a data rate of 2.048 Mb/s.

Pin Description (continued)

PBGA Ball Number	Name	Description
K18, K19, K20, L20, L18, L19, M18, M19, M20, N20, N19, N18	STo16 - 27	**Serial Output Streams 16 to 27 (5 V Tolerant Tri-state Outputs).** In 2 Mb/s mode, these outputs have data rate of 2.048 Mb/s with 32 channels per stream. In 4 Mb/s or 8 Mb/s mode, the STo16 - 18 outputs have data rates of 4.096 Mb/s or 8.192 Mb/s with 64 or 128 channels per stream respectively; STo19 - 27 are driven low. No sub-rate switching mode is offered for STo16-27.
R18	ODE	**Output Drive Enable (5 V Tolerant Input).** When this pin is low, STo0 to STo27, STio0 to STio31, C1M5o, C32/64o, ST_CKo0, ST_CKo1, ST_FPo0 and ST_FPo1 outputs are all in high-impedance state. When ODE is high all of the aforementioned pins are active.
J2	BCSTo	**Backplane Control Signal (Output)**. This pin is used for backplane external tristate controllers. When this signal is high, the corresponding output channels are in a high impedance state. BCSTo's bit rate is 32.768 MHz.
E18	LCSTo	**Local Control Signal (Output).** This pin is used for local external tristate control. When this signal is high, the corresponding ouput channels are in a high impedance state. The bit rate is 32.768 MHz.
Y13	C20i	**Master Clock (5 V Tolerant Input).** This pin accepts a 20.000 MHz clock.
R19	C8_A_io	**Clock A (5 V Tolerant I/O).** This is a 8.192 MHz clock with 50% duty cycle.
R20	FRAME_A_io	**Frame Reference A (5 V Tolerant I/O).** This is a 122 ns wide, negative pulse, with 125 us period.
P20	A_Active	**A Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_A_io and the FRAME_A_io pins are inputs or outputs. When Bit 13 of the DOM1 register is low, this pin drives low and the C8_A_io and FRAME_A_io output drivers are disabled. When Bit 13 of the DOM1 register is high, this pin drives high and the C8_A_io and FRAME_A_io output drivers are enabled.
T19	C8_B_io	**Clock B (5 V Tolerant I/O).** This is a 8.192 MHz clock with 50% duty cycle.
T18	FRAME_B_io	**Frame Reference B (5 V Tolerant I/O).** This is a 122 ns wide, negative pulse, with 125 us period.
P19	B_Active	**B Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_B_io and the FRAME_B_io pins are inputs or outputs. When Bit 14 of the DOM1 register is low, this pin drives low and the C8_B_io and FRAME_B_io output drivers are disabled. When Bit 14 of the DOM1 register is high, this pins drives high and the C8_B_io and FRAME_B_io output drivers are enabled.
T20	FAIL_A	**A Failure (Output).** When the C8_A_io or the FRAME_A_io signal fails, this signal goes to high.
U18	FAIL_B	**B Failure (Output).** When the C8_B_io or the FRAME_B_io signal fails, this signal goes to high.

Pin Description (continued)

PBGA Ball Number	Name	Description
U19	CTREF1	**CT-Bus Reference 1 (5 V Tolerant Input).** This pin accepts 8 KHz, 1.544 MHz or 2.048 MHz network timing reference.
U20	CTREF2	**CT-Bus Reference 2 (5 V Tolerant Input).** This pin accepts 8 KHz, 1.544 MHz or 2.048 MHz network timing reference.
W17, Y17, V16, W16, Y16, V15, W15, Y15	LREF0- 7	**Local Reference (5 V Tolerant Inputs).** These pins accept 8 KHz, 1.544 MHz or 2.048 MHz local timing reference.
V17	NREFo	**Network Reference Output (Output).** Any local reference can be switched to this output. The output data rate can be either the same as the selected reference input data rate or divided to be 8 KHz.
Y20	PRI_LOS	**Primary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that PRIMARY REFERENCE is not valid. Combined with SEC_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
Y19	SEC_LOS	**Secondary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that SECONDARY REFERENCE is not valid. Combined with the PRI_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
W14	FAIL_PRI	**Primary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the PLS bit of the DPLL House Keeping Register (DHKR). When the primary reference fails, this signal goes to 1.
Y14	FAIL_SEC	**Secondary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the SLS bit of the DPLL House Keeping Register (DHKR). When the secondary reference fails, this signal goes to 1.
W18	C32/64o	**C32/64o Clock (5 V Tolerant Output).** A 32.768 MHz output clock when the DPLL Clock Monitor register bit (CKM) is low. A 65.536 MHz clock when the DPLL Clock Monitor register bit (CKM) is high.
Y18	C1M5o	**C1.5o Clock (5 V Tolerant Output).** A 1.544 MHz output clock.
V20	$\overline{\text{ST\_FPo0}}$	**ST-Bus Frame Pulse Output (5 V Tolerant Output).** The width of this output ST-Bus frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 KHz.
V19	$\overline{\text{ST\_CKo0}}$	**ST-Bus Clock Output (5 V Tolerant Output).** The frequency of this output ST-Bus clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
W8	$\overline{\text{ST\_FPo1}}$	**ST-Bus Frame Pulse Output (5 V Tolerant Output)**. The width of this output ST-Bus frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 KHz.
Y8	$\overline{\text{ST\_CKo1}}$	**ST-Bus Clock Output (5 V Tolerant Output)**. The frequency of this output ST-Bus clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
V1	$\overline{\text{CS}}$	**Chip Select (5 V Tolerant Input).** This active low input is used by the microprocessor to access the microport.

Pin Description (continued)

PBGA Ball Number	Name	Description
W1	$\overline{DS}$	**Data Strobe (5 V Tolerant Input).** This active low input works in conjunction with $\overline{CS}$ to initiate the read and write cycles.
Y1	R/$\overline{W}$	**Read/Write (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0 - D15) during the microprocessor access.
W4, Y3, V4, W3, Y2, V3, W2, V2, U3, U2, U1, T3, T2, T1	A0 - A13	**Address 0 - 13 (5 V Tolerant Inputs).** These are the address lines to the internal memories and registers.
P3, P2, P1, N2, N3, N1, M1, M2, M3, L1, L2, L3, K1, K2, K3, J3	D0 - D15	**Data Bus 0 - 15 (5 V Tolerant I/Os)**. These pins form the 16-bit data bus of the microport.
J1	$\overline{DTA}$	**Data Transfer Acknowledge (5 V Tolerant Output)**. This active low output indicates that a data bus transfer is completed. A pull-up resistor is required to hold a high level.
B9	$\overline{PCI\_OE}$	**PCI Output Enable (3.3 V Tolerant Input)**. This active low input is the control signal used to tristate the STio0 - 31 pins during hot-swapping. During normal operation this signal should be low.
W13	C64BYPS	**PLL Bypass Clock Input (5 V Tolerant Input).** Used for device testing. In functional mode, this input MUST be low.
V11	TM1	**APLL Test Pin 1 (3.3 V Input).** Use for APLL testing only. In normal operation, this input should be connected to ground.
Y10	TM2	**APLL Test Pin 2 (3.3 V Input).** Use for APLL testing only. In normal operation, this input should be connected to ground.
W10	SG1	**APLL Test Control (3.3 V Input).** Use for APLL testing only. In normal operation, this input should be connected to ground.
W11	AT1	**Analog Test Access (5 V Tolerant I/O).** Use for APLL testing only. No connection for normal operation.
Y11	DT1	**Digital Test Access Output (5 V Tolerant Output).** Use for APLL testing only. No connection for normal operation.
W5	TMS	**Test Mode Select (3.3 V Input with Internal pull-up).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
W6	TDi	**Test Serial Data In (3.3 V Input with Internal pull-up)**. JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
Y4	TDo	**Test Serial Data Out (3.3 V Tolerant Tri-state Output)**. JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.

Pin Description (continued)

PBGA Ball Number	Name	Description
V6	TCK	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic. This pin should be low when JTAG is not enabled.
Y5	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with Internal pull-up).** Asynchronously initializes the JTAG TAP Controller by putting it in the Test-Logic-Reset state. This pin should be pulled low to ensure that the MT90866 is in normal functional mode.
Y6	IC0	Leave unconnected for normal operation.
Y7	IC1	Leave unconnected for normal operation.
V7	IC2	In normal operation this pin MUST be connected to ground.
V10	IC3	Leave unconnected for normal operation.
V8	IC4	Leave unconnected for normal operation.
W7	IC5	Leave unconnected for normal operation.
V9	IC6	Leave unconnected for normal operation.
W9	IC7	Leave unconnected for normal operation.
Y9	IC8	Leave unconnected for normal operation.

1.0 Device Overview

The MT90866 can switch up to 4,096 × 2,432 channels while providing a rate conversion capability. It is designed to switch 64 kb/s PCM or N X 64 kb/s data between the backplane and local switching applications. The device maintains frame integrity in data applications and minimum throughput delay for voice application on a per channel basis.

The backplane interface can operate at 8.192 Mb/s in CT-Bus mode or 16.384 Mb/s in ST-BUS mode and is arranged in 125 µs wide frames that contain 128 or 256 channels respectively. A built-in rate conversion circuit allows users to interface between backplane and local interfaces which operates at 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s. When the device is in the local sub-rate switching mode, 2-bit 16 kb/s or 4-bit 32 kb/s data channels can be switched within the device. The local sub-rate switching mode is available in 2 Mb/s mode only.

By using Zarlink's message mode capability, the microprocessor can access input and output time slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices.

2.0 Functional Description

A Functional Block Diagram of the MT90866 is shown in Figure 1, "Functional Block Diagram" on page 2. It is designed to interface CT-Bus and ST-BUS serial streams from a backplane source and ST-BUS serial streams from a local source.

3.0 Frame Alignment Timing

In the ST-BUS or the CT-Bus mode, the C8_A_io or C8_B_io pin accepts an 8.192 MHz clock for the frame pulse alignment. The FRAME_A_io or FRAME_B_io is the frame pulse signal which goes low at the frame boundary for 122 ns. The frame boundary is defined by the rising edge of the C8_A_io or C8_B_io clock during the low cycle of the frame pulse. Figure 3, "CT-Bus Timing for 8 Mb/s Backplane Data Streams" on page 17 is the CT-Bus timing for the backplane 8.192 Mb/s data streams and Figure 4, "ST-BUS Timing for 16 Mb/s Backplane Data Streams" on page 18 is the ST-BUS timing for the 16.384 Mb/s backplane data stream.

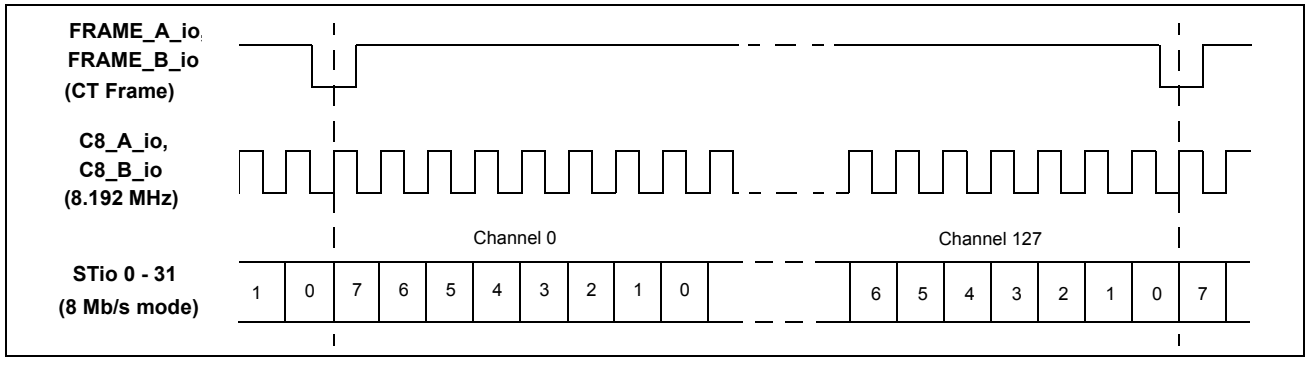


Figure 3 - CT-Bus Timing for 8 Mb/s Backplane Data Streams

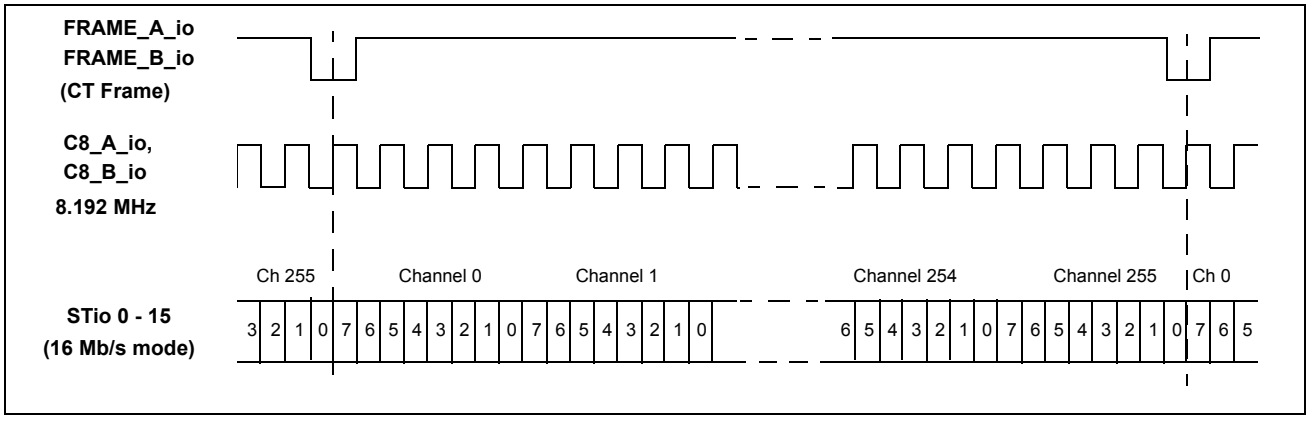


Figure 4 - ST-BUS Timing for 16 Mb/s Backplane Data Streams

4.0 Switching Configuration

The device has two operation modes at different data rates for the backplane interface and five operation modes for the local interface. These modes can be programmed via the Device Mode Selection (DMS) register. Mode selections between the backplane and local interfaces are independent.

4.1 Backplane Interface

The backplane interface can be programmed to accept data streams of 8 Mb/s or 16 Mb/s. When H.110 mode is enabled, STio0 to STio31 have a data rate of 8.192 Mb/s. When ST-BUS mode is enabled, STio0 to STio15 have a data rate of 16.384 Mb/s. Table 1 on page 18 describes the data rates and mode selections for the backplane interface.

4.2 Local Interface

Five operation modes, 2 Mb/s, 4 Mb/s, 8 Mb/s, 2-bit sub-rate and 4-bit sub-rate switching, can be selected for the local ST-BUS interface. The local interface is divided into five groups. Group 0 contains STi/STo0-3, Group 1 contains STi/STo4-7, Group 2 contains STi/STo8-11, Group 3 contains STi/STo12-15 and Group 4 contains STi/STo16-27. Each group can be selected individually through the Device Mode Selection (DMS) register. Streams belonging to the same group have the same operation mode. For Groups 0 to 3, any one of the five operation modes can be selected. Input data streams STi0-15 and output data streams, STo0 -15 can be selected according to the group to which they belong. STi16-27 and output data streams STo16-27 belong to Group 4 and can operate in 2 Mb/s mode. In Group 4, only input data streams Sti16-18 and output data streams Sto16-18 can operate in 4 Mb/s and 8 Mb/s mode. When operating Group 4 at 4 Mb/s or 8 Mb/s the unused output streams, STo19-27 are driven low. No sub-rate modes are available for Group 4 data streams. See Table 2 on page 19 to Table 6 on page 20 for a description of the data rates and mode selection for the local ST-BUS interface.

BMS bit of the DMS Register	Modes	Backplane Interface
0	8.192 Mb/s	STio0 - 31
1	16.384 Mb/s	STio0 - 15

Table 1 - Mode Selection for Backplane Streams

DMS Register Bits			Modes	Usable Streams
LG02	LG01	LG00		
0	0	0	8.192 Mb/s	STi0 - 3, STo0 - 3
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 2 - Mode Selection for Local STi0 - 3 and STo0 - 3 Streams, Group 0

DMS Register Bits			Modes	Usable Streams
LG12	LG11	LG10		
0	0	0	8.192 Mb/s	STi4 - 7, STo4 -7
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 3 - Mode Selection for Local STi4 - 7 and STo4 - 7 Streams, Group 1

DMS Register Bits			Modes	Usable Streams
LG22	LG21	LG20		
0	0	0	8.192 Mb/s	STi8 - 11, STo8 - 11
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 4 - Mode Selection for Local STi8 - 11 and STo8 - 11 Streams, Group 2

DMS Register Bits			Modes	Usable Streams
LG32	LG31	LG30		
0	0	0	8.192 Mb/s	STi12-15, STo12-15
0	0	1	4.096 Mb/s	
0	1	0	2.048 Mb/s	
0	1	1	4-bit subrate	
1	0	0	2-bit subrate	

Table 5 - Mode Selection for Local STi12 - 15 and ST012 - 15 Streams, Group 3

DMS Register Bits		Modes	Usable Streams
LG41	LG40		
0	0	8.192 Mb/s	STi16 - 18, STo16 - 18
0	1	4.096 Mb/s	
1	0	2.048 Mb/s	STi16 - 27, STo16 - 27

Table 6 - Mode Selection for Local STi16 - 27 and STo16 - 27 Streams, Group 4

5.0 Local Input Delay Selection

The local input delay selection allows individual local input streams to be aligned and shifted against the input frame pulse (FRAME_A_io or FRAME_B_io). This feature compensates for the variable path delays in the local interface. Such delays can occur in large centralized and distributed switching system.

Each local input stream can have its own bit delay offset value by programming the local input bit delay selection registers (LIDR0 to LIDR9). See Table 12, "Local Input Bit Delay Registers (LIDR0 to LIDR9) Bits" on page 50, for the contents of these registers. Possible bit adjustment can range up to +7 3/4 bit periods forward with resolution of 1/4 bit period. See Table 13 on page 51 and Figure 19 on page 51 for local input delay programming.

6.0 Output Advancement Selection

The MT90866 allows users to advance individual backplane or local output streams with respect to the frame boundary. This feature is useful in compensating variable output delays caused by various output loading conditions. Each output stream can have its own advancement value programmed by the output advancement registers. The backplane output advancement registers (BOAR0 to BOAR3) are used to program the backplane output advancement. The local output advancement registers (LOAR0 to LOAR3) are used to program the local output advancement. Possible adjustment for local and backplane output data streams is 22.5 ns with a resolution of 7.5 ns. The advancement is independent of the output data rate. Table 14 on page 52 and Figure 20, "Example of Backplane Output Advancement Timing" on page 52, and Table 15 on page 53 and Figure 21, "Local Output Advancement Timing" on page 53 describe the details of the output advancement programming for the backplane and local interfaces respectively.

7.0 Local Output Timing Considerations

The output data of the MT90866's local side is slightly advanced with respect to the frame and bit boundary as defined by the local output clocks and frame pulses (ST_FPo0, ST_CKo0, ST_FPo1, ST_CKo1). The advancement is in the range of 5 ns to 17 ns. Despite this advancement, the MT90866 will operate within the parameters specified in the datasheet because input data are usually sampled at the 3/4 or 1/2 point of the bit cell. However, the user should be cautious when introducing additional delay to the clock signals only (e.g., by passing them through glue logic, FPGA, or CPLD), which will introduce a few nanoseconds of delay relative to the data. If the clock signal is delayed, data will be advanced from the receiver device's point of view. This may cause errors in sampling the data. Using an example where a 3/4 sampling point is used, there is about 30 ns from the sampling point to the end of the bit cell. With a worst-case of 17 ns advancement, the timing margin will be approximately 13 ns. Any additional delays applied to the local output clocks (ST_CKo0 and ST_CKo1) must not exceed 13 ns minus the hold time of the receiving device. Delays applied to both clocks and data equally will not impact the device operation.

8.0 Memory Block Programming

The MT90866 block programming mode (BPM) register provides users with the capability of initializing the local and backplane connection memories in two frames. The local connection memory is partitioned into high and low parts. Bit 13 - bit 15 of every backplane connection memory location will be programmed with the pattern stored in bit 6 - bit 8 of the BPM register. Bit 13 - bit 15 of every local connection memory low location will be programmed with the pattern stored in bits 3 to 5 of the BPM register. The other bit positions of the backplane connection memory, the local low connection memory and all bits of the local high connection memory are loaded with zeros. See Figure 5, "Block Programming Data in the Connection Memories" on page 22 for the connection memory contents when the device is in block programming mode.

The block programming mode is enabled by setting the memory block program (MBP) bit of the Control register to high. After the block programming enable (BPE) bit of the BPM register is set to high, the block programming data will be loaded into bits 13 to 15 of every backplane connection memory location and bits 13 to 15 of every local connection memory low location. The other connection memory bits are loaded with zeros. When the memory block programming is completed, the device resets the BPE bit to low. See Table 11 on page 49 for the bit assignment of the BPM register.

9.0 Delay Through the MT90866

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications it is recommended to select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications it is recommended to select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the BTM2 - BTM0 bits of the backplane connection memory or LTM0 - LTM2 bits of the local connection memory as described in Table 25 on page 63 and Table 29 on page 65, respectively.

9.1 Variable Delay Mode

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams. The minimum delays achievable in the MT90866 device are 3-channel delay, 5-channel delay, and 10-channel delay for the 2 MB/s, 4 MB/s, and 8 MB/s respectively. The maximum delay is one frame plus three channels, one frame plus five channels, and one frame plus ten channels for the 2 Mb/s, 4 Mb/s and 8 Mb/s modes respectively.

For the backplane interface, the variable delay mode can be programmed through the backplane connection memory bits, BTM2 - BTM0. When BTM2 - BTM0 are programmed to "000", it is a per-channel variable delay from

local input to the backplane output. When BTM2 - BTM0 are set to “010”, it is a per-channel variable delay from backplane input to backplane output.

For the local interface, the variable delay mode can be programmed through the local connection memory low bits, LTM2 - LTM0. When LTM2 - LTM0 is programmed to “000”, it is a per-channel variable delay from local input to local output. When LTM2 - LTM0 is set to “010”, it is a per-channel variable delay from backplane input to local output.

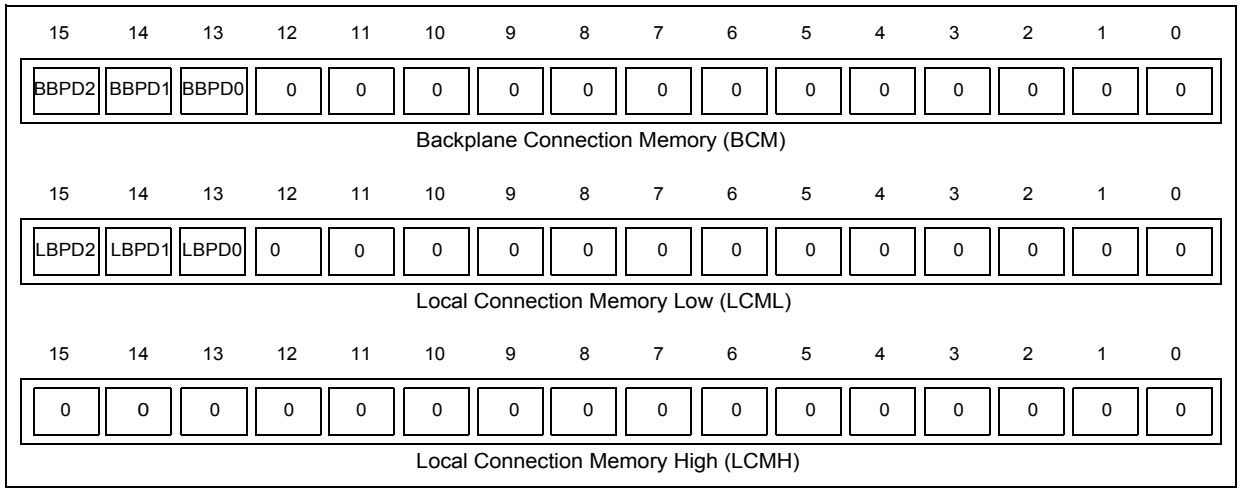


Figure 5 - Block Programming Data in the Connection Memories

9.2 Constant Delay Mode

In this mode, a multiple data memory buffer is used to maintain frame integrity in all switching configurations by using three pages of Data Memory where a channel written in any of the buffers during frame N is always read out during frame N+2.

For the backplane interface, when BTM2 - BTM0 is programmed to “001”, it is a per-channel constant delay mode from local input to backplane output. When BTM2 - BTM0 is programmed to “011”, it is a per-channel constant delay from backplane input to backplane output.

For the local interface, when LTM2 - LTM0 is programmed to “001”, it is a per-channel constant delay mode from local input to local output. When LTM2 - LTM0 is set to “011”, it is a per-channel constant delay mode from backplane input to local output.

10.0 Microprocessor Interface

The MT90866 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed bus structure. The required microprocessor signals are the 16-bit data bus (D15-D0), 14-bit address bus (A13-A0) and 4 control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 44, "Motorola Non-Multiplexed Bus Timing" on page 83 for the Motorola non-multiplexed bus timing.

The MT90866 microprocessor port provides access to the internal registers, the connection and data memories. All locations provide read/write access except for the Local and Backplane Bit Error Rate registers (LBERR and BBERR) and Data Memory which can only be read by the users.

10.1 $\overline{DTA}$ Data Transfer Acknowledgment Pin

The $\overline{DTA}$ pin of the microprocessor is driven LOW by internal logic to indicate that a data bus transfer is completed. When the bus cycle ends, this pin switches to the high impedance state. An external pull-up of between 1 KΩ and 10 KΩ is required at this output.

11.0 Address Mapping of Memories and Registers

The address bus on the microprocessor interface selects the internal registers and memories of the MT90866. If the address bit A13 is low, then the registers are addressed by A12 to A0 as shown in Table 7 on page 23.

A13 - A0	Location
0000_H	Control Register, CR
0001_H	Device Mode Selection Register, DMS
0002_H	Block Programming Mode Register, BPM
0003_H	Reserved
0004_H	Local Input Bit Delay Register 0, LIDR0
0005_H	Local Input Bit Delay Register 0, LIDR1
0006_H	Local Input Bit Delay Register 2, LIDR2
0007_H	Local Input Bit Delay Register 3, LIDR3
0008_H	Local Input Bit Delay Register 4, LIDR4
0009_H	Local Input Bit Delay Register 5, LIDR5
$000A_H$	Local Input Bit Delay Register 6, LIDR6
$000B_H$	Local Input Bit Delay Register 7, LIDR7
$000C_H$	Local Input Bit Delay Register 8, LIDR8
$000D_H$	Local Input Bit Delay Register 9, LIDR9
$000E_H$ to $001B_H$	Reserved
$001C_H$	Backplane Output Advancement Register 0, BOAR0
$001D_H$	Backplane Output Advancement Register 1, BOAR1
$001E_H$	Backplane Output Advancement Register 2, BOAR2
$001F_H$	Backplane Output Advancement Register 3, BOAR3
0020_H	Local Output Advancement Register 0, LOAR0
0021_H	Local Output Advancement Register 1, LOAR1
0022_H	Local Output Advancement Register 2, LOAR2
0023_H	Local Output Advancement Register 3, LOAR3
0024_H to 0026_H	Reserved
0027_H	Local BER Input Selection Register, LBIS
0028_H	Local BER Register, LBERR
0029_H	Backplane BER Input Selection Register, BBIS
$002A_H$	Backplane BER Register, BBERR
$002B_H$	DPLL Operation Mode Register 1, DOM1

Table 7 - Address Map For Internal Registers (A13 = 0)

A13 - A0	Location
$002C_H$	DPLL Operation Mode Register 2, DOM2
$002D_H$	DPLL Output Adjustment Register, DPOA
$002E_H$	DPLL House Keeping Register, DHKR

Table 7 - Address Map For Internal Registers (A13 = 0) (continued)

If A13 is high, the remaining address input lines are used to select the data and connection memory positions corresponding to the serial input or output data streams as shown in Table 8 on page 25.

The Control register (CR), the Device Mode Selection register (DMS) and the Block Programming Mode register (BPM) control all the major functions of the device. The DMS and BPM should be programmed immediately after system power up to establish the desired switching configuration as explained in the Frame Alignment Timing and Switching Configurations sections. The Control register is used to select Data or Connection Memory for microport operations, ST-BUS output frame and clock modes, and to set Memory Block Programing and Bit Error Rate Testing.

The Control register (CR) consists of the memory block programming bit (MBP) and the memory select bits (MS2-0). The memory block programming bit allows users to program the entire connection memory in two frames (see Memory Block Programming section). The memory select bits control the selection of the connection memories or the data memories. See Table 9 on page 46 for content of the Control register.

The DMS register consists of the backplane and the local mode selection bits (BMS, LG41 - LG40, LG32 - LG30, LG22 - LG20, LG12 - LG10 and LG02 - LG00) that are used to enable various switching modes for the backplane and the local interfaces respectively. See Table 10 on page 47 for the content of the DMS register.

The BPM register consists of the block programming data bits (LBPD2-0 and BBPD2-0) and the block programming enable bit (BPE). The block programming enable bit allows users to program the entire backplane and local connection memories in two frames (see Memory Block Programming section). If the ODE pin is low, the backplane CT-Bus is in input mode and the local output drivers are in high impedance state. If the ODE pin is high, all the backplane CT-Bus and local ST-BUS output drivers are controlled on a per channel basis by backplane and local connection memories, respectively. By programming BTM2 through BTM0 bits to “110” in the backplane connection memory, the user can control the per-channel input on the backplane interface. For the local interface, users can program LTM2 -0 bits to “110” in the local connection memory to control the per-channel high impedance output on the local ST-BUS. See Table 11 on page 49 for the content of the BPM register.

A13 (Note 1)	Stream Address (ST0-31)						Channel Address (Ch0-255)								
	A12	A11	A10	A9	A8	Stream #	A7	A6	A5	A4	A3	A2	A1	A0	Channel #
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	Ch 63 (Note 3 & 6)
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	1	1	1	1	1	1	0	Ch 126
1	1	1	0	1	1	Stream 27	0	1	1	1	1	1	1	1	Ch 127 (Note 4 & 7)
1	1	1	1	0	0	Stream 28	.	.	.	.	.	.	.	.	.
1	1	1	1	0	1	Stream 29	.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	Stream 30	1	1	1	1	1	1	1	0	Ch 254
1	1	1	1	1	1	Stream 31	1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Notes:
1. Bit A13 must be high for access to data and connection memory positions. Bit A13 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2 Mb/s.
3. Channels 0 to 63 are used when serial stream is at 4 Mb/s.
4. Channels 0 to 127 are used when serial stream is at 8 Mb/s.
5. Channels 0 to 255 are used when serial stream is at 16 Mb/s.
6. Channels 0 to 63 are used when local serial stream is in 4-bit wide sub-rate switching mode.
7. Channels 0 to 127 are used when local serial stream is in 2-bit wide sub-rate switching mode.

Table 8 - Address Map for Memory Locations (A13 = 1)

12.0 Backplane Connection Memory

The backplane connection memory controls the switching configuration of the backplane interface. Locations in the backplane connection memory are associated with particular STio streams.

The BTM2 - 0 bits of each backplane connection memory allows the per-channel selection for the message or the connection mode, the constant or the variable delay mode, the high impedance control of the STio driver or the bit error test enable. See Table 25 on page 63 for the content per-channel control function.

In the switching mode, the contents of the backplane connection memory stream address bits (BSAB4-0) and channel address bits (BCAB7-0) define the source information (stream and channel) of the time slot that will be switched to the backplane STio streams. During the message mode, only the lower 8 bits (8 least significant bits) of the backplane connection memory will be transferred to the STio pins.

13.0 Local Connection Memory

The local connection memory controls the local interface switching configuration. Local connection memory is split into a high and a low part. Locations in the local connection memory are associated with particular STo output streams.

The LTM2 - 0 bits of each local connection memory low allows the per-channel selection for the message or the connection mode, the constant or the variable delay mode, the high impedance control of the STo driver or the bit error test enable. See Table 29 on page 65 for the content per-channel control function.

In the switching mode, the contents of the local connection memory low stream address bits (LSAB4-0) and the channel address bits (LCAB7-0) of the local connection memory defines the source information (stream and

channel) of the time slot that will be switched to the local STo streams. During the message mode, only the lower 8 bits (8 least significant bits) of the local connection memory low bits are transferred to the STo pins.

In the sub-rate switching mode, although the output channels are divided up into 2 or 4-bit channels, the input streams still have 8-bit channel boundaries. Therefore, it is necessary to indicate which bits in the input 8-bit channel will be switched out to the 2 or 4-bit channel. When 2-bit or 4-bit sub-rate switching is enabled, the LSRS1-0 bits in the local connection memory high define which bit positions contains the sub-rate data.

14.0 Bit Error Rate Test

The MT90866 offers users a Bit Error Rate (BER) test feature for the backplane and the local interfaces. The circuitry of the BER test consists of a transmitter and a receiver on both interfaces that can transmit and receive the BER patterns independently. The transmitter can output a pseudo random patterns of the form 2^{15} - 1 to any channel and any stream within a frame time. For the test, users can program the output channel and stream through the backplane or local connection memory and the input channel and stream using Local or Backplane BER Input Selection (BIS) registers. See Table 16 on page 54 and Table 18 on page 54 for the LBIS and the BBIS registers contents, respectively.

The receiver receives the BER pattern and does an internal BER pattern comparison. For backplane interface, the comparison result is stored in the Backplane BER register (BBERR). For local interface, the result is stored in the Local BER register (LBERR).

15.0 External Tristate Control

The MT90866 has the flexibility to provide users with the choice of external per-channel tristate control. Two control signals are provided. For the backplane interface, it is the BCSTo output. For the local interface, it is the LCSTo output. Each control signal has a data rate of 32.768 Mb/s with 4,096 control bits per frame. Each bit position corresponds to a specific output stream and channel location. When the control bit is high, the corresponding output channel is in the high impedance state, whereas when the control bit is low, the corresponding output channel has active output data.

15.1 BCSTo Control Stream

When the STio0-31 streams are in the 8 Mb/s mode, the STio0_Ch0 control bit of the BCSTo stream is advanced by thirty-six C32/64o 32.768 Mb/s clock cycles from the backplane frame boundary. See Figure 6, "Backplane Control (BCSTo) Timing when the STio data rate is 8 Mb/s" on page 26 for the BCSTo control bit pattern.

When the STio0-15 streams are in the 16 Mb/s mode, the STio0_Ch0 control bit of the BCSTo is advanced by thirty-six C32/64o 32.768 Mb/s clock cycles from the backplane frame boundary. See Figure 7, "Backplane Control (BCSTo) Timing when the STio data rate is 16 Mb/s" on page 27 for the BCSTo control bit pattern.

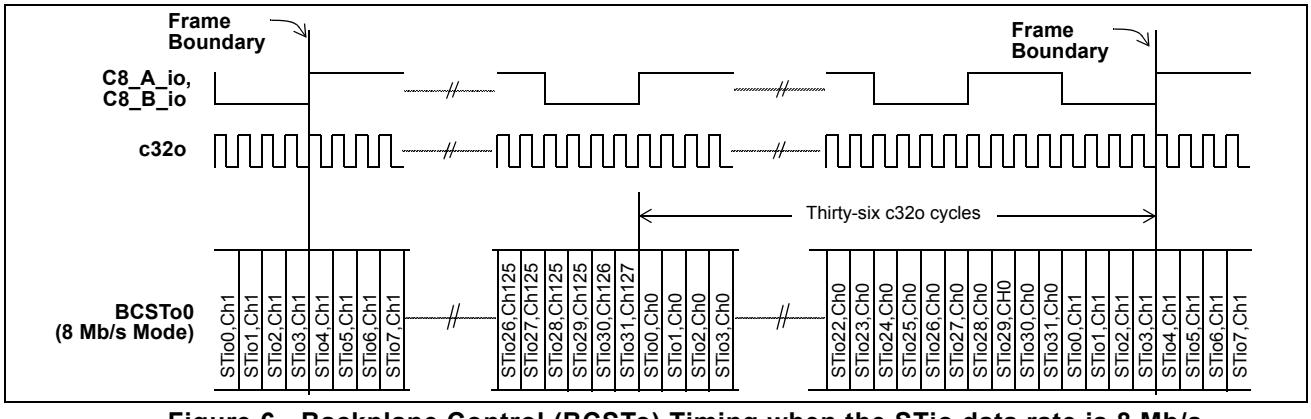


Figure 6 - Backplane Control (BCSTo) Timing when the STio data rate is 8 Mb/s

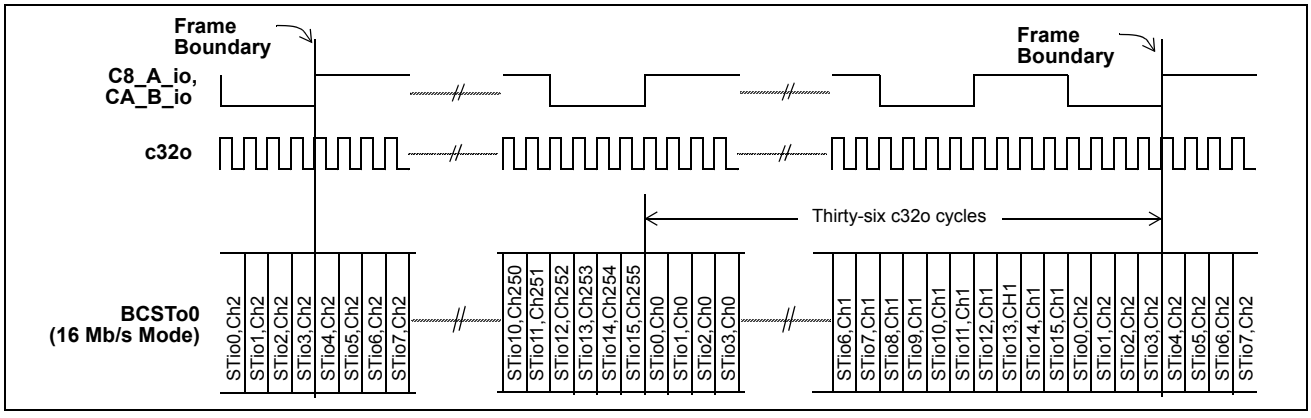


Figure 7 - Backplane Control (BCSTo) Timing when the STio data rate is 16 Mb/s

15.2 LCSTo Control Stream

The LCSTo control bits are partitioned into 128 time slots, Slots 0 to 127. Each slot has 32 bits. Dummy bits represent logic levels which should be ignored by the users. The first control bit in Slot 0 is advanced by thirty-two C32/64o 32.768 Mb/s clock cycles from the frame boundary. See Figure 8, "Local Control (LCSTo) Timing when STo0-18 are operated at 8 Mb/s" on page 28 for the partition of the time slots and the frame alignment details.

When the STo0-18 streams are operated at 8 Mb/s, Slots 0 to 127 are used to represent the control bits for Channels 0 to 127 of the 8 Mb/s streams. STo19-17 are driven low in this configuration. See Figure 8, "Local Control (LCSTo) Timing when STo0-18 are operated at 8 Mb/s" on page 28 for the LCSTo control bit pattern.

When the STo0-18 streams are operated at 4 Mb/s, Slots 2N (where N = 0 to 63) have the control bit pattern but Slots 2N+1 have dummy bits which should be ignored by the user. STo19-17 are driven low in this configuration. See Figure 9, "Local Control (LCSTo) Timing when STo0-18 are operated at 4 Mb/s" on page 29 for the LCSTo control bit pattern.

When the STo0-27 streams are operated at 2 Mb/s, Slots 4N (where N = 0 to 31) have the control bit pattern, but Slots 4N+1, 4N+2 and 4N+3 have dummy bits. See Figure 10, "Local Control (LCSTo) Timing when all STo0-27 are operated at 2 Mb/s" on page 30 for the LCSTo control bit pattern.

When the STo streams are programmed with various data rates as described in Table 6 on page 20, the available control bit positions in every time slot is associated with the corresponding output stream channels which operate at various data rates. Figure 11, "Example of Local Control (LCSTo) Timing when the Local Streams have Different Data Rates" on page 31 gives an example when STo0-3, 4-7, 8-11, 12-15, 16-27 are programmed to operate at 8 Mb/s, 4 Mb/s, 8 Mb/s, 4 Mb/s and 2 Mb/s respectively.

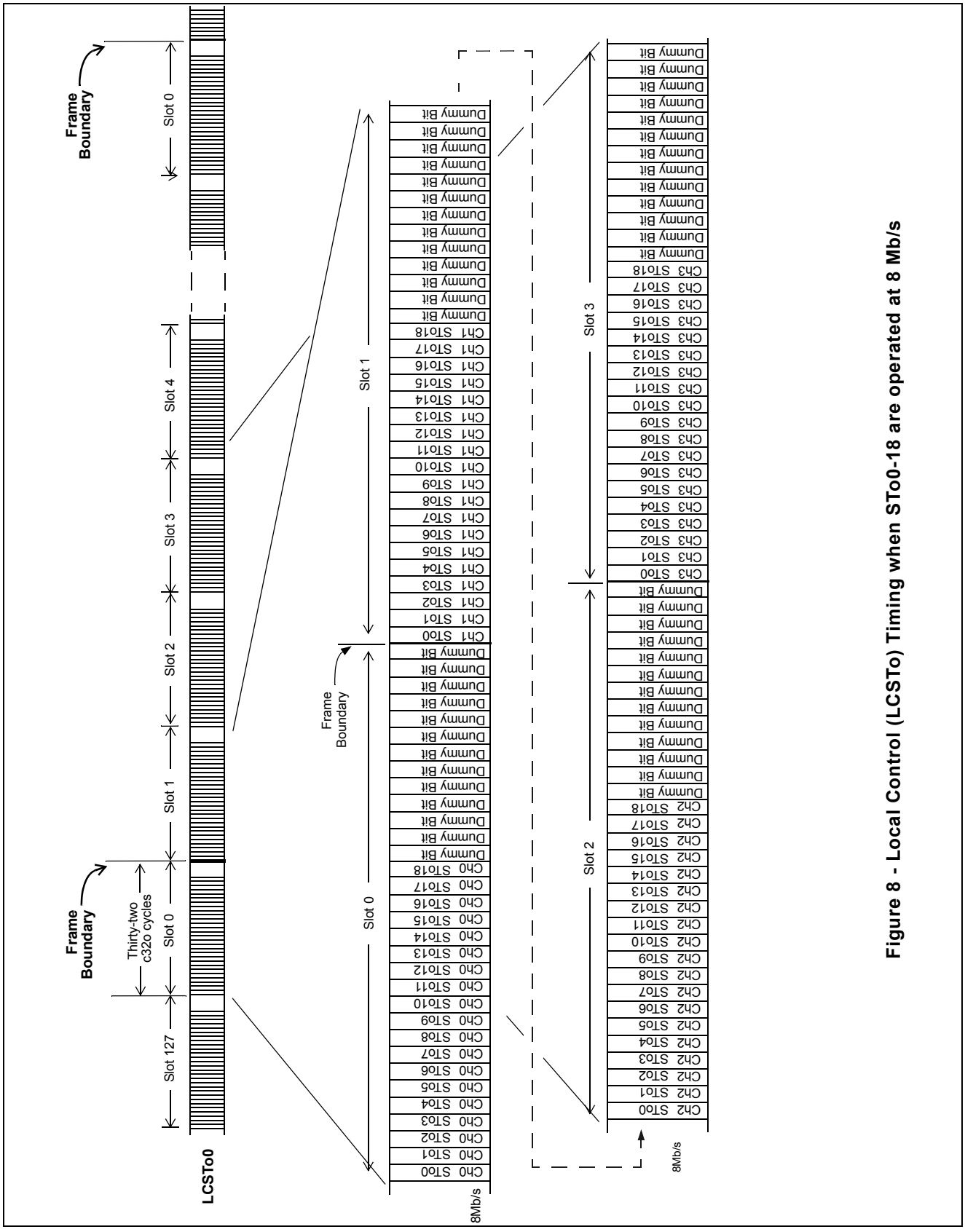


Figure 8 - Local Control (LCSTo) Timing when STo0-18 are operated at 8 Mb/s

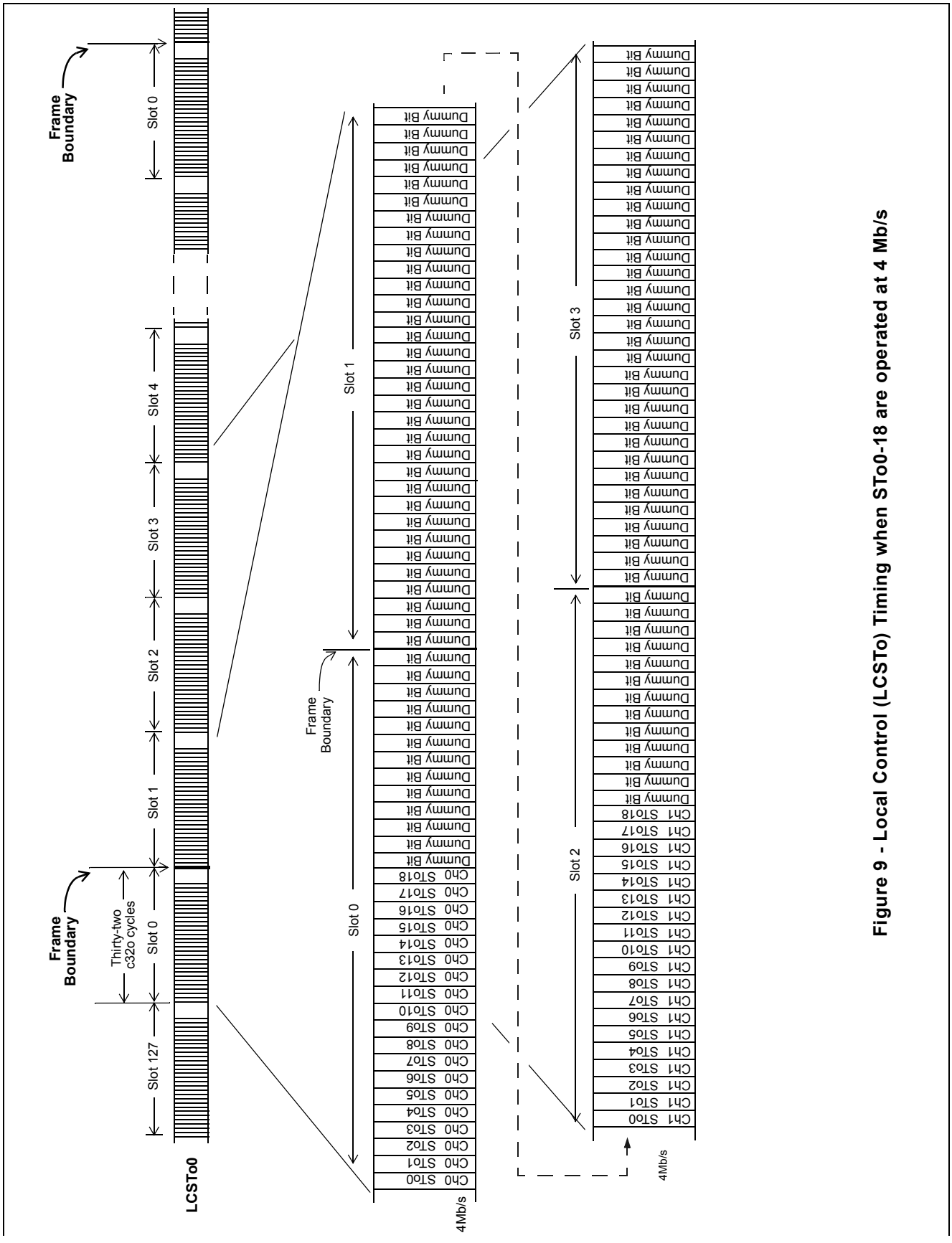


Figure 9 - Local Control (LCSTo) Timing when STo0-18 are operated at 4 Mb/s

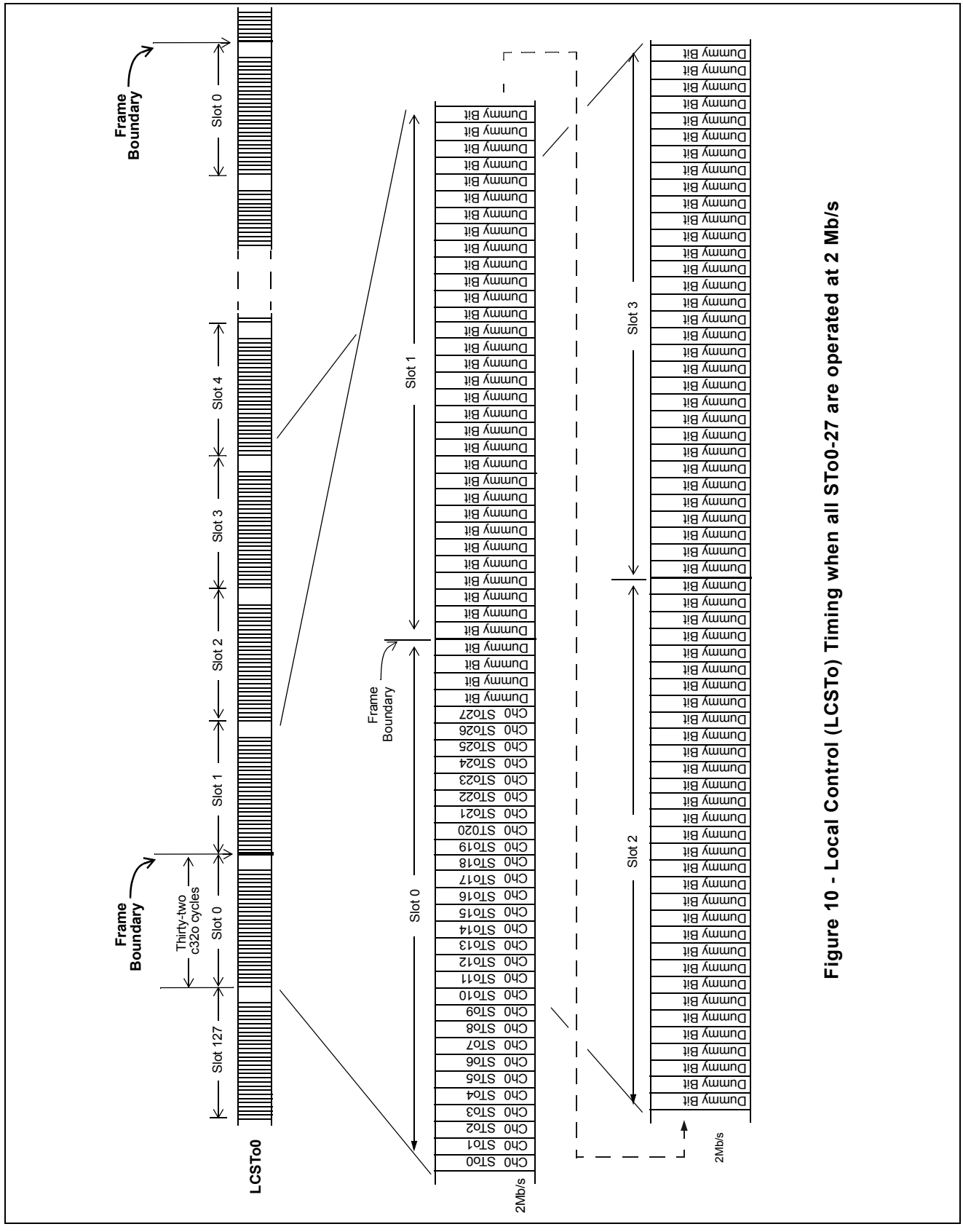


Figure 10 - Local Control (LCSTo) Timing when all STo0-27 are operated at 2 Mb/s

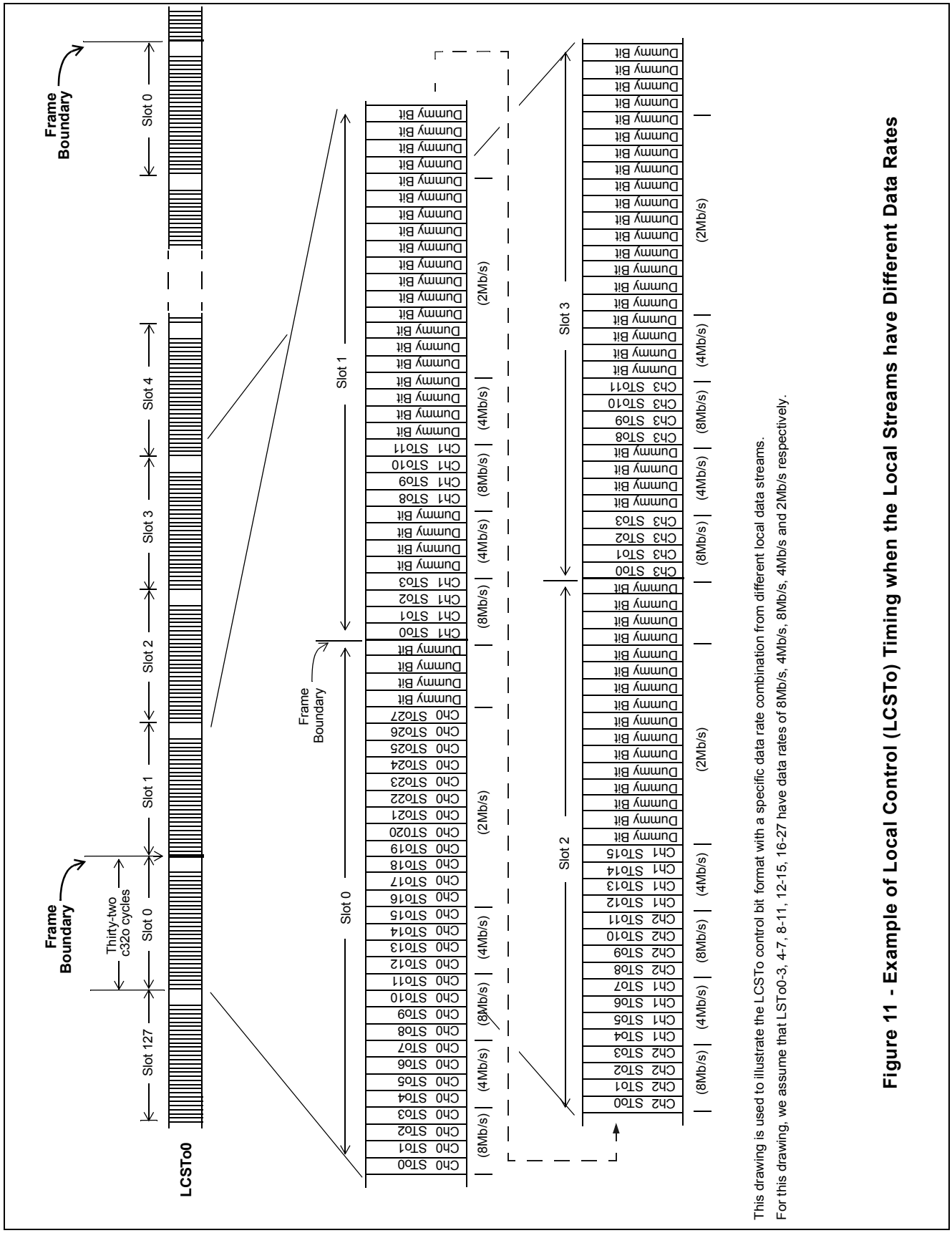


Figure 11 - Example of Local Control (LCSTo) Timing when the Local Streams have Different Data Rates

This drawing is used to illustrate the LCSTo control bit format with a specific data rate combination from different local data streams.

For this drawing, we assume that LSTo0-3, 4-7, 8-11, 12-15, 16-27 have data rates of 8Mb/s, 4Mb/s, 8Mb/s, 4Mb/s and 2Mb/s respectively.

16.0 DPLL

The Digital Phase Locked Loop (DPLL) accepts selectable 1.544 MHz, 2.048 MHz, or 8 kHz input reference signals. It accepts reference inputs from independent sources and provides bit-error-free reference switching. The DPLL meets phase slope and MTIE requirements defined by the Telcordia GR-1244-CORE standard.

The DPLL also provides the timing for the rest of the MT90866 Digital Switch, generating several network clocks with the appropriate quality. Clocks are synchronized to one of two input reference clocks and meet the requirements of the H.110 clock specification.

The master clock (CLK80M) for the DPLL is provided by the Analog Phase Locked Loop (APLL) from the MT90866 master clock input pin C20i. Since the APLL output is “locked” to the input, the accuracy of CLK80M clock is equal to the accuracy of C20i.

16.1 MT90866 Modes of Operation

The DPLL, and consequently the MT90866, can, as required by the H.110 standard, operate in three different modes: Primary Master, Secondary Master and Slave. See Figure 12, "Typical Timing Control Configuration" on page 32.

To configure the DPLL, there are two Operation Mode registers: DOM1 and DOM2. See Table 20 on page 55 and Table 21, "DPLL Operation Mode (DOM2) Register Bits" on page 58 for the contents of these registers.

In all modes the MT90866 monitors both the “A Clocks” (C8_A_io and FRAME_A_io) and the “B Clocks” (C8_B_io and FRAME_B_io). The Fail_A and the Fail_B signals indicate the quality of the “A Clocks” and “B Clocks” respectively.

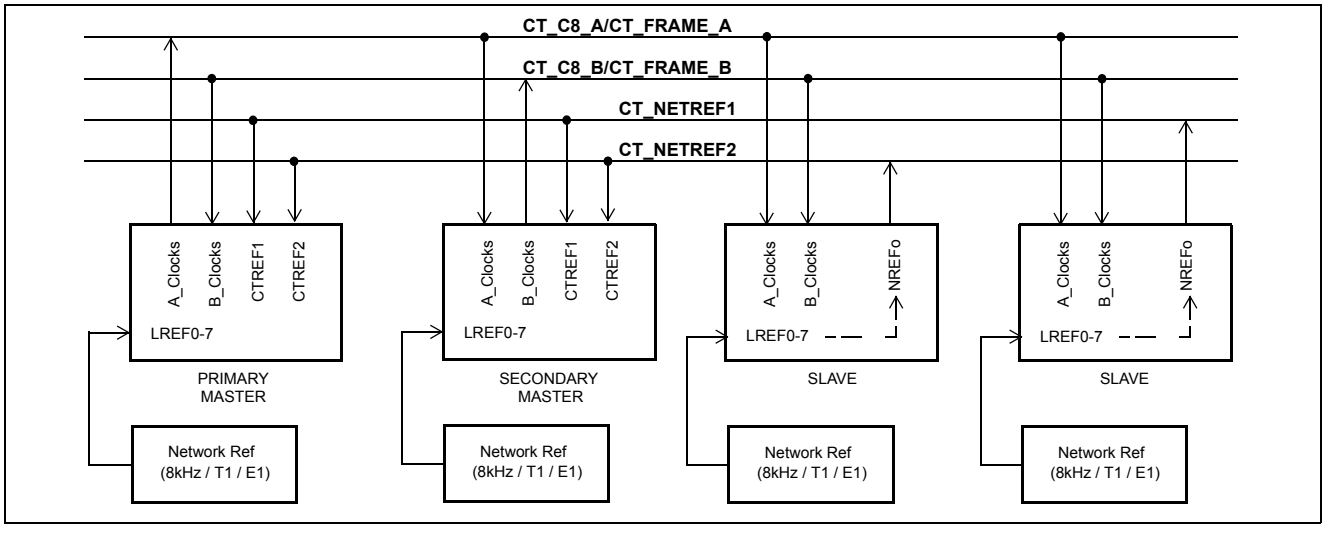


Figure 12 - Typical Timing Control Configuration

16.1.1 Primary Master Mode

In the Primary Master Mode, the MT90866 drives the “A Clocks” (C8_A_io and FRAME_A_io), by locking to the primary reference (PRI_REF). The PRI_REF can be provided by one of the locally derived network reference sources (LREF0-7), or the CTREF1 input or the CTREF2 input. In this mode the MT90866 has the ability to monitor the primary reference. If the primary reference becomes unreliable, the device continues driving “A Clocks” in stable Holdover Mode until it makes a **Stratum 4 Enhanced** compatible switch to the secondary reference (SEC_REF) for its network timing. The secondary reference can be provided by one of the local network references (LREF0-7), the CTREF1 or the CTREF2.

If the primary reference comes back or recovers, the MT90866 makes a **Stratum 4 Enhanced** compatible switch back to the original primary reference and the system returns to normal operation state.

If necessary, the MT90866 can be prevented from switching back to the original primary reference by programming the RPS bit in DOM1 register to give preference to the secondary reference.

While in the Primary Master mode, the MT90866 attenuates jitter and wander above 1.52 Hz from the selected input reference clock and generates all output clocks according to the DPLL jitter transfer function diagram on Figure 17, "DPLL Jitter Transfer Function Diagram - wide range of frequencies" on page 42 and Figure 18, "Detailed DPLL Jitter Transfer Function Diagram" on page 43.

For the Primary Master mode selection, see Table 22, "MT90866 Mode Selection - By Programming DOM1 and DOM2 Registers" on page 60.

16.1.2 Secondary Master Mode

In the Secondary Master Mode, the MT90866 drives the “B Clocks” (C8_B_io and FRAME_B_io), by locking to the “A Clocks”. As required by the H.110 standard, the “B Clocks” are edge-synchronous with the “A Clocks”, as long as jitter on the “A Clocks” meets Telcordia GR-1244-CORE specifications.

If the “A Clocks” become unreliable, system software is notified and the MT90866 continues driving the “B Clocks” in stable Holdover Mode until it makes a **Stratum 4 Enhanced** compatible switch to the secondary reference (SEC_REF) for its network timing. The secondary reference can be the local network reference (LREF0-7), the CTREF1 or the CTREF2. If the “A Clocks” can not recover, the designated secondary master can be promoted to primary master by system software. This promotion will cause the “B Clocks” to assume the role of the “A Clocks”.

For the Secondary Master mode selection, see Table 22, "MT90866 Mode Selection - By Programming DOM1 and DOM2 Registers" on page 60.

16.1.3 Slave Mode

In the Slave Mode, the MT90866 is phase locked to the “A Clocks”. If the “A Clocks” become unreliable, the device goes to stable Holdover Mode until it makes a **Stratum 4 Enhanced** compatible switch to the “B Clocks”. The MT90866 will perform all required functionality as long as the “A Clocks” and the “B Clocks” conform to the Telcordia GR-1244-CORE jitter specifications.

In addition, the device can be used to generate a CT reference (CT_REF1 or CT_REF2) from its network references, LREF0-7.

While the device is in Slave Mode and the “A Clocks” or the “B Clocks” do not recover, then the designated slave can be promoted to secondary master by system software. In that case, the network reference can be used as the secondary reference.

Table 22 on page 60 shows how to program the DOM1 and DOM2 registers to enable the Slave mode of the MT90866.

17.0 DPLL Functional Description

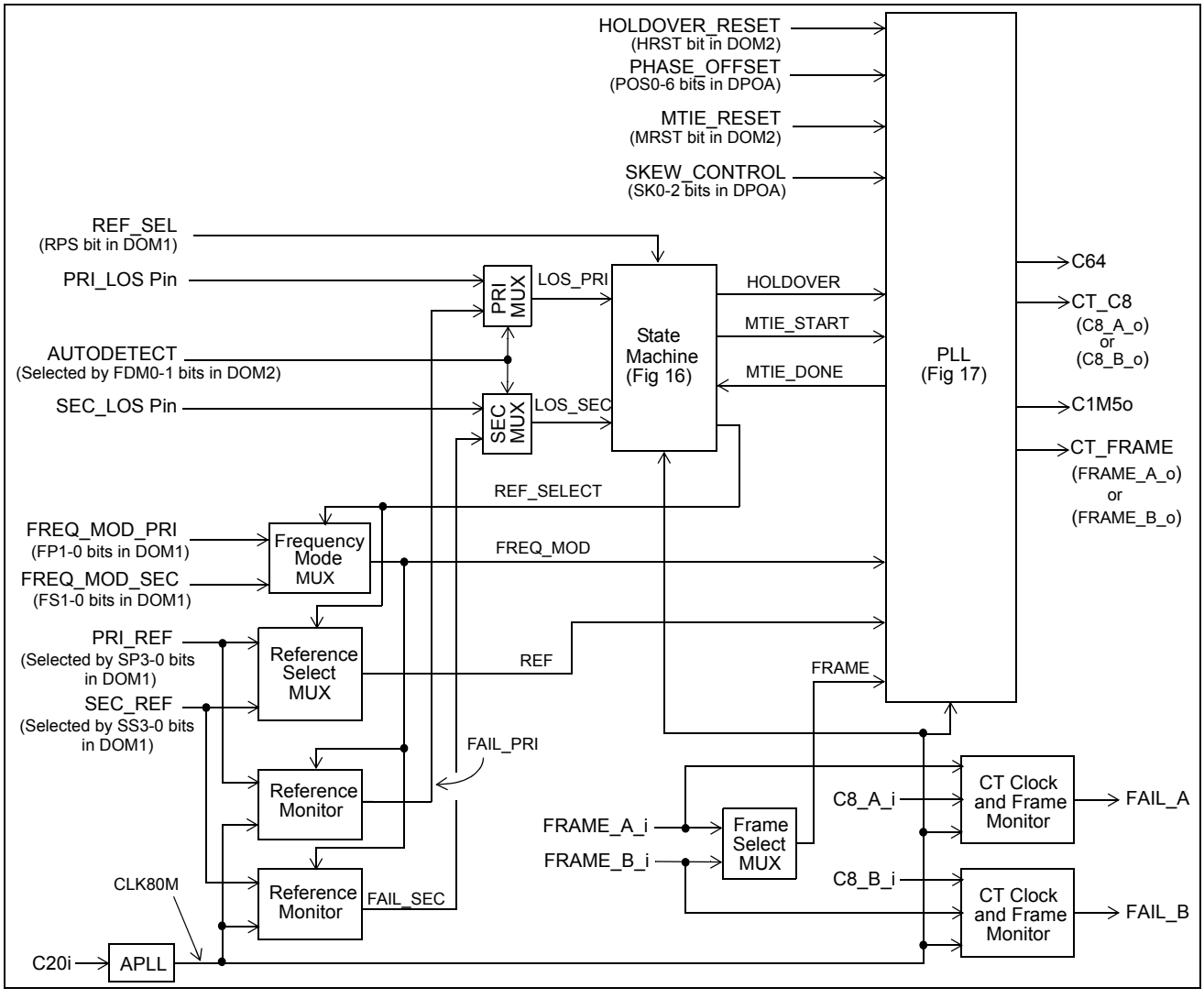


Figure 13 - DPLL Functional Block Diagram

17.1 Reference Select and Frequency Mode MUX Circuits

The DPLL accepts two simultaneous reference input signals and operates on their rising edges. Either the primary reference (PRI_REF) signal or the secondary reference (SEC_REF) signal can be selected to be the reference signal (REF) to the PLL circuit. The appropriate frequency mode input (either FREQ_MOD_PRI or FREQ_MOD_SEC) is selected to be the input of the PLL Circuit. The selection is done by the State Machine Circuit based on the current state.

The FREQ_MOD_PRI and the FREQ_MOD_SEC are 2-bit wide inputs which reflect the value in the FP1-0 and FS1-0 bits of the DOM1 register. The primary and the secondary references operate independently from each other and can have different frequencies. Switching the reference from one frequency to another does not require the device reset to be applied. Table 20 on page 55 shows input frequency selection for the primary and secondary reference respectively.

17.2 PRI and SEC MUX Circuits

The DPLL has four different modes to handle reference failure. These modes are selected by the FDM0 and FDM1 bits of the DOM2 Register. If FDM1-0 is ’10’ then the Primary reference is always used regardless of failures. If FDM1-0 is ’11’ then the Secondary reference is always used regardless of failures. Otherwise the DPLL operates in one of two failure detection modes: Autodetect or Manual detection mode. When the FDM0 and FDM1 bits are set to low in the DOM2 register ‘00’, the DPLL is in the Autodetect Mode. In this mode, the outputs from the Reference Monitor Circuits LOS_PRI and LOS_SEC are used by the State Machine Circuit. When the FDM0 bit is set to high and FDM1 bit is set to low ‘01’, the DPLL is in the Manual Detection Mode and the LOS_PRI and LOS_SEC signals are selected from the PRI_LOS and SEC_LOS input pins to be used by the State Machine Circuit. See Table 21 on page 58 for selection of the Failure Detection Modes.

17.3 Frame Select MUX

When the “A Clocks” or the “B Clocks” are selected as the input reference, an 8.192 MHz clock (either C8_A_io or C8_B_io) is provided to be the input reference to the PLL circuit (REF). Because the output frame pulse (CT_FRAME) must be aligned with the selected input frame pulse, the appropriate frame pulse (either FRAME_A_io or FRAME_B_io) is selected in the Frame Select MUX circuit to be the input of the PLL circuit (FRAME).

17.4 CT Clock and Frame Monitor Circuits

The CT Clock and Frame Monitor circuits check the period of the C8_A_io and the C8_B_io clocks and the FRAME_A_io and FRAME_B_io frame pulses. According to the H.110 specification, the C8 period is 122 ns with a tolerance of +/- 35 ns measured between rising edges. If C8 falls outside the range of [87 ns,157 ns], the clock is rejected and the fail signal (FAIL_A or FAIL_B) becomes high. The Frame pulse period is measured with respect to the C8 clock. The frame pulse period must have exactly 1024 C8 cycles. Otherwise, the fail signal (FAIL_A or FAIL_B) becomes high. When the CT BUS clock and frame pulse signals return to normal, the FAIL_A or FAIL_B signal returns to logic low.

17.5 Reference Monitor Circuits

There are two Reference Monitor Circuits: one for the primary reference (PRI_REF) and one for the secondary reference (SEC_REF). These two circuits monitor the selected input reference signals and detect failures by setting up the appropriate fail outputs (FAIL_PRI and FAIL_SEC). These fail signals are used in the Autodetect mode as the LOS_PRI and LOS_SEC signals to indicate when the reference has failed. The method of generating a failure depends on the selected reference.

When the selected reference frequency is 8.192 MHz (“A Clocks” or “B Clocks”), the fail signals are passed through from the CT Clock and Frame Monitor circuit outputs FAIL_A and FAIL_B, and used directly as FAIL_PRI and FAIL_SEC, accordingly.

For all other reference frequencies (8 kHz, 1.544 MHz and 2.048 MHz), the following checks are performed:

- For all references, the “minimum 90 ns” check is done. This is required by the H.110 specifications - both low level and high level of the reference must last for minimum 90 ns each.
- The “period in the specified range” check is done for all references. The length of the period of the selected input reference is checked if it is in the specified range. For the E1 (2.048 MHz clock) or the T1 (1.544 MHz clock) reference, the period of the clock can vary within the range of 1 +/- 1/4 of the defined clock period which is 488 ns for the E1 clock and 648 ns for T1 clock. For the 8 KHz reference, the variation is from 1 +/- 1/32 period.
- If the selected reference is E1 or T1, “64 periods in the specified range” check is done. The selected reference is observed for a long period (64 reference clock cycles) and checked if it is within the specified range - from 62 to 66 clock periods.

These reference signal verifications include a complete loss or a large frequency shift of the selected reference signal. When the reference signal returns to normal, the LOS_PRI and LOS_SEC signals will return to logic low.

17.6 State Machine Circuit

The State Machine handles the reference selection. Depending on REF_SEL and LOS signals (selection between FAIL_PRI and PRI_LOS and between FAIL_SEC and SEC_LOS), the state machine selects PRI_REF or SEC_REF as the current input reference and dictates the PLL Circuit mode: Normal or Holdover Mode. In the Normal Mode, the DPLL output clocks are locked to the selected input reference (PRI_REF or SEC_REF). In the Holdover Mode, the DPLL clocks retain the phase and frequency values they had 32 to 64 ms prior to moving from the Normal to the Holdover Mode. When going from the Holdover to the Normal Mode, the State Machine activates the MTIE circuit and goes through the states MTIE PRI or MTIE SEC to prevent a phase shift of the output clocks during the DPLL reference switch (from PRI_REF to SEC_REF and vice versa). The state diagram is given in Figure 14, "State Machine Diagram" on page 36.

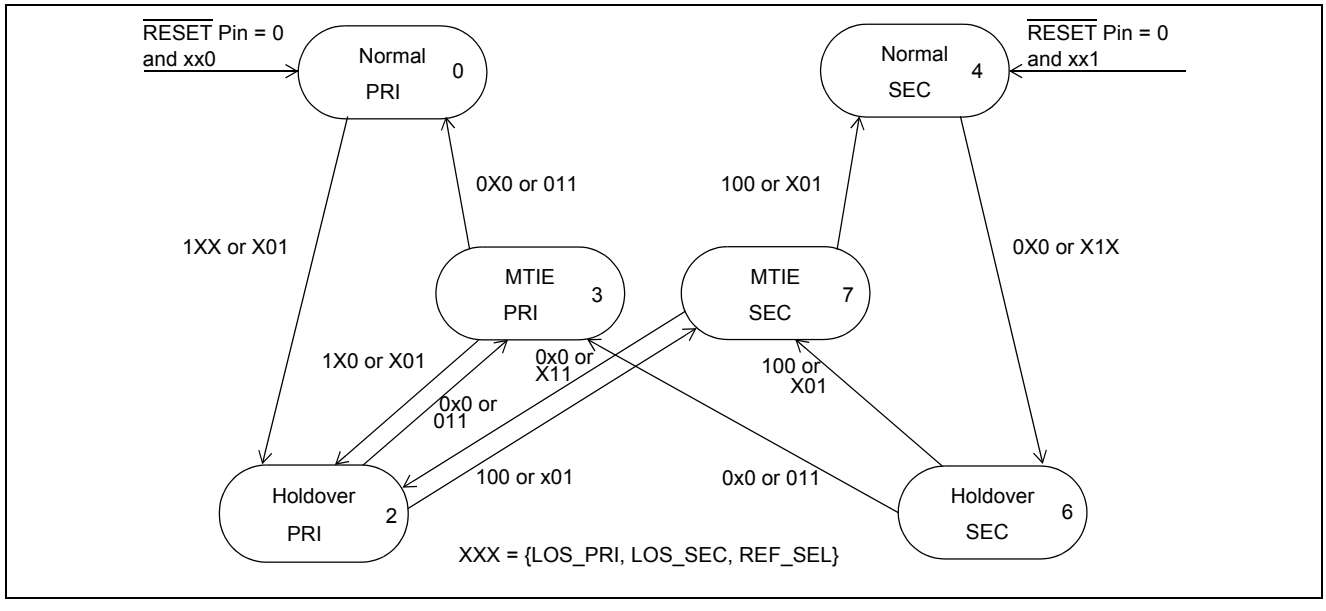


Figure 14 - State Machine Diagram

18.0 Phase Locked Loop (PLL) Circuit

As shown in Figure 15, "Block Diagram of the PLL Module" on page 37, the PLL module consists of a Skew Control, Maximum Time Interval Error (MTIE), Phase Detector, Phase Offset Adder, Phase Slope Limiter, Loop Filter, Digitally Controlled Oscillator (DCO), Divider and Frequency Select MUX modules.

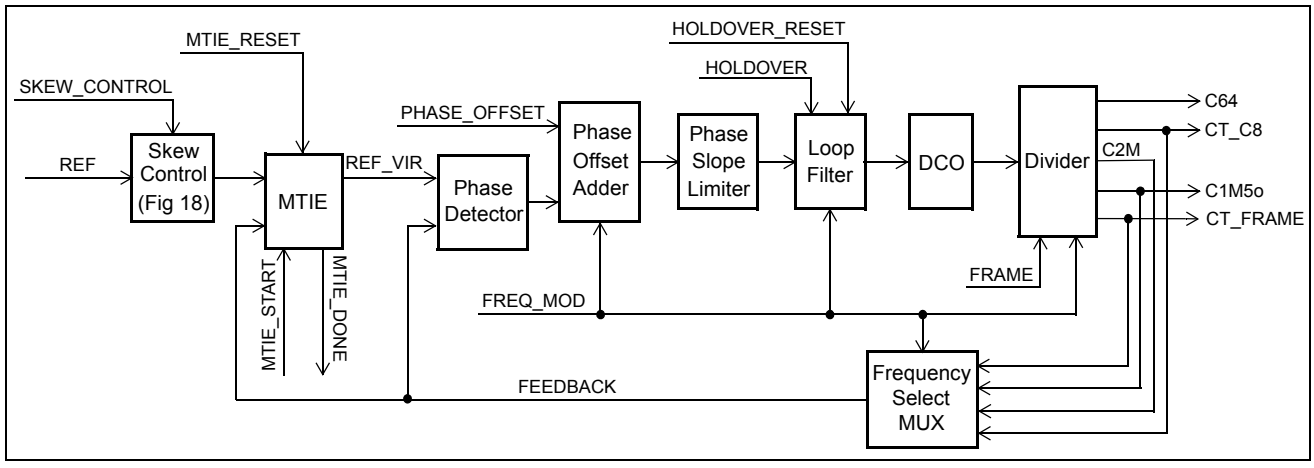


Figure 15 - Block Diagram of the PLL Module

18.1 Skew Control

The circuit delays a selected reference input with a tapped delay line with seven taps - see Figure 16, "Skew Control Circuit Diagram" on page 37. The maximum delay of the per unit delay element is factored at intervals of 3.5 ns. The tap is selected by the SKEW_CONTROL bus which is programmed by the SKC2-SKC0 bits of the DPLL Output Adjustment (DPOA) register. The skew of this input will result in a static phase offset which varies from 0 to 7 steps of the maximum delay per unit delay element, between the input and the outputs of the DPLL.

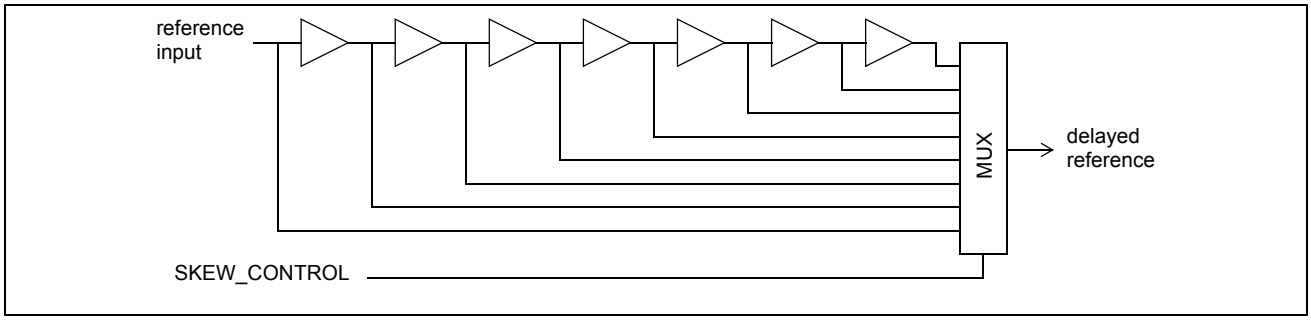


Figure 16 - Skew Control Circuit Diagram

18.2 Maximum Time Interval Error (MTIE)

The MTIE circuit prevents any significant change in the output clock phase during a reference switch. Because the input references can have any relationship between their phases and the output follows the selected input reference, any switch from one reference to another could cause a large phase jump in the output clock if such a circuit did not exist. This large phase jump could cause significant data loss. The MTIE circuit keeps the phase difference between the output clock of the DPLL and the input reference the same as if the reference switch had not taken place.

The MTIE circuit has two modes:

- Measuring mode - the circuit measures the phase difference between the new reference from the Skew Control circuit and the feedback signal (FEEDBACK) from the Frequency Select MUX circuit. This mode is active during the movement of the DPLL from the Holdover to the Normal Mode, and is set by the MTIE_START signal of the State machine module. The measured value is stored into a counter and used in the Delay mode. When the measurement process is done, the State Machine module is notified by generating the MTIE_DONE signal, allowing it to go to the Normal Mode.

- Delay mode - after the rising edge of the new reference clock from the Skew Control circuit, the MTIE circuit uses the measured value to generate the virtual reference pulse (REF_VIR) to the Phase Detector circuit. While the DPLL is in the Normal Mode, the MTIE Circuit is in Delay mode. It keeps the phase difference between the output signals of the DPLL and selected input reference as the previous output signal would have been if the reference switch had not taken place.

During a reference switch, the State Machine module first changes the mode of the DPLL from the Normal to the Holdover Mode. In the Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates very accurate outputs using storage techniques.

Because the input reference coming from the Skew Control circuit is asynchronous to the sampling clock used in the MTIE circuit, a phase error may exist between the selected input reference signal and the output signal of the DPLL. In the worst case, the Maximum Time Interval Error (MTIE) is one period of the internally used clock cycle (65.536 MHz if the selected reference frequency is 8 kHz, 2.048 MHz and 8.192 MHz, and 49.408 MHz when the selected reference frequency is 1.544 MHz). This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between the input signal and the output signal can change. The value of this delay is the accumulation of the error measured during each reference switch. After many switches from one reference to another, the delay between the selected input reference and the DPLL output clocks can become unacceptably large. The user should provide MTIE reset (set MRST bit in the DOM2 register to high) causing output clocks to align to the nearest edge of the selected input reference. It is recommended that the MTIE is reset after multiple reference switchings and the device falls back to its initial reference. The MTIE **MUST** be kept in the reset mode when the ZL50031 is operating in the slave mode.

18.3 Phase Detector

The Phase Detector circuit compares the virtual reference signal from the MTIE Circuit (REF_VIR) with the feedback signal from the Frequency Select MUX circuit (FEEDBACK) with respect to their rising edges, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Phase Offset Adder Circuit. The Frequency Select MUX allows the proper feedback signal to be selected (e.g., 8 kHz, 1.544 MHz, 2.048 MHz or 8.192 MHz).

18.4 Phase Offset Adder

The Phase Offset Adder Circuit adds the PHASE_OFFSET word (bits POS6-POS0 of the DPLL Output Adjustment register - see Table 23 on page 61) to the error signal from the Phase Detector circuit to create the final phase error. This value is passed to the Phase Slope Limiter circuit. The PHASE_OFFSET word can be positive or negative. Since the PLL will stabilize to a situation where the average of the sum of the phase offset word and the phase detector output is zero, a nonzero value in the input of the Phase Offset Adder circuit will result in a static phase offset between the input and output signals of the DPLL.

If the selected input reference of the DPLL is either 8 KHz or 2.048 MHz, the step size in this static phase offset is 15.2 ns. With a 7-bit 2's complement value, the static phase offset can be set between -0.96 μs and +0.97 μs. If the selected input reference of the DPLL is 1.544 MHz, the maximum phase offset is between -1.27 μs and 1.29 μs with a resolution of 20.2 ns.

Together with the Skew Control bits (SKC2-SKC0), users can program a static phase offset between -960 ns and +990 ns if the selected input reference of the DPLL is either 8 kHz or 2.048 MHz. If the selected reference is 1.544 MHz, the programmable phase offset is between -1.27 μs and 1.30 μs. For the programmable ranges mentioned above, the resolution is 1.9 ns per step. See Table 23 on page 61 for the content of the DPOA register.

When the selected input reference frequency of the DPLL is 8.192 MHz ("A Clocks" or "B Clocks" are selected as the reference), the Phase Offset Adder is bypassed. The output of the Phase Detector circuit is connected directly to the input of the Phase Slope Limiter circuit. When an 8.192 MHz clock (C8_A_io or C8_B_io) is used as the reference in the Secondary Master or the Slave mode, the H.110 standard requires the output clock to always follow the input reference on an edge-to-edge basis, so the static phase offset is not required.

18.5 Phase Slope Limiter

The limiter receives the error signal from the Phase Offset Adder circuit and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 7.6 ns per 125 us. Because of this slope, the MT90866 is within the maximum phase slope of 81 ns per 1.326 ms specified by the Telcordia GR-1244-CORE standard.

The frequency stability of the Holdover Mode is ±0.07 ppm, which translates to a worst case 49 frame (125 μs) slips in 24 hours. This is better than the Telcordia GR-1244-CORE Stratum 3 requirement of ±0.37 ppm (255 frame slips per 24 hours).

18.6 Loop Filter

The Loop Filter circuit gives frequency offset to the DCO circuit, based on the phase difference between the input and the feedback reference. It is similar to a first order low pass filter, with two positions for cut-off frequency (-3 dB attenuation) depending on the selected reference frequency, and it mainly determines the jitter transfer function of the DPLL.

In Primary Master mode when the selected input reference frequency is either 2.048 MHz, 1.544 MHz or 8 kHz, the cut-off frequency is approximately at 1.52 Hz and all the reference variations, including jitter, are attenuated according to the DPLL jitter transfer function (see Figure 17, "DPLL Jitter Transfer Function Diagram - wide range of frequencies" on page 42 and Figure 18, "Detailed DPLL Jitter Transfer Function Diagram" on page 43). The Loop Filter circuit ensures that the jitter transfer requirements in ETS 300-011 and Telecordia GR-499-CORE are met when the selected reference frequency is either 2.048 MHz, 1.544 MHz or 8 kHz.

When the selected input reference frequency is 8.192 MHz (i.e., in Secondary Master or Slave modes), the reference variations are bypassed to the output clocks. The cut-off frequency is at about 100 kHz, well beyond 500 Hz, the corner frequency of the Telcordia GR-1244-CORE input jitter tolerance curve.

The storage techniques, which enable generating very accurate output frequencies during the Holdover Mode of DPLL, are built into the Loop Filter circuit. When no jitter is presented on the selected input reference, the holdover frequency stability is 0.007 ppm.

18.7 Digitally Controlled Oscillator (DCO)

The DCO circuit adds frequency offset from the Loop Filter, which represents the phase error between the input and the feedback reference, to the ideal center frequency value and generates appropriately corrected output high speed clock. The Synchronization method of the DCO is dependent on the state of the DPLL State Machine module.

In the Normal Mode, the DCO circuit provides an output signal which is frequency and phase locked to the selected input reference signal.

In the Holdover Mode, the DCO circuit is running at a frequency that is equal to the frequency which was generated by the DCO circuit when the DPLL was in the Normal Mode.

In the Freerun Mode, the DCO circuit is free running at its center frequency with an output accuracy equal to the accuracy of the device master clock (C20i).

18.8 Divider

The Divider Circuit divides the DCO output frequency down to the required outputs. The following outputs are generated:

- C64 (65.536 MHz clock) - used as the internal clock for the MT90866 device.
- CT_C8 (8.192 MHz clock), C2M (2.048 MHz clock), C1M5o (1.544 MHz clock) and CT_FRAME (8 kHz negative frame pulse) - feedback reference signals to the Frequency Select MUX Circuit.

The CT_FRAME and the CT_C8 are required clocks. C1M5o is provided as an output clock of the MT90866.

The duty cycle of all output signals is independent of the duty cycle of the device master clock, C20i. The CT_C8, C2M and C1M5o clocks have nominal 50% duty cycle,

The output frame pulse (CT_FRAME) is generated in such a way that it is always aligned with the CT_C8 clock to form the required H.110 CT Bus clock and frame pulse shape (when the CT_FRAME is low the rising edge of the CT_C8 defines the frame boundary). Depending on the selected input reference frequency, the CT_FRAME is generated in the following way:

- When the input reference frequency is 8 kHz, the output frame pulse is aligned with the rising edge of the reference.
- When the reference frequency is either 2.048 MHz or 1.544 MHz, the CT_FRAME randomly defines the output frame boundary, always keeping the described relation to the CT_C8 clock.
- When the reference frequency is 8.192 MHz, the output frame pulse (CT_FRAME) has to be aligned with the input frame pulse (FRAME_A_io or FRAME_B_io). Since an 8.192 MHz clock (either C8_A_io or C8_B_io) is used as the reference clock, the selected frame pulse from the Frame Select MUX is provided as the input to the Divider circuit and the CT_FRAME is synchronized to it.

18.9 Frequency Select MUX Circuit

According to the selected input reference of the DPLL, this MUX will select the appropriate output frequency to be the feedback signal to the PLL and MTIE Circuits.

18.10 Modes of Operation

The DPLL can operate in two main modes: the Normal and the Holdover Mode. Each of these modes has two states: the primary or the secondary state. The state depends on which reference is currently selected as the preferred reference the PRI_REF or the SEC_REF. When the DPLL is in the Holdover Mode and the HRST bit of the DOM2 register is pulsed logic high (or held high continuously), the DPLL operates in Freerun Mode.

18.10.1 Normal Mode

Normal Mode is typically used when a clock source synchronized to the network is required.

In the Normal Mode, the DPLL provides timing (C64, CT_C8, C2M and C1M5o) and frame synchronization (CT_FRAME) signals which are synchronized to one of two input references (PRI_REF or SEC_REF). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz, 2.048 MHz or 8.192 MHz.

From a device reset condition or after reference switch, the DPLL can take up to 50 seconds to phase lock the output signals to the selected input reference signal.

18.10.2 Holdover Mode

Holdover Mode is typically used for short durations while network synchronization is temporarily disrupted.

If the FDM1-0 bits are programmed to ‘01’ in the DOM2 register and the PRI_LOS and SEC_LOS pins are high, the DPLL is in the Holdover Mode. The DPLL can also be in the Holdover Mode if the FDM1-0 bits are programmed to ‘00’ and the SLS and PLS bit are observed as ‘11’ in the DPLL House Keeping Register (DHKR).

In the Holdover Mode, the DPLL provides timing and synchronization signals which are based on storage techniques and are not locked to an external reference signal. The storage value is determined while the device is in Normal Mode and locked to an external reference signal. When the DPLL is in the Normal Mode and locks to the input reference signal, a numerical value corresponding to the DPLL output reference frequency is stored alternately in two memory locations every 32 ms. When the device is switched into the Holdover Mode, the value in memory from between 32 ms and 64 ms is used to set the output frequency of the device.

The frequency stability of the Holdover Mode is ±0.07 ppm, which translates to a worst case 49 frame (125 μs) slips in 24 hours.

Two factors affect the frequency stability of the Holdover Mode. The first factor is the drift on the frequency of the master clock (C20i) while in the Holdover Mode. Drift on the master clock directly affects the Holdover Mode stability. Note that the absolute master clock stability does not affect the Holdover Frequency stability, only the change in C20i stability while in Holdover. For example, a ±32 ppm master clock may have a temperature coefficient of ±0.1 ppm/ °C. So a 10 degree change in temperature, while the DPLL is in the Holdover Mode may result in an additional offset (over the ±0.07 ppm) in frequency stability of ±1 ppm, which is much greater than the ±0.07 ppm of the DPLL. The second factor affecting Holdover frequency stability is large jitter on the reference input prior to the mode switch.

18.10.3 Freerun Mode

When the DPLL is in the Holdover Mode and the HRST bit of the DOM2 register is pulsed logic high (or held high continuously), the device is in Freerun Mode.

In Freerun Mode, the DPLL provides timing and synchronization signals which are based on the frequency of the master clock (C20i) only, and are not synchronized to the reference input signals. The frequency of the output signals is an ideal frequency with the freerun accuracy of -0.03 ppm plus the accuracy of the master clock (i.e., CT_C8 has frequency of 8.192 MHz +/- C20i_accuracy - 0.03 ppm).

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

19.0 Measures of Performance

The following are some the DPLL performance indicators and their corresponding definitions.

19.1 Intrinsic Output Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as freerun or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band-limiting filters depending on the applicable standards.

19.2 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly without cycle slips (i.e., remain in lock and regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and the jitter frequency depends on the applicable standards. The input jitter tolerance of the DPLL depends on the selected reference frequency and can not exceed: ± 15 U.I. for E1 or T1 references, and ± 1 U.I. for 8 kHz references.

19.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

In slave and secondary master mode the H.110 standard requires the “B Clocks” to be edge-synchronous with the “A Clocks”, as long as jitter on the “A Clocks” meets Telcordia GR-1244-CORE specifications. Therefore in these two modes no jitter attenuation is performed

In primary master mode the jitter attenuation of the DPLL is determined by the internal 1.52 Hz low pass Loop Filter and the Phase Slope Limiter. Figure 17, "DPLL Jitter Transfer Function Diagram - wide range of frequencies" on page 42 shows the DPLL jitter transfer function diagram in a wide range of frequencies, while Figure 18, "Detailed DPLL Jitter Transfer Function Diagram" on page 43 is the portion of the diagram from Figure 17 around 0 dB of the jitter transfer amplitude. At this point it is possible to see that when operating in primary master mode the DPLL is a second order, type 2 PLL. The jitter transfer function can be described as a low pass filter to 1.52 Hz, -20 dB/decade, with peaking less then 0.5 dB.

All outputs are derived from the same signal, therefore these diagrams apply to all outputs. Since 1U.I. at 1.544 MHz (648 ns_{PP}) is not equal to 1 U.I. at 2.048 MHz (488 ns_{PP}). a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example:

What is the T1 and E1 output jitter when the T1 input jitter is 20 U.I. (T1 U.I. Units) and the T1 to T1 jitter attenuation is 18 dB, for a given jittering frequency?

$$OutputT1 = InputT1 \times 10^{\left(\frac{-A}{20}\right)}$$

$$OutputT1 = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI(T1)$$

$$OutputE1 = OutputT1 \times \frac{(1UIT1)}{(1UIE1)}$$

$$OutputE1 = OutputT1 \times \frac{(644ns)}{(488ns)} = 3.3UI(T1)$$

Using the method mentioned above, the jitter attenuation can be calculated for all combinations of inputs and outputs.

Because intrinsic jitter is always present, the jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

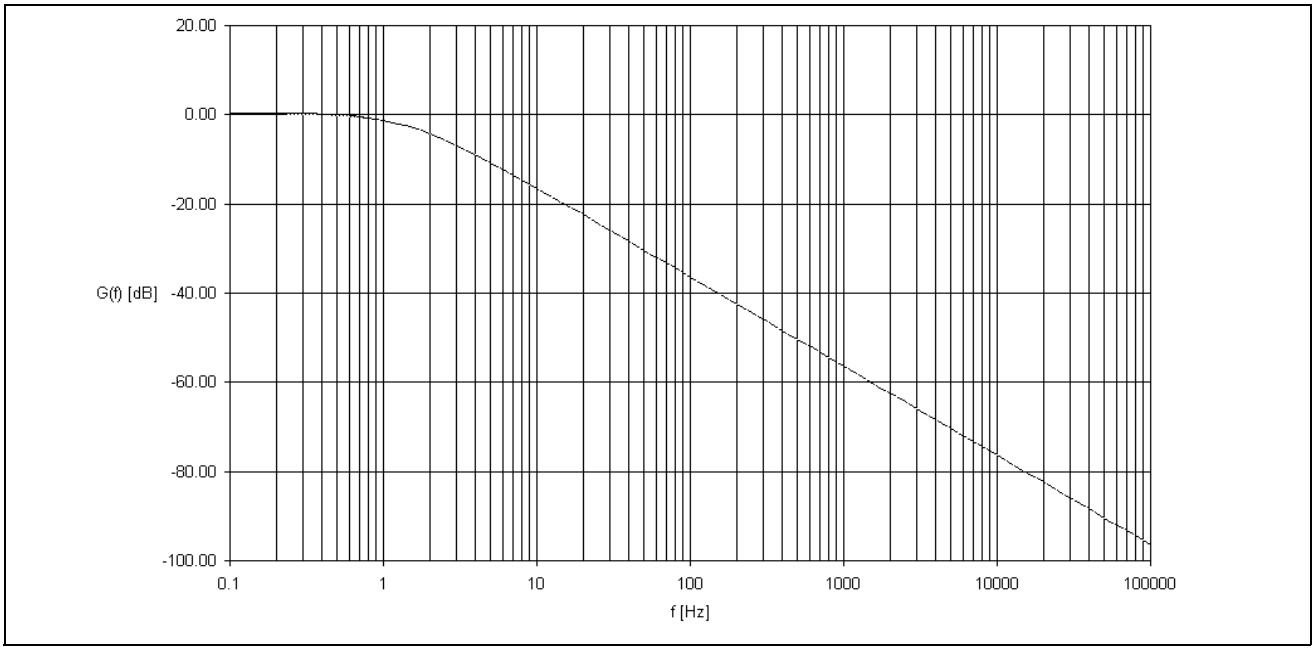


Figure 17 - DPLL Jitter Transfer Function Diagram - wide range of frequencies

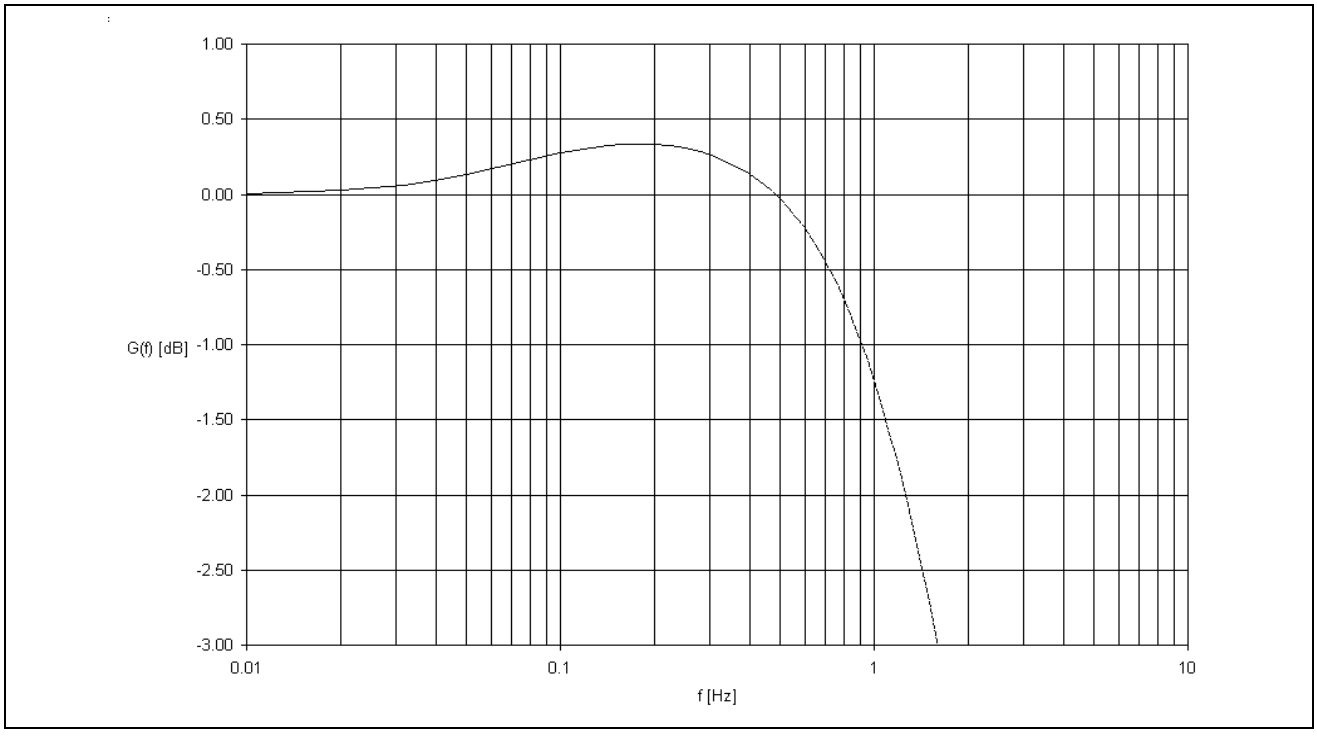


Figure 18 - Detailed DPLL Jitter Transfer Function Diagram

19.4 Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when the DPLL is not locked to an external reference, but is operating in the Freerun Mode. Because the output of the DCO Circuit has only discrete values, the output frequency of the DPLL has the limited accuracy of 0.03 ppm based upon the design implementation. In addition, the master clock (C20i) accuracy also directly affects the freerun accuracy. The freerun accuracy is then, 0.03 ppm plus the master clock accuracy.

19.5 Holdover Frequency Stability

Holdover frequency stability is defined as the maximum fractional frequency offset of an output clock signal when it is operating using a stored frequency value. For the DPLL, the stored value is determined while the device is in Normal Mode and locked to an external reference signal. As a result, when the DPLL is in the Normal Mode, the stability of the master clock (C20i) does not affect the holdover frequency stability because the DPLL will compensate for master clock changes while in Normal Mode. However, when the DPLL is in the Holdover Mode, the stability of the master clock does affect the Holdover frequency stability. The holdover frequency stability is 0.07 ppm assuming that the C20i frequency is held constant.

19.6 Locking Range

The locking range is the input frequency range over which the DPLL must be able to pull into synchronization and to maintain the synchronization. The locking range is defined by the Loop Filter Circuit and is equal to +/- 298 ppm.

Note that the locking range is related to the master clock (C20i). If the master clock is shifted by -100 ppm, the whole locking range also shifts -100 ppm downwards to be: -398 ppm to 198 ppm.

19.7 Phase Slope

The phase slope or the phase alignment speed is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal. Many telecom standards like Telcordia GR-1244-CORE state that the phase slope may not exceed a certain value, usually 81 ns/1.327 ms (61 ppm). This can be achieved by limiting the phase detector output to 61 ppm or less.

In the DPLL when operating in primary master mode the Phase Slope Limiter Circuit achieves the maximum phase slope to be: 56 ppm or 7.0 ns/125 us. When operating in secondary master or slave mode the output edges follow the input edges in accordance with the H.110 standard.

19.8 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

For the DPLL, the maximum time interval error is less than 21 ns per reference switch.

19.9 Phase Lock Time

The Phase Lock Time is the time it takes the PLL to phase lock to the input signal. Phase lock occurs when the input and the output signals are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

i) initial input to output phase difference
ii) initial input to output frequency difference
iii) PLL loop filter
iv) PLL limiter

Although a short phase lock time is desirable, it is not always possible to achieve due to other PLL requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time, but better (smaller) phase slope performance (limiter) results in longer lock times. The DPLL loop filter and limiter were optimized to meet the Telcordia GR-499-CORE jitter transfer and Telcordia GR-1244-CORE phase alignment speed requirements. Consequently, phase lock time, which is not a standards requirement, is less than 50 seconds.

20.0 Initialization of the MT90866

During power up, the $\overline{\text{TRST}}$ pin should be pulled low to ensure that the MT90866 is in the functional mode. An external pull-down resistor is required on this pin so that the MT90866 will not enter the JTAG test mode during power up.

After power up, the contents of the connection memory can be in any state. The ODE pin should be held low after power up to keep all serial outputs in a high impedance state until the microprocessor has initialized the switching matrix. This procedure prevents two serial outputs from driving the same stream simultaneously. To ensure proper operation, a delay of 600 μs must be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the switch. The memory block programming feature can also be used to quickly initialize the backplane and local connection memories.

When this process is completed, the microprocessor controlling the MT90866 can bring the ODE pin high to relinquish the high impedance state control.

21.0 JTAG Support

The MT90866 JTAG interface conforms to the Boundary-Scan IEEE1149.1 standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

21.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the MT90866 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)** - TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Select Input (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Input (TDI)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Output (TDO)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)** - Resets the JTAG scan structure. This pin is internally pulled to Vdd when it is not driven from an external source.

21.2 Instruction Register

The MT90866 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG Interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

21.3 Test Data Register

As specified in IEEE 1149.1, the MT90866 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT90866 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO.

The Device Identification Register - The JTAG device ID for the MT90866 is $0086614B_H$.

Version<31:28>:	0000
Part No. <27:12>:	0000 1000 0110 0110
Manufacturer ID<11:1>:	0001 0100 101
LSB<0>:	1

21.4 BSDL

A BSDL (Boundary Scan Description Language) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149 test interface.

22.0 Register Descriptions

Read/Write Address: 0000_H

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	STS3	STS2	STS1	STS0	PRST	CBEBB	SBERB	CBERL	SBERL	0	MBP	MS2	MS1	MS0

Bit	Name	Description
15-14	Unused	Reserved.
13-12	STS3-2	**ST-BUS Frame Pulse and Clock Output Selection 1:** These two bits are used to select different ST-BUS output frame pulse ($\overline{ST\_FPo1}$) and clock ($\overline{ST\_CKo1}$). **STS3 / STS2 / $\overline{ST\_FPo1}$ Pulse Width / $\overline{ST\_CKo1}$ Freq** **0 / 0 / 244 ns / 4.096 MHz** **0 / 1 / 122 ns / 8.192 MHz** **1 / 0 / 61 ns / 16.384 MHz**
11-10	STS1-0	**ST-BUS Frame Pulse and Clock Output Selection 0:** These two bits are used to select different ST-BUS output frame pulse ($\overline{ST\_FPo0}$) and clock ($\overline{ST\_CKo0}$). **STS1 / STS0 / $\overline{ST\_FPo0}$ Pulse Width / $\overline{ST\_CKo0}$ Freq** **0 / 0 / 244 ns / 4.096 MHz** **0 / 1 / 122 ns / 8.192 MHz** **1 / 0 / 61 ns / 16.384 MHz**
9	PRST	**PRBS Reset:** When high, the PRBS transmitter output will be initialized.
8	CBERB	**Backplane Bit Error Rate Clear:** A low to high transition of this bit will reset the backplane internal bit error counter and the backplane BER register (BBERR).
7	SBERB	**Backplane Start Bit Error Rate Test:** A low to high transition in this bit starts the backplane bit error rate test. The bit error test result is kept in the backplane BER register (BBERR).
6	CBERL	**Local Bit Error Rate Clear:** A low to high transition of this bit will reset the local internal bit error counter and the BER register (LBERR).
5	SBERL	**Local Start Bit Error Rate Test:** A low to high transition in this bit starts the local bit error rate test. The bit error test result is kept in the local BER register (LBERR).
4	Unused	**Reserved.** In functional mode, this bit MUST be low.
3	MBP	**Memory Block Programming:** When this bit is high, the connection memory block programming feature is ready for the programming of bit 13 to bit 15 of the backplane connection memory and local connection memory low. When it is low this feature is disabled.

Table 9 - Control Register (CR) Bits

Bit	Name	Description
2-0	MS2-0	**Memory Select Bits:** These three bits are used to select different connection and data memories.

MS2	MS11	MS0	Memory Selection
0	0	0	Local Connection Memory Low Read/Write
0	0	1	Local Connection Memory High Read/Write
0	1	0	Backplane Connection Memory Read/Write
0	1	1	Local Data Memory Read
1	0	0	Backplane Data Memory Read

Table 9 - Control Register (CR) Bits (continued)

Read/Write Address: 0001_H

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BMS	LG41	LG40	LG32	LG31	LG30	LG22	LG21	LG20	LG12	LG11	LG10	LG02	LG01	LG00

Bit	Name	Description
15	Unused	Reserved.
14	BMS	Backplane Mode Select: This bit refers to the different mode for the backplane interface.

BMS	Switching Mode	Usable Streams
0	8 Mb/s	STio0 - 31
1	16 Mb/s	STio0 - 15

13-12	LG41-LG40	**Local Group 4 Mode Select:** These two bits refer to different switching mode for group 4(STi16-27 and STo16-27) of the local interface. When operating at 4Mb/s or 8Mb/s, the STo19-27 are driven low.

LG41	LG40	Switching Mode	Usable Streams
0	0	8 Mb/s	STi16-18, STo16-18
0	1	4 Mb/s	STi16-18, STo16-18
1	0	2 Mb/s	STi16-27, STo16-27

11-9	LG32-LG30	**Local Group 3 Mode Select:** These three bits refer to different switching mode for group 3 (STi12-15 and STo12-15) of the local interface.

LG32	LG31	LG30	Switching Mode	Usable Streams
0	0	0	8 Mb/s	STi12-15, STo12-15
0	0	1	4 Mb/s	STi12-15, STo12-15
0	1	0	2 Mb/s	STi12-15, STo12-15
0	1	1	4-bit wide subrate	STi12-15, STo12-15
1	0	0	2-bit wide subrate	STi12-15, STo12-15

Table 10 - Device Mode Selection (DMS) Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>8-6</td><td>LG22-LG20</td><td>Local Group 2 Mode Select: These three bits refer to different switching mode for group 2 (STi8-11 and STo8-11) of the local interface.
<table>
<tr><th>LG22</th><th>LG21</th><th>LG20</th><th>Switching Mode</th><th>Usable Streams</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 Mb/s</td><td>STi8-11, STo8-11</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4 Mb/s</td><td>STi8-11, STo8-11</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 Mb/s</td><td>STi8-11, STo8-11</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4-bit wide subrate</td><td>STi8-11, STo8-11</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2-bit wide subrate</td><td>STi8-11, STo8-11</td></tr>
</table></td></tr>
<tr><td>5-3</td><td>LG12-LG10</td><td>Local Group 1 Mode Select: These three bits refer to different switching modes for group 1 (STi4-7 and STo4-7) of the local interface.
<table>
<tr><th>LG12</th><th>LG11</th><th>LG10</th><th>Switching Mode</th><th>Usable Streams</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 Mb/s</td><td>STi4-7, STo4-7</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4 Mb/s</td><td>STi4-7, STo4-7</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 Mb/s</td><td>STi4-7, STo4-7</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4-bit wide subrate</td><td>STi4-7, STo4-7</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2-bit wide subrate</td><td>STi4-7, STo4-7</td></tr>
</table></td></tr>
<tr><td>2-0</td><td>LG02-LG00</td><td>Local Group 0 Mode Select: These three bits refer to different switching modes for group 0 (STi0-3 and STo0-3) of the local interface.
<table>
<tr><th>LG02</th><th>LG01</th><th>LG00</th><th>Switching Mode</th><th>Usable Streams</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 Mb/s</td><td>STi0-3, STo0-3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4 Mb/s</td><td>STi0-3, STo0-3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 Mb/s</td><td>STi0-3, STo0-3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4-bit wide subrate</td><td>STi0-3, STo0-3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2-bit wide subrate</td><td>STi0-3, STo0-3</td></tr>
</table></td></tr>
</table>

Table 10 - Device Mode Selection (DMS) Register Bits (continued)

Read/Write Address: 0002_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	BBPD2	BBPD1	BBPD0	LBPD2	LBPD1	LBPD0	BPE	0	0

Bit	Name	Description
15-9	Unused	**Reserved.** In functional mode, these bits MUST be low.
8-6	BBPD2-0	**Backplane Block Programming Data Bits:** These bits carry the value to be loaded into the backplane connection memory block whenever the Memory Block Programming feature is activated. After the MBP bit in the control register is set to high and the BPE is set to high, the contents of the bits BBPD2 - 0 are loaded into bits 15 - 13 of the backplane connection memory. Bits 12 - 0 of the backplane connection memory are programmed to be zero.
5-3	LBPD2-0	**Local Block Programming Data Bits:** These bits carry the value to be loaded into the local connection memory low whenever the Memory Block Programming feature is activated. After the MBP bit in the control register is set to high and the BPE is set to high, the contents of the bits LBPD2 - 0 are loaded into bits 15 - 13 of the local connection memory low. Bits 12 - 0 of the local connection memory low and bits 15 - 0 of the local connection memory high are programmed to be zero.
2	BPE	**Block Programming Enable:** A low to high transition of this bit enables the Memory Block Programming function. The BPE, BBPD2-0 and LBPD2-0 in the BPM register have to be defined in the same write operation. Once the BPE bit is set to high, MT90866 requires two frames to complete the block programming. After the block programming has finished, the BPE bit returns to low to indicate that the operation is complete. When BPE is high, BPE or MBP can be set to low to abort the programming operation. When BPE is high, the other bits in the BPM register must not be changed for two frames to ensure proper operation. Whenever the microprocessor writes BPE to be high to start the block programming function, the user must maintain the same logical value on the other bits in the BPM register to avoid any change in the setting of the device.
1-0	Unused	**Reserved.** In functional mode, these bits MUST be low.

Table 11 - Block Programming Mode (BPM) Register Bits

Read/Write Addresses: 0004_H for LIDR0 register, 0005_H for LIDR1 register,
0006_H for LIDR2 register, 0007_H for LIDR3 register,
0008_H for LIDR4 register, 0009_H for LIDR5 register,
$000A_H$ for LIDR6 register, $000B_H$ for LIDR7 register,
$000C_H$ for LIDR8 register, $000D_H$ for LIDR9 register,

Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIDR0	0	LID24	LID23	LID22	LID21	LID20	LID14	LID13	LID12	LID11	LID10	LID04	LID03	LID02	LID01	LID00
LIDR1	0	LID54	LID53	LID52	LID51	LID50	LID44	LID43	LID42	LID41	LID40	LID34	LID33	LID32	LID31	LID30
LIDR2	0	LID84	LID83	LID82	LID81	LID80	LID74	LID73	LID72	LID71	LID70	LID64	LID63	LID62	LID61	LID60
LIDR3	0	LID114	LID113	LID112	LID111	LID110	LID104	LID103	LID102	LID101	LID100	LID94	LID93	LID92	LID91	LID90
LIDR4	0	LID144	LID143	LID142	LID141	LID140	LID134	LID133	LID132	LID131	LID130	LID124	LID123	LID122	LID121	LID120
LIDR5	0	LID174	LID173	LID172	LID171	LID170	LID164	LID163	LID162	LID161	LID160	LID154	LID153	LID152	LID151	LID150
LIDR6	0	LID204	LID203	LID202	LID201	LID200	LID194	LID193	LID192	LID191	LID190	LID184	LID183	LID182	LID181	LID180
LIDR7	0	LID234	LID233	LID232	LID231	LID230	LID224	LID223	LID222	LID221	LID220	LID214	LID213	LID212	LID211	LID210
LIDR8	0	LID264	LID263	LID262	LID261	LID260	LID254	LID253	LID252	LID251	LID250	LID244	LID243	LID242	LID241	LID240
LIDR9	0	0	0	0	0	0	0	0	0	0	0	LID274	LID273	LID272	LID271	LID270

Name	Description
LIDn4, LIDn3, LIDn2, LIDn1, LIDn0 (See Note 1)	**Local Input Delay Bits 4 - 0:** These five bits define how long the serial interface receiver takes to recognize and to store bit 0 from the STi input pins: i.e., to start a new frame. The input delay can be selected to +7.75 data rate clock periods from the frame boundary.
Note 1: n denotes an STi stream number from 0 to 27.	

Table 12 - Local Input Bit Delay Registers (LIDR0 to LIDR9) Bits

Local Input Bit Delay	Corresponding Delay Bits				
	LIDn4	LIDn3	LIDn2	LIDn1	LIDn0
No clock period shift (Default)	0	0	0	0	0
+ 1/4 data rate clock period	0	0	0	0	1
+ 1/2 data rate clock period	0	0	0	1	0
+ 3/4 data rate clock period	0	0	0	1	1
+ 1 data rate clock period	0	0	1	0	0
+ 1 1/4 data rate clock period	0	0	1	0	1
+ 1 1/2 data rate clock period	0	0	1	1	0
+ 1 3/4 data rate clock period	0	0	1	1	1
+ 2 data rate clock period	0	1	0	0	0
.....	.....				
+ 7 3/4 data rate clock period	1	1	1	1	1

Table 13 - Local Input Bit Delay Programming

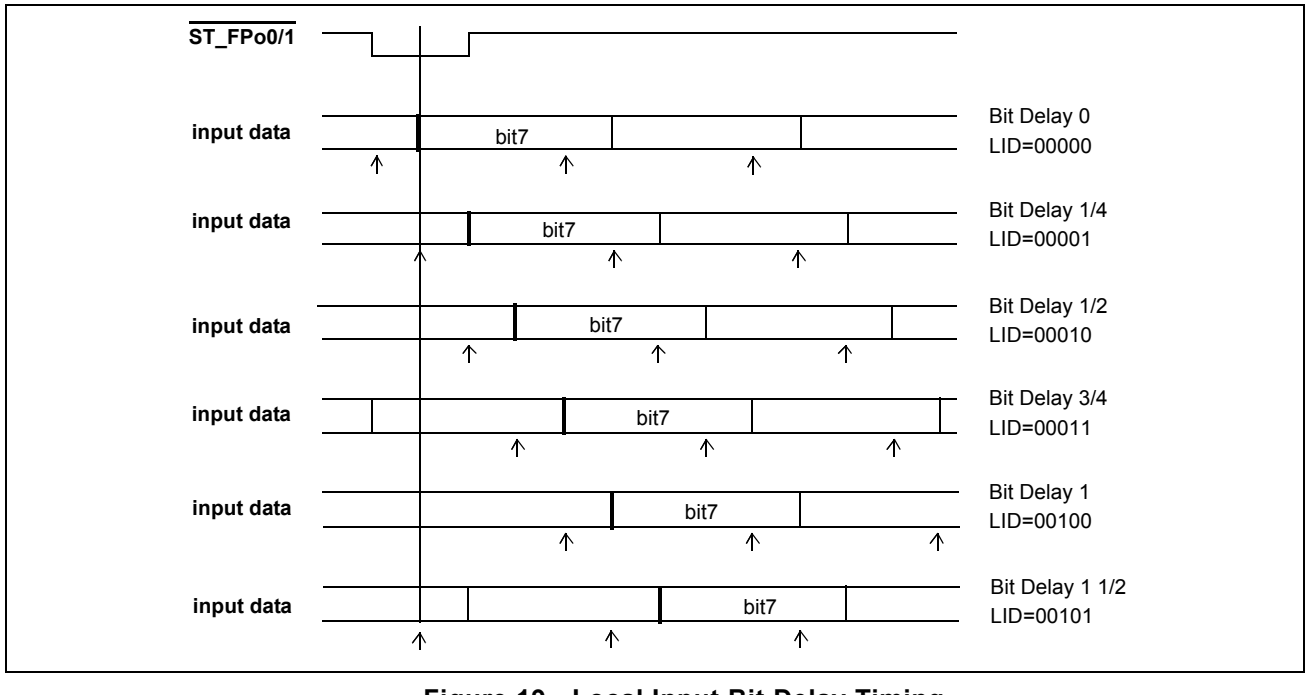


Figure 19 - Local Input Bit Delay Timing

Read/Write Addresses: $001C_H$ for BOAR0 register, $001D_H$ for BOAR1 register, $001E_H$ for BOAR2 register, $001F_H$ for BOAR3 register,

Reset value: 0000_H for all BOAR registers.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOAR0	BOA 71	BOA 70	BOA 61	BOA 60	BOA 51	BOA 50	BOA 41	BOA 40	BOA 31	BOA 30	BOA 21	BOA 20	BOA 11	BOA 10	BOA 01	BOA 00
BOAR1	BOA 151	BOA 150	BOA 141	BOA 140	BOA 131	BOA 130	BOA 121	BOA 120	BOA 111	BOA 110	BOA 101	BOA 100	BOA 91	BOA 90	BOA 81	BOA 80
BOAR2	BOA 231	BOA 230	BOA 221	BOA 220	BOA 211	BOA 210	BOA 201	BOA 200	BOA 191	BOA 190	BOA 181	BOA 180	BOA 171	BOA 170	BOA 161	BOA 160
BOAR3	BOA 311	BOA 310	BOA 301	BOA 300	BOA 291	BOA 290	BOA 281	BOA 280	BOA 271	BOA 270	BOA 271	BOA 260	BOA 251	BOA 250	BOA 241	BOA 240

Name)	Description
BOAn1, BOAn0 (See Note 1)	**Backplane Output Advancement Bits 1 - 0:** These two bits represent the amount of offset that a particular stream output can be advanced. When the offset is zero, the serial output stream has normal alignment with the frame pulse.

BOAn1	BOAn0	Output Advancement	C8_A_io or C8_B_io period	8.192 Mb/s (bit)	16.384 Mb/s (bit)
0	0	0 ns	0	0	0
0	1	7.5 ns	- 1/16	- 1/16	- 1/8
1	0	15 ns	- 1/8	- 1/8	- 1/4
1	1	22.5 ns	- 3/16	- 3/16	- 3/8

Note 1: n denotes a STio stream number from 0 to 31.

Table 14 - Backplane Output Advancement Registers (BOAR0 to BOAR3) Bit

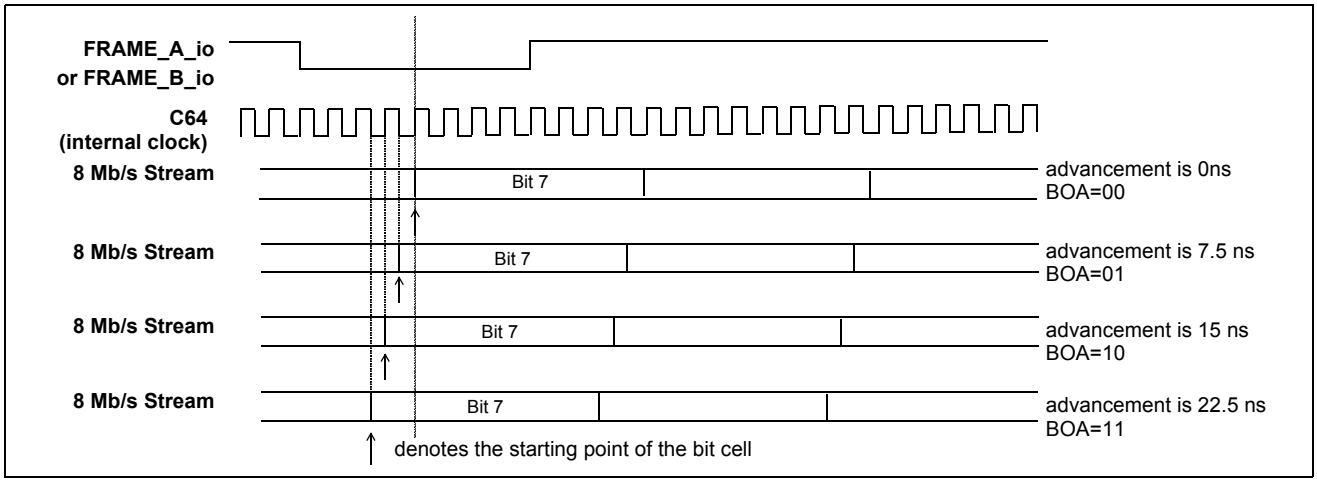


Figure 20 - Example of Backplane Output Advancement Timing

Read/Write Addresses: 0020_H for LOAR0 register, 0021_H for LOAR1 register, 0022_H for LOAR2 register, 0023_H for LOAR3 register,

Reset value: 0000_H for all LOAR registers.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAR0	LOA 71	LOA 70	LOA 61	LOA 60	LOA 51	LOA 50	LOA 41	LOA 40	LOA 31	LOA 30	LOA 21	LOA 20	LOA 11	LOA 10	LOA 01	LOA 00
LOAR1	LOA 151	LOA 150	LOA 141	LOA 140	LOA 131	LOA 130	LOA 121	LOA 120	LOA 111	LOA 110	LOA 101	LOA 100	LOA 91	LOA 90	LOA 81	LOA 80
LOAR2	LOA 231	LOA 230	LOA 221	LOA 220	LOA 211	LOA 210	LOA 201	LOA 200	LOA 191	LOA 190	LOA 181	LOA 180	LOA 171	LOA 170	LOA 161	LOA 160
LOAR3	0	0	0	0	0	0	0	0	LOA 271	LOA 270	LOA 271	LOA 260	LOA 251	LOA 250	LOA 241	LOA 240

Name	Description
LOAn1, LOAn0 (See Note 1)	**Local Output Advancement Bits 1-0:** These two bits represent the amount of offset that a particular stream output can be advanced. When the offset is zero, the serial output stream has normal alignment with the frame pulse.

LOAn1	LOAn0	Output Advancement	C8_A_io or C8_B_io period	2.048 Mb/s (bit)	4.096M b/s (bit)	8.192 Mb/s (bit)
0	0	0 ns	0	0	0	0
0	1	- 7.5 ns	- 1/16	- 1/64	- 1/32	- 1/16
1	0	- 15 ns	- 1/8	- 1/32	- 1/16	- 1/8
1	1	- 22.5 ns	- 3/16	- 3/64	- 3/32	- 3/16

Note 1: n denotes a STi stream number from 0 to 27.

Table 15 - Local Output Advancement Registers (LOAR0 to LOAR3) Bits

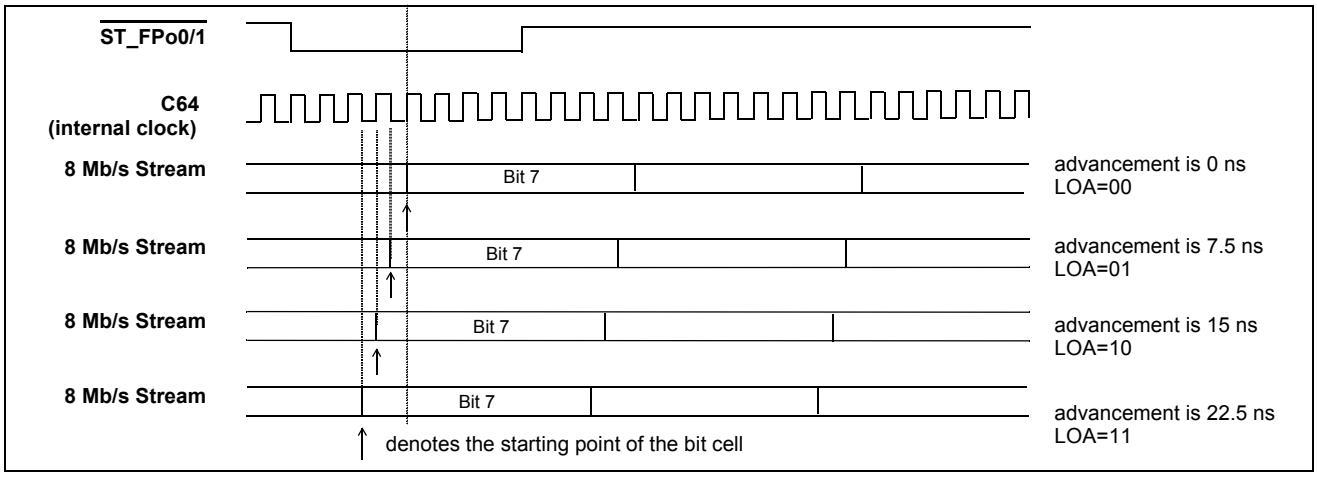


Figure 21 - Local Output Advancement Timing

Read/Write Address: 0027_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	LBS A4	LBS A3	LBS A2	LBS A1	LBS A0	LBC A7	LBC A6	LBC A5	LBC A4	LBC A3	LBC A2	LBC A1	LBC A0

Bit	Name	Description
15 - 13	Unused	**Reserved.**
12 - 8	LBSA4 - LBSA0	**Local BER Input Stream Address Bits:** These bits refer to the local input data stream which receives the BER data.
7 - 0	LBCA7 - LBCA0	**Local BER Input Channel Address Bits**: These bits refer to the local input channel which receives the BER data.

Table 16 - Local Bit Error Rate Input Selection (LBIS) Register Bits

Read Address: 0028_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBER 15	LBER 14	LBER 13	LBER 12	LBER 11	LBER 10	LBER 9	LBER 8	LBER 7	LBER 6	LBER 5	LBER 4	LBER 3	LBER 2	LBER 1	LBER 0

Bit	Name	Description
15 - 0	LBER15 - LBER0	**Local Bit Error Rate Count Bits:** These bits refer to the local bit error counts. This counter stops incrementing when it reaches the value 0xFFFF.

Table 17 - Local Bit Error Rate Register (LBERR) Bits

Read/Write Address: 0029_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	BBSA 4	BBSA 3	BBSA 2	BBSA 1	BBSA 0	BBCA 7	BBCA 6	BBCA 5	BBCA 4	BBCA 3	BBCA 2	BBCA 1	BBCA 0

Bit	Name	Description
15 - 13	Unused	**Reserved**.
12 - 8	BBSA4 - BBSA0	**Backplane BER Input Stream Address Bits**: These bits refer to the backplane input data stream which receives the BER data.
7 - 0	BBCA7 - BBCA0	**Backplane BER Input Channel Address Bits:** These bits refer to the backplane input channel which receives the BER data.

Table 18 - Backplane Bit Error Rate Input Selection (BBIS) Register Bits

Read Address: $002A_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBER 15	BBER 14	BBER 13	BBER 12	BBER 11	BBER 10	BBER 9	BBER 8	BBER 7	BBER 6	BBER 5	BBER 4	BBER 3	BBER 2	BBER 1	BBER 0

Bit	Name	Description
15 - 0	BBER15 -BBER0	**Backplane Bit Error Rate Count Bits:** These bits refer to the backplane bit error count. This counter stops incrementing when it reaches the value 0xFFFF.

Table 19 - Backplane Bit Error Rate Register (BBERR) Bits

Read/Write Address: $002B_H$ for DOM1 Register
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNEN	BEN	AEN	RPS	FS1	FS0	FP1	FP0	SS3	SS2	SS1	SS0	SP3	SP2	SP1	SP0

Bit	Name	Description
15	CNEN	**NREFo Output Enable Bit:** When CNEN is low, NREFo output is disabled, i.e. tri-stated. When CNEN is high, NREFo output is enabled.
14	BEN	**B Clocks Output Enable Bit:** When BEN is low, the “B Clocks” (C8_B_io and FRAME_B_io) are disabled, i.e. tri-stated - C8_B_io and FRAME_B_io behave as inputs. When BEN is high, the “B Clocks” are enabled - C8_B_io and FRAME_B_io behave as outputs.
13	AEN	**A Clocks Output Enable Bit:** When AEN is low, the “A Clocks” (C8_A_io and FRAME_A_io) are disabled, i.e. tri-stated - C8_A_io and FRAME_A_io behave as inputs. When AEN is high, the “A Clocks” are enabled - C8_A_io and FRAME_A_io behave as outputs.
12	RPS	**Reference Selection Bit:** When RPS is low, the preferred reference is the primary reference (PRI_REF). When RPS is high, the preferred reference is the secondary reference (SEC_REF).
11 - 10	FS1 - FS0	**SEC_REF Frequency Selection Bits:** These bits are used to select different clock frequencies for the secondary reference.

FS1	FS0	Secondary Reference
0	0	8 kHz
0	1	1.544 MHz
1	0	2.048 MHz
1	1	8.192 MHz (“A Clocks” or “B Clocks”)

Table 20 - DPLL Operation Mode (DOM1) Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>9 - 8</td><td>FP1 - FP0</td><td>PRI_REF Frequency Selection Bits: These bits are used to select different clock frequencies for the primary reference.
<table>
<tr><th>FS1</th><th>FS0</th><th>Primary Reference</th></tr>
<tr><td>0</td><td>0</td><td>8 kHz</td></tr>
<tr><td>0</td><td>1</td><td>1.544 MHz</td></tr>
<tr><td>1</td><td>0</td><td>2.048 MHz</td></tr>
<tr><td>1</td><td>1</td><td>8.192 MHz (“A Clocks” or “B Clocks”)</td></tr>
</table></td></tr>
<tr><td>7 - 4</td><td>SS3 - SS0</td><td>Secondary Clock Reference Input Selection Bits: These bits are used to select secondary reference input.
<table>
<tr><th>SS3 - SS0</th><th>Secondary Clock Reference Input</th></tr>
<tr><td>0000</td><td>CTREF1</td></tr>
<tr><td>0001</td><td>CTREF2</td></tr>
<tr><td>0010</td><td>“A Clocks”</td></tr>
<tr><td>0011</td><td>“B Clocks”</td></tr>
<tr><td>0100</td><td>Reserved</td></tr>
<tr><td>0101</td><td>Reserved</td></tr>
<tr><td>0110</td><td>Reserved</td></tr>
<tr><td>0111</td><td>Reserved</td></tr>
<tr><td>1000</td><td>LREF0</td></tr>
<tr><td>1001</td><td>LREF1</td></tr>
<tr><td>1010</td><td>LREF2</td></tr>
<tr><td>1011</td><td>LREF3</td></tr>
<tr><td>1100</td><td>LREF4</td></tr>
<tr><td>1101</td><td>LREF5</td></tr>
<tr><td>1110</td><td>LREF6</td></tr>
<tr><td>1111</td><td>LREF7</td></tr>
</table></td></tr>
</table>

Table 20 - DPLL Operation Mode (DOM1) Register Bits (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>3 - 0</td><td>SP3 - SP0</td><td>Primary Clock Reference Input Selection Bits: These bits are used to select primary reference input.
<table>
<tr><th>SP3 - SS0</th><th>Primary Clock Reference Input</th></tr>
<tr><td>0000</td><td>CTREF1</td></tr>
<tr><td>0001</td><td>CTREF2</td></tr>
<tr><td>0010</td><td>“A Clocks”</td></tr>
<tr><td>0011</td><td>“B Clocks”</td></tr>
<tr><td>0100</td><td>Reserved</td></tr>
<tr><td>0101</td><td>Reserved</td></tr>
<tr><td>0110</td><td>Reserved</td></tr>
<tr><td>0111</td><td>Reserved</td></tr>
<tr><td>1000</td><td>LREF0</td></tr>
<tr><td>1001</td><td>LREF1</td></tr>
<tr><td>1010</td><td>LREF2</td></tr>
<tr><td>1011</td><td>LREF3</td></tr>
<tr><td>1100</td><td>LREF4</td></tr>
<tr><td>1101</td><td>LREF5</td></tr>
<tr><td>1110</td><td>LREF6</td></tr>
<tr><td>1111</td><td>LREF7</td></tr>
</table></td></tr>
</table>

Table 20 - DPLL Operation Mode (DOM1) Register Bits (continued)

Read/Write Address: $002C_H$ for DOM2 Register
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	HRST	MRST	FDM1	FDM0	BFEN	AFEN	CNIN	DIV1	DIV0	CNS2	CNS1	CNS0

Bit	Name	Description
15 - 12	Unused	Reserved.
11	HRST	**DPLL Hold Memory Reset Bit:** When HRST is low, the DPLL hold memory circuit is in functional mode. When HRST is high, the hold memory circuit will be reset. While the DPLL is in Holdover Mode, pulsing HRST high (or holding it high continuously) will force the DPLL to the Freerun Mode.
10	MRST	**MTIE Reset Bit:** When MRST is low, the DPLL MTIE circuit is in functional mode. When MRST is high, the MTIE circuit will be reset - the DPLL outputs will align with the nearest edge of the selected reference. When the MT90866 is operating in the slave mode, this bit **MUST** be set high to reset the MTIE circuit.
9 - 8	FDM1 - FDM0	**Failure Detect Mode Bits:** These two bits control how to choose the Failure Detection.

FDM1	FDM0	Failure Detection Mode
0	0	Autodetect - Automatic Failure Detection by internal reference monitor circuit
0	1	External - Failure Detection controlled by external inputs (PRI_LOS and SEC_LOS)
1	0	Forced Primary - The DPLL is forced to use primary reference
1	1	Forced Secondary - The DPLL is forced to use secondary reference

7	BFEN	**B Clocks Fail Output Enable Bit:** When BFEN is low, FAIL_B output is disabled, i.e., tri-stated. When BFEN is high, FAIL_B output is enabled.
6	AFEN	**A Clocks Fail Output Enable Bit:** When AFEN is low, FAIL_A output is disabled, i.e., tri-stated. When AFEN is high, FAIL_A output is enabled.
5	CNIN	**CTREF1 andCTREF2 Inputs Inverted:** When CNIN is high, the CTREF1 and CTREF2 inputs will be inverted, prior to entering the DPLL module. When CNIN is low, the CTREF1 and CTREF2 inputs will not be inverted.

Table 21 - DPLL Operation Mode (DOM2) Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>4 -3</td><td>DIV1 - DIV0</td><td>Divider Bits: These two bits define the relationship between the input reference and the NREFo output.
<table>
<tr><th>DIV1</th><th>DIV0</th><th>NREFo Output</th></tr>
<tr><td>0</td><td>0</td><td>Input reference</td></tr>
<tr><td>0</td><td>1</td><td>Input reference/193 (8 KHz signal when input reference clock = 1.544 MHz)</td></tr>
<tr><td>1</td><td>0</td><td>Input reference/256 (8 KHz signal when input reference clock = 2.048 MHz)</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>2 - 0</td><td>CNS2 - CNS0</td><td>NREFo Source Selection Bits: These three bits select one of the LREF7 - LREF0 to be the NREFo source.
<table>
<tr><th>CNS2</th><th>CNS1</th><th>CNS0</th><th>NREFo Source</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>LREF0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>LREF1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>LREF2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>LREF3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>LREF4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>LREF5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>LREF6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>LREF7</td></tr>
</table></td></tr>
</table>

Table 21 - DPLL Operation Mode (DOM2) Register Bits (continued)

	Bit	Primary Master Mode	Secondary Master Mode	Slave Mode
DOM1 register Bits	BEN (bit 14)	**0** - Monitor “B Clocks”	**1** - Drive “B Clocks”	**0** - Monitor “B Clocks”
	AEN (bit 13)	**1** - Drive “A Clocks”	**0** - Monitor “A Clocks”	**0** - Monitor “A Clocks”
	RPS (bit 12)	**0** - Preferred reference is PRI_REF	**0** - Preferred reference is PRI_REF	**0** - Preferred reference is PRI_REF
	FS1-0 (bits 11-10) Frequency of the secondary reference	**00** - 8 kHz **01** - 1.544 MHz **10** - 2.048 MHz	**00** - 8 kHz **01** - 1.544 MHz **10** - 2.048 MHz	**11** - 8.192 MHz Clock (“B Clocks”)
	FP1-0 (bits 9-8) Frequency of the primary reference	**00** - 8 kHz **01** - 1.544 MHz **10** - 2.048 MHz	**11** - 8.192 MHz Clock (“A Clocks”)	**11** - 8.192 MHz Clock (“A Clocks”)
	SS3-0 (bits 7-4) Secondary reference selection:	**0000** - CTREF1 **0001** - CTREF2 **1000** - LREF0 **1001** - LREF1 **1010** - LREF2 **1011** - LREF3 **1100** - LREF4 **1101** - LREF5 **1110** - LREF6 **1111** - LREF7	**0000** - CTREF1 **0001** - CTREF2 **1000** - LREF0 **1001** - LREF1 **1010** - LREF2 **1011** - LREF3 **1100** - LREF4 **1101** - LREF5 **1110** - LREF6 **1111** - LREF7	**XXXX** - C8_B_io When bits **FS1-0** are set to **11**, C8_B_io is always used as the secondary reference, regardless of the values of bits SS3-0. Output frame pulses are aligned to FRAME_B_io if secondary reference is the active reference
	SP3-0 (bits 3-0) Primary reference selection:	**0000** - CTREF1 **0001** - CTREF2 **1000** - LREF0 **1001** - LREF1 **1010** - LREF2 **1011** - LREF3 **1100** - LREF4 **1101** - LREF5 **1110** - LREF6 **1111** - LREF7	**XXXX** - C8_A_io When bits **FP1-0** are set to **11**, C8_A_io is always used as the primary reference, regardless of the values of bits SP3-0. Output frame pulses are aligned to FRAME_A_io if primary reference is the active reference	**XXXX** - C8_A_io When bits **FP1-0** are set to **11**, C8_A_io is always used as the primary reference, regardless of the values of bits SP3-0. Output frame pulses are aligned to FRAME_A_io if primary reference is the active reference
DOM 2 Register Bits	MRST (bit 10)	**0** - MTIE functional **1** - MTIE reset	**0** - MTIE functional **1** - MTIE reset	**1** - MTIE MUST be kept in the reset state in Slave mode
	FDM1, FDM0 (bits 9-8) Failure detect mode selection	**00** - Autodetect Mode	**00** - Autodetect Mode **01** - External Mode (Note 1)	**00** - Autodetect Mode **01** - External Mode (Note 1)
* Note 1: It is assumed that the switching among references is done by an external software control, if the External Mode is selected.				

Table 22 - MT90866 Mode Selection - By Programming DOM1 and DOM2 Registers

Read/Write Address: $002D_H$ for DPOA Register
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POS 6	POS 5	POS 4	POS 3	POS 2	POS 1	POS 0	0	0	0	0	0	0	SKC2	SKC1	SKC0

Bit	Name	Description
15 - 9	POS6 - POS0	**Phase Offset Bits:** These seven bits refer to the 2's complement phase word to control the DPLL output phase offset. The offset varies in steps of 15 ns if the reference is 8 kHz or 2.048 MHz. The offset varies in steps of 20 ns if the reference is 1.544 MHz.
8 - 3	Unused	**Reserved.**
2 - 0	SKC2 - SKC0	**Skew Control Bits:** These three bits control the delay of the DPLL outputs from 0 to 7 steps in interval of maximum unit delay of 3.5 ns.

Table 23 - DPLL Output Adjustment (DPOA) Register Bits

Read/Write Address: $002E_H$ for DHKR Register

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	SLS	PLS	CKM	Limit	State 2	State 1	State 0

Bit	Name	Description
15 - 7	Unused	**Reserved.**
6	SLS	**Secondary Loss Detection Bit (Read-only bit):** This bit is the same as the output from the DPLL Reference Monitor FAIL_SEC.
5	PLS	**Primary Loss Detection Bit (Read-only bit):** This bit is the same as the output from the DPLL Reference Monitor FAIL_PRI.
4	CKM	**DPLL Clock Monitor Bit:** When high, the primary output C32/64o is 65.536 MHz clock. When low, the primary output C32/64o is 32.768 MHz clock. This is the only writable bit in this register.
3	Limit	**Limit (Read-only bit):** Indicates that DPLL Phase Slope limiter limits input phase.

Table 24 - DPLL House Keeping (DHKR) Register Bits

<table>
<tr>
<td>2 - 0</td>
<td>State</td>
<td>State: These 3 bits indicate the state of the DPLL State Machine. Please refer to Figure 14, "State Machine Diagram" on page 36.
<table>
<tr><th>State 2-0</th><th>State Name</th></tr>
<tr><td>000</td><td>NORMAL_PRI</td></tr>
<tr><td>001</td><td>Reserved</td></tr>
<tr><td>010</td><td>HOLDOVER_PRI</td></tr>
<tr><td>011</td><td>MTIE_PRI</td></tr>
<tr><td>100</td><td>NORMAL_SEC</td></tr>
<tr><td>101</td><td>Reserved</td></tr>
<tr><td>110</td><td>HOLDOVER_SEC</td></tr>
<tr><td>111</td><td>MTIE_SEC</td></tr>
</table>
</td>
</tr>
</table>

Table 24 - DPLL House Keeping (DHKR) Register Bits (continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BTM 2	BTM 1	BTM 0	BSAB 4	BSAB 3	BSAB 2	BSAB 1	BSAB 0	BCA B7	BCA B6	BCA B5	BCA B4	BCA B3	BCA B2	BCA B1	BCA B0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 -13</td><td>BTM2 - 0</td><td>Throughput Delay and Message Control Bits: These three bits control the backplane CT-Bus input or output.

BTM2-0 Throughput delay and Message Mode control
000 Per-channel variable delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The backplane CT-Bus output is from local ST-BUS input.
001 Per-channel constant delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The backplane CT-Bus output is from local ST-BUS input.
010 Per-channel variable delay from backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The backplane CT-Bus output is from backplane CT-Bus input.
011 Per-channel constant delay from backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The backplane CT-Bus output is from backplane CT-Bus input.
100 Per-channel message mode; only the lower byte (bits 7 to 0) of the connection memory location will be the presented to the backplane CT-Bus output channel.
101 Per-channel BER pattern; the pseudo random BER test pattern will be presented to the backplane CT-Bus output channel.
110 Per-channel input. The backplane CT-Bus is input.
111 Reserved.

<table>
<tr><th rowspan="2">BTM2</th><th rowspan="2">BTM1</th><th rowspan="2">BTM0</th><th colspan="2">Input Source</th><th rowspan="2">Var. delay</th><th rowspan="2">Const. delay</th><th rowspan="2">Msg Mode</th><th rowspan="2">BER</th><th rowspan="2">I/O HiZ</th></tr>
<tr><th>Local</th><th>Backplane</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td></td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td></td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td>x</td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td>x</td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td></td><td></td><td></td><td>x</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td></td><td></td><td></td><td></td><td>x</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td></td><td></td><td></td><td></td><td></td><td>x</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="7">Reserved</td></tr>
</table>
</td></tr>
<tr><td>12 - 8</td><td>BSAB4 - BSAB0</td><td>Source Stream Address Bits: These five bits refer to the number of the data streams for the source (local or backplane) connection.</td></tr>
<tr><td>7 - 0 (See Note 1)</td><td>BCAB7 - BCAB0</td><td>Source Channel Address Bits: These eight bits refer to the number of the channel that is the source (local or backplane) connection.</td></tr>
<tr><td colspan="3">Note 1: Only Bits 7-0 will be used for per-channel message mode for the backplane STio streams.</td></tr>
</table>

Table 25 - Backplane Connection Memory Bits

Data Rate	Source Stream	BSAB Bit Usage	BCAB Bit Usage
2 Mb/s	STi0-27	BSAB4-0	BCAB4-0 (32-ch/frame)
4 Mb/s	STi0-18	BSAB4-0	BCAB5-0 (64-ch/frame)
8 Mb/s	STi0-18	BSAB4-0	BCAB6-0 (128-ch/frame)
2-bit subrate	STi0-15	BSAB3-0	BCAB6-0 (128 ch/frame)
4-bit subrate	STi0-15	BSAB3-0	BCAB5 -0 (64 ch/frame)

Table 26 - BSAB and BCAB Bits Usage when Source Streams are from the Local Port

Data Rate	Source Stream	BSAB Bit Usage	BCAB Bit Usage
8 Mb/s	STio0-31	BSAB4-0	BCAB6-0 (128-ch/frame)
16 Mb/s	STio0-15	BSAB3-0	BCAB7-0 (256 ch/frame)

Table 27 - BSAB and BCAB Bits Usage when Source Streams are from the Backplane Port

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	LSRS1	LSRS0

Bit	Name	Description
15 - 2	Unused	**Reserved**.
1 - 0	LSRS1 - LSRS0	**Sub-rate Switching Bits:** For the 4-bit wide sub-rate switching: LSRS1 - 0 / STo Output 01 / Bit 7 - 4 of the 8 bit data 00 / Bit 3 - 0 of the 8 bit data For 2-bit wide sub-rate switching: LSRS1 - 0 / STo Output 11 / Bit 7 - 6 of the 8 bit data 10 / Bit 5 - 4 of the 8 bit data 01 / Bit 3 - 2 of the 8 bit data 00 / Bit 1 - 0 of the 8 bit data

Table 28 - Local Connection Memory High Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTM 2	LTM 1	LTM 0	LSAB 4	LSAB 3	LSAB 2	LSAB 1	LSAB 0	LCAB 7	LCAB 6	LCAB 5	LCAB 4	LCAB 3	LCAB 2	LCAB 1	LCAB 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 -13</td><td>LTM2 - 0</td><td>
Throughput Delay and Message Channel Control Bits: These three bits control the local ST-BUS output.

LTM2-0 — Throughput delay and Message Mode control

000 Per-channel variable delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The local ST-BUS output is from the local ST-BUS input.

001 Per-channel constant delay from local interface; the content of the connection memory is the local data memory address of the switched input channel and stream. The local ST-BUS output is from the local ST-BUS input.

010 Per-channel variable delay from backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The local ST-BUS output is from the backplane CT-Bus input.

011 Per-channel constant delay from the backplane interface; the content of the connection memory is the backplane data memory address of the switched input channel and stream. The local ST-BUS output is from backplane CT-Bus input.

100 Per-channel message mode; only the lower byte (bits 7 to 0) of the connection memory location will be presented to the local ST-BUS output channel.

101 Per-channel BER pattern; the pseudo random BER test pattern will be presented to the local ST-BUS output channel.

110 Per-channel high-impedance. The local ST-BUS output is high-impedance.

111 Reserved

<table>
<tr><th rowspan="2">LTM2</th><th rowspan="2">LTM1</th><th rowspan="2">LTM0</th><th colspan="2">Input Source</th><th rowspan="2">Var. delay</th><th rowspan="2">Const. delay</th><th rowspan="2">Msg Mode</th><th rowspan="2">BER</th><th rowspan="2">Output HiZ</th></tr>
<tr><th>Local</th><th>Backplane</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td></td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td></td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td>x</td><td>x</td><td></td><td></td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td>x</td><td></td><td>x</td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td></td><td></td><td></td><td>x</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td></td><td></td><td></td><td></td><td>x</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td></td><td></td><td></td><td></td><td></td><td>x</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="7">Reserved</td></tr>
</table>
</td></tr>
<tr><td>12 - 8</td><td>LSAB4 - LSAB0</td><td>Source Stream Address Bits: These five bits refer to the number of the data streams for the source (local or backplane) connection.</td></tr>
</table>

Table 29 - Local Connection Memory Low Bits

Bit	Name	Description
7 - 0 (See Note 1)	LCAB7 - LCAB0	**Source Channel Address Bits:** These eight bits refer to the number of the channel that is the source (local or backplane) connection.
Note 1: Only Bits 7-0 will be used for per-channel message mode for the local STo streams.		

Table 29 - Local Connection Memory Low Bits (continued)

Data Rate	Source Stream	LSAB Bit Usage	LCAB Bit Usage
8 Mb/s	STio0-31	LSAB4-0	LCAB6-0 (128-ch/frame)
16 Mb/s	STio0-15	LSAB3-0	LCAB7-0 (256 ch/frame)

Table 30 - LSAB and LCAB Bits Usage when Source Streams are from the Backplane Port

Data Rate	Source Stream	LSAB Bit Usage	LCAB Bit Usage
2 Mb/s	STi0-27	LSAB4-0	LCAB4-0 (32-ch/frame)
4 Mb/s	STi0-18	LSAB4-0	LCAB5-0 (64-ch/frame)
8 Mb/s	STi0-18	LSAB4-0	LCAB6-0 (128-ch/frame)
2-bit subrate	STi0-15	LSAB3-0	LCAB6-0 (128 ch/frame)
4-bit subrate	STi0-15	LSAB3-0	LCAB5 -0 (64 ch/frame)
Note: When operating at 4 Mb/s or 8 Mb/s, STo19-27 are driven low.			

Table 31 - LSAB and LCAB Bits Usage when Source Stream are from the Local Port

23.0 DC/AC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}	-0.5	5.0	V
2	BSTio Bias Voltage	V_{DD5V}	-0.5	7.0	V
3	Input Voltage	V_I	-0.5	V_{DD} + 0.5	V
4	Output Voltage	V_o	-0.5	V_{DD} + 0.5	V
5	Package power dissipation	P_D		2	W
6	Storage temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD}	3.0	3.3	3.6	V
3	BSTio Bias Voltage (3 V PCI Spec)	V_{DD5V}	3.0	3.3	3.6	V
3	BSTio Bias Voltage (5 V PCI Spec)	V_{DD5V}	4.5	5.0	5.5	V
4	Input Voltage	V_I	0		V_{DD}	V
5	Input Voltage on 5 V Tolerant Inputs	V_{I_5V}	0		V_{DD5V}	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current	I_{DD}			480	mA	Output unloaded
2	Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
3	Input Low Voltage	V_{IL}			$0.3V_{DD}$	V	
4	Input Leakage (input pins)	I_L			15	µA	$0 < V < V_{DD\_IO}$ See Note 1
5	Weak Pullup Current	I_{PU}		33	50	µA	Input at 0V
6	Weak Pulldown Current	I_{PD}		33	50	µA	Input at V_{DD}
7	Input Pin Capacitance	C_I		5	10	pF	
8	Output High Voltage	V_{OH}	$0.8V_{DD}$			V	I_{OH} = 10 mA
9	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
10	High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD\_IO}$
11	Output Pin Capacitance	C_O			15	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (Vin).

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V	

AC Electrical Characteristics† - Input Frame Pulse and Input Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FRAME_A_io, FRAME_B_io Input Frame Pulse Width	t_{CFPIW}	90	122	180	ns	
2	FRAME_A_io, FRAME_B_io Input Frame Pulse Setup Time	t_{CFPIS}	45		90	ns	
3	FRAME_A_io, FRAME_B_io Input Frame Pulse Hold Time	t_{CFPIH}	45		90	ns	
4	C8_A_io, C8_B_io Input Clock Period	t_{C8MIP}	122-ϕ		122+ϕ	ns	
5	C8_A_io, C8_B_io Input Clock High Time	t_{C8MIH}	58-ϕ		64+ϕ	ns	
6	C8_A_io, C8_B_io Input Clock Low Time	t_{C8MIL}	58-ϕ		64+ϕ	ns	
7	Phase Correction	ϕ	0		10	ns	
8	C8_A_io, C8_B_io Input Rise/Fall Time	t_{rC8i}, t_{fC8i}	0		5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

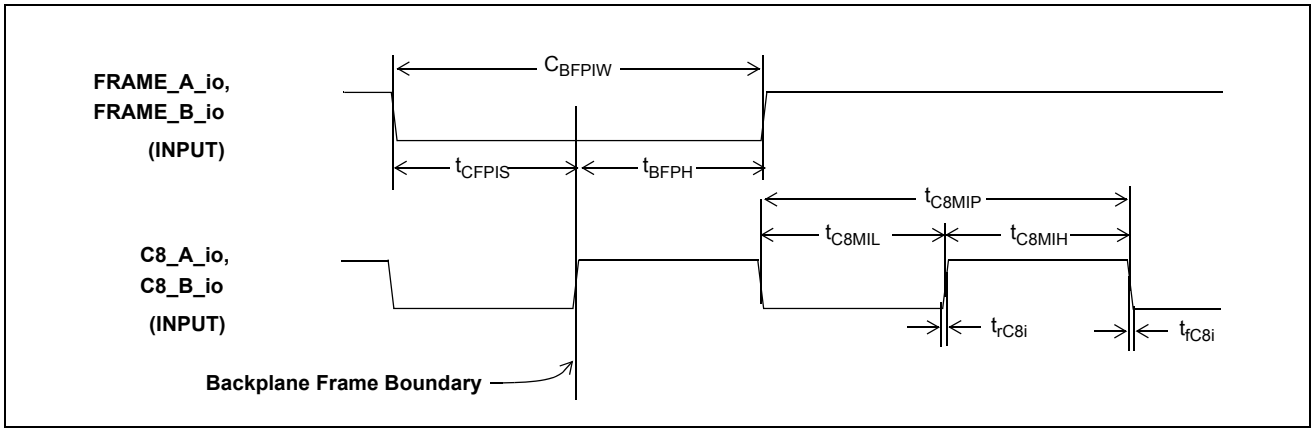


Figure 22 - Backplane Frame Pulse Input and Clock Input Timing Diagram

AC Electrical Characteristics† - Output Frame Pulse and Output Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Internal Timing Variation	Δ^*	6.50		7.50	ns	
2	Backplane Frame Boundary Offset	t_{FBOS}	1.25-Δ		2.5+Δ	ns	
3	FRAME_A_io, FRAME_B_io Output Pulse Width	t_{CFPOW}	122-Δ	122	122+Δ	ns	C_L=30pF
4	Delay from FRAME_A_io, FRAME_B_io output falling edge to C8_a_io,C8_B_io output rising edge	t_{CFODF}	61-Δ/2		61+Δ/2	ns	
5	Delay from C8_A_io,C8_B_io output rising edge to FRAME_A_io,FRAME_B_io output rising edge	t_{CFODR}	61-Δ/2		61+Δ/2	ns	
6	C8_A_io, C8_B_io Output Clock Period	t_{C8MP}	122-Δ	122	122+Δ	ns	C_L=30pF
7	C8_A_io, C8_B_io Output High Time	t_{C8MH}	61-Δ/2		61+Δ/2	ns	
8	C8_A_io, C8_B_io Output Low Time	t_{C8ML}	61-Δ/2		61+Δ/2	ns	
9	C8_A_io, C8_B_io Output Rise Time	t_{rC8o}			13	ns	
10	C8_A_io, C8_B_io Output Fall Time	t_{fC8o}			14		
11	C32/64o (32.768 MHz) Output Delay Time	t_{C32MOD}			Δ	ns	C_L=30pF
12	C32/64o (32.768 MHz) Period	t_{C32MP}	30.5-Δ	30.5	30.5+Δ	ns	
13	C32/64o (32.768 MHz) High Time	t_{C32MH}	15.25-Δ/2		15.25+Δ/2	ns	
14	C32/64o (32.768 MHz) Low Time	t_{C32ML}	15.25-Δ/2		15.25+Δ/2	ns	
15	C32/64o (65.536 MHz) Period	t_{C64MP}	15.25-Δ/2	15.25	15.25+Δ/2	ns	
16	C32/64o (65.536 MHz) High Time	t_{C64MH}	Δ		0.5+Δ	ns	
17	C32/64o (65.536 MHz) Low Time	t_{C64ML}	Δ		5.5+Δ	ns	
18	C32/64o Clock Rise Time (32.768 MHz or 65.536 MHz)	t_{r32o}			5	ns	
19	C32/64o Clock Fall Time (32.768 MHz or 65.536 MHz)	t_{f32o}			6	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* The AC electrical characteristics are listed as a function of the internal timing variation (Δ) to highlight the value of each parameter independent of the variation. It is important to choose the maximum or minimum Δ value correctly for worst case timing calculation. When adding parameters for timing calculation, it is sufficient to include this Δ only once in the calculation.

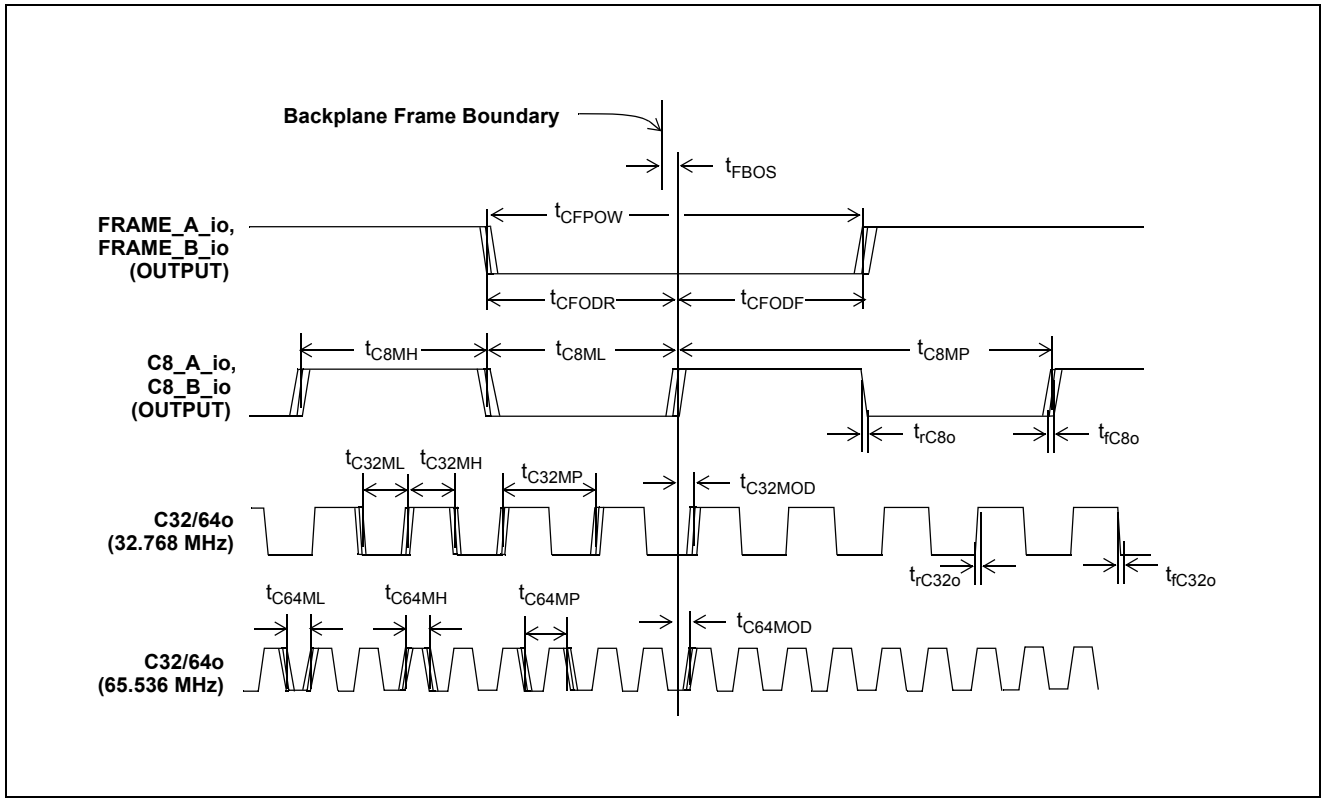


Figure 23 - Backplane Frame Pulse Output and Clock Output Timing Diagram (in Primary Master Mode and Secondary Master Mode)

AC Electrical Characteristics† - C20i Master Input Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C20i Input Clock Period	t_{C20MP}	49.995	50	50.005	ns	
2	C20i Input Clock Tolerance		-100		100	ppm	
3	C20i Input Clock High Time	t_{C20MH}	20		30	ns	
4	C20i Input Clock Low Time	t_{C20ML}	20		30	ns	
5	C20i Input Rise/Fall Time	t_{rC20M}, t_{fC20M}			10	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

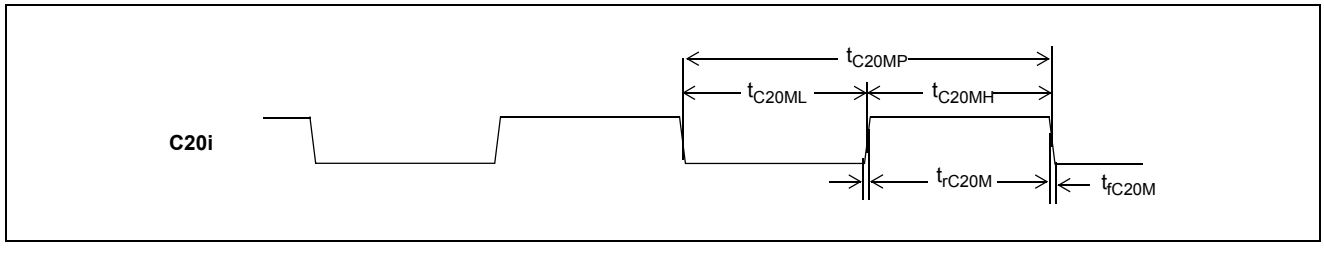


Figure 24 - Backplane Frame Pulse Input and Clock Input Timing Diagram

AC Electrical Characteristics† - Reference Input Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	CTREF1, CTREF2, LREF0-7 Period	t_{R8KP}	121	125	129	µs	8 kHz Mode
2	CTREF1, CTREF2, LREF0-7 High Time	t_{R8kh}	0.09		128.91	µs	
3	CTREF1, CTREF2, LREF0-7 Low Time	t_{R8kL}	0.09		128.91	µs	
4	CTREF1, CTREF2, LREF0-7 Rise/Fall Time	t_{rR8K}, t_{fR8K}	0		20	ns	
5	CTREF1, CTREF2, LREF0-7 Period	t_{R2MP}	366	488	610	ns	2.048 MHz Mode
6	CTREF1, CTREF2, LREF0-7 High Time	t_{R2Mh}	90	244	520	ns	
7	CTREF1, CTREF2, LREF0-7 Low Time	t_{R2ML}	90	244	520	ns	
8	CTREF1, CTREF2, LREF0-7 Rise/Fall Time	t_{rR2M}, t_{fR2M}	0		20	ns	
9	CTREF1, CTREF2, LREF0-7 Period	t_{R1M5P}	486	648	810	ns	1.544 MHz Mode
10	CTREF1, CTREF2, LREF0-7 High Time	t_{R1M5h}	90	324	720	ns	
11	CTREF1, CTREF2, LREF0-7 Low Time	t_{R1M5L}	90	324	720	ns	
12	CTREF1, CTREF2, LREF0-7 Rise/Fall Time	t_{rR1M5}, t_{fR1M5}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

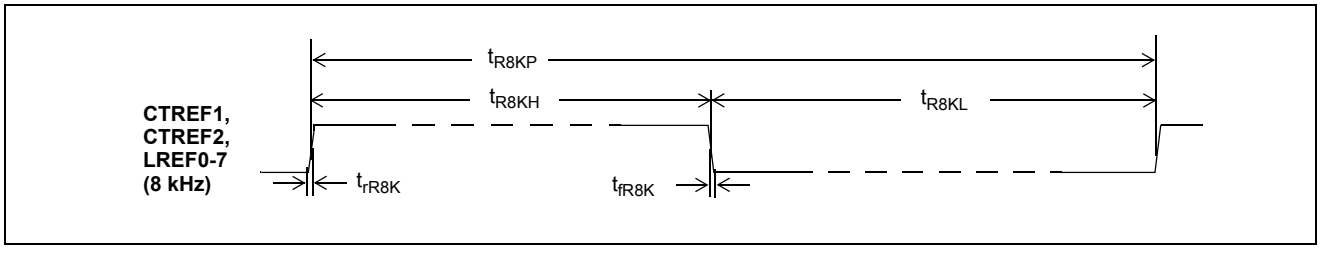


Figure 25 - Reference Input Timing Diagram when the input frequency = 8 kHz

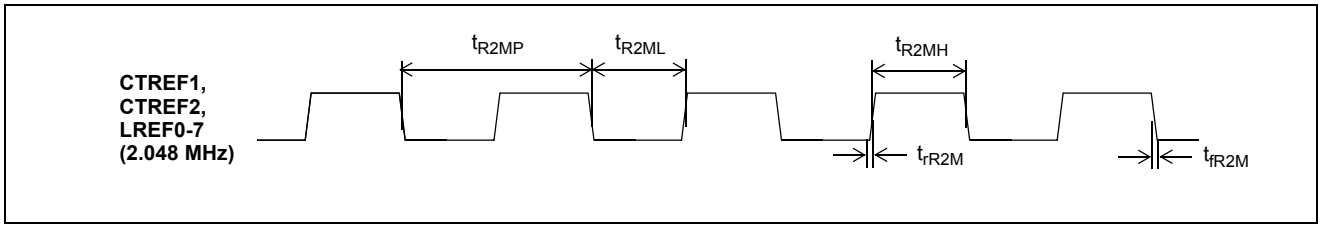


Figure 26 - Reference Input Timing Diagram when the input frequency = 2.048 MHz

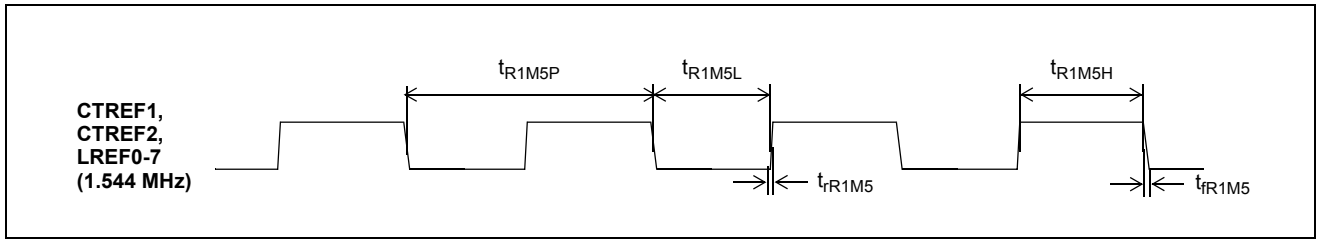


Figure 27 - Reference Input Timing Diagram when the input frequency = 1.544 Hz

AC Electrical Characteristics† - Reference Output Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	NREFo Output Delay Time	t_{ROD}			20	ns	(DIV1,DIV0) = (0,0) in the DOM2 Register
2	NREFo Clock Period	t_{RP}	Same as LREF0-7 Period				
3	NREFo Clock High Time	t_{RH}	Same as LREF0-7 High Time				
4	NREFo Clock Low Time	t_{RL}	Same as LREF0-7 Low Time				
5	NREFo Clock Rise/Fall Time	t_{rREF}, t_{fREF}	0		12 14	ns	
6	NREFo Clock Period	t_{R8KOP}	124.9	125	125.1	µs	(DIV1,DIV0) = (0,1) or (DIV1,DIV0) = (1,0) in the DOM2 Register
7	NREFo Clock High Time	t_{R8KO2H}	124.4	124.5	124.6	µs	
8	NREFo Clock Low Time	t_{R8KO2L}	488-Δ	488	488+Δ	ns	
9	NREFo Clock High Time	$t_{R8KO15H}$	124.3	124.4	124.5	µs	
10	NREFo Clock Low Time	$t_{R8KO15L}$	648-Δ	648	648+Δ	ns	

‡ Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

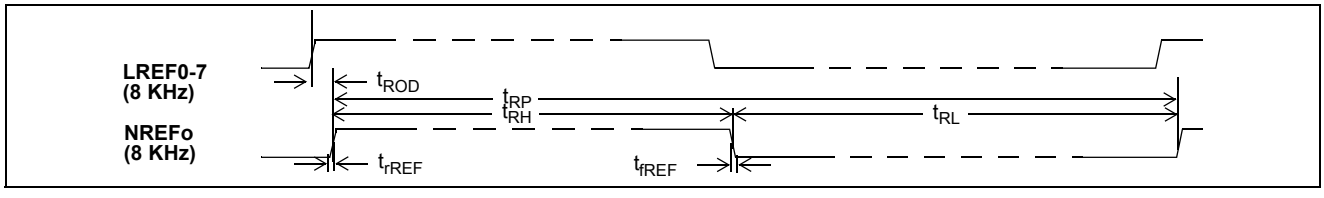


Figure 28 - Reference Output Timing Diagram when (DIV1, DIV0) = (0, 0) in DOM2 Register

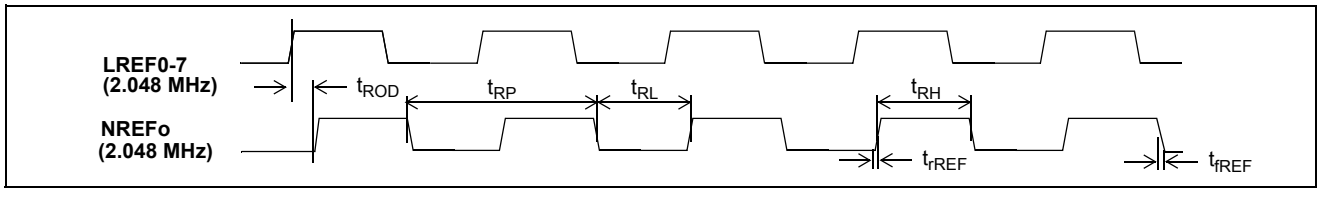


Figure 29 - Reference Output Timing Diagram when (DIV1, DIV0) = (0, 0) in DOM2 Register

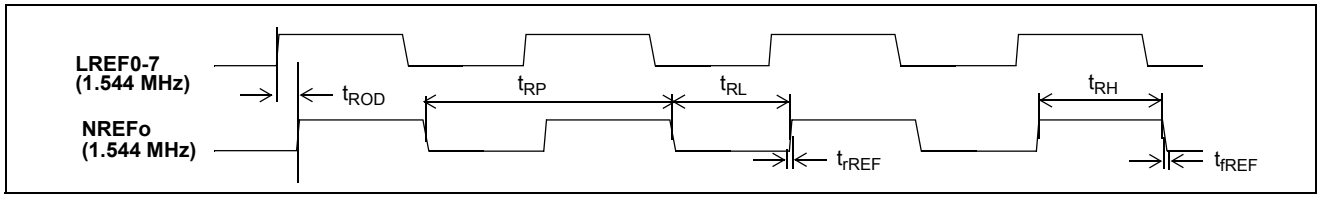


Figure 30 - Reference Input Timing Diagram when (DIV1, DIV0) = (0, 0) in DOM2 Register

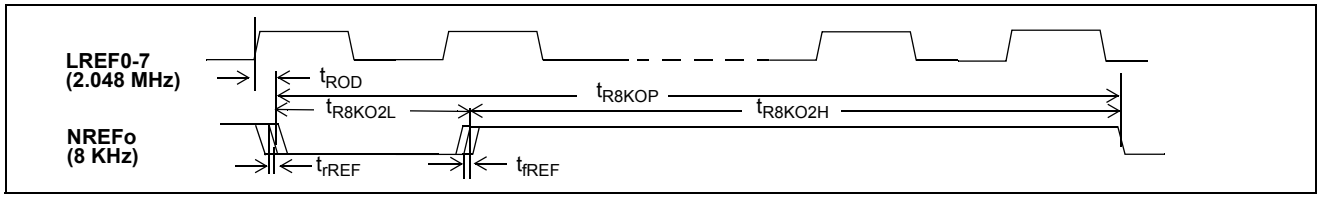


Figure 31 - Reference Output Timing Diagram when (DIV1, DIV0) = (1, 0) in DOM2 Register

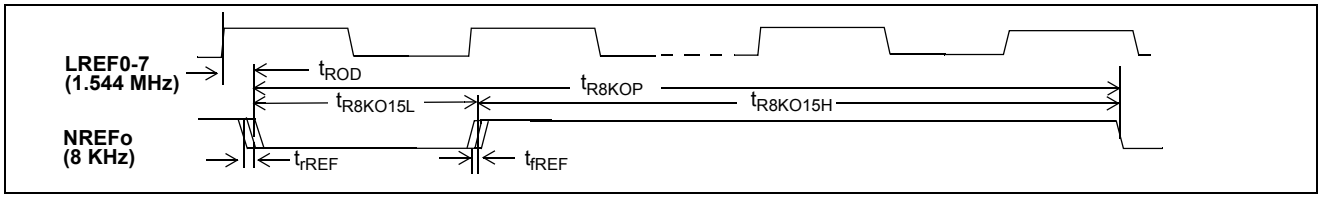


Figure 32 - Reference Output Timing Diagram when (DIV1, DIV0) = (0, 1) in DOM2 Register

AC Electrical Characteristics† - Local Frame Pulse and Clock Timing, $\overline{\text{ST\_CKo}}$ = 4.096 MHz

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Local Frame Boundary Offset[1]	t_{LFBOS}	Δ		17.5+Δ	ns	C_L=30pF
2	$\overline{\text{ST\_FPo0/1}}$ Width	t_{FPW4}	244-Δ	244	244+Δ	ns	
3	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of $\overline{\text{ST\_FPo0/1}}$ to falling edge of $\overline{\text{ST\_CKo0/1}}$	t_{FODF4}	122-Δ/2		122+Δ/2	ns	
4	$\overline{\text{ST\_FPo}}$ 0/1Output Delay from Falling edge of $\overline{\text{ST\_CKo0/1}}$ to rising edge of $\overline{\text{ST\_FPo0/1}}$	t_{FODR4}	122-Δ/2		122+Δ/2	ns	
5	$\overline{\text{ST\_CKo0/1}}$ Clock Period	t_{CP4}	244-Δ	244	244+Δ	ns	
6	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width High	t_{CH4}	122-Δ/2		122+Δ/2	ns	
7	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width Low	t_{CL4}	122-Δ/2		122+Δ/2	ns	
8	$\overline{\text{ST\_CKo0/1}}$ Clock Rise/Fall Time	t_{rC4o}, t_{C4o}			14	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: No jitter presented on input reference clock.

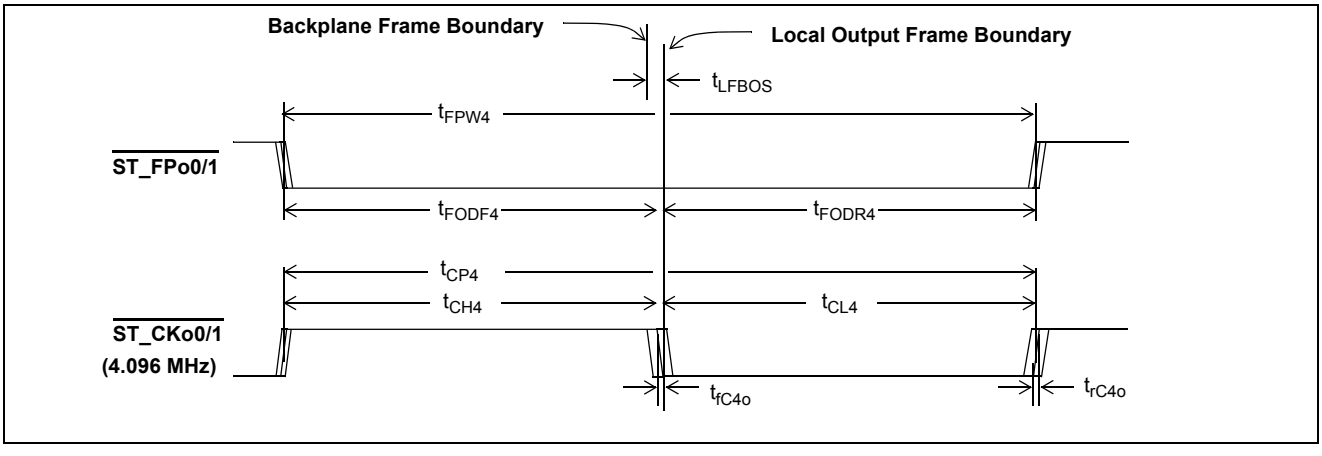


Figure 33 - Local Clock Timing Diagram when ST_CKo0/1 frequency = 4.096 MHz

AC Electrical Characteristics† - Local Frame Pulse and Clock Timing, $\overline{\text{ST\_CKo0}}$ = 8.192 MHz

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Local Frame Boundary Offset[1]	t_{LFBOS}	Δ		17.5+Δ	ns	C_L=30 pF
2	$\overline{\text{ST\_FPo0/1}}$ Width	t_{FPW8}	122-Δ	122	122+Δ	ns	
3	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of $\overline{\text{ST\_FPo0/1}}$ to falling edge of $\overline{\text{ST\_CKo0/1}}$	t_{FODF8}	61-Δ/2		61+Δ/2	ns	
4	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of $\overline{\text{ST\_CKo0-1}}$ to rising edge of $\overline{\text{ST\_FPo0/1}}$	t_{FODR8}	61-Δ/2		61+Δ/2	ns	
5	$\overline{\text{ST\_CKo0/1}}$ Clock Period	t_{CP8}	122-Δ	122	122+Δ	ns	
6	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width High	t_{Ch8}	61-Δ/2		61+Δ/2	ns	
7	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width Low	t_{CL8}	61-Δ/2		61+Δ/2	ns	
8	$\overline{\text{ST\_CKo0/1}}$ Clock Rise/Fall Time	t_{rC8o}, t_{fC8o}			14	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: No jitter presented on input reference clock.

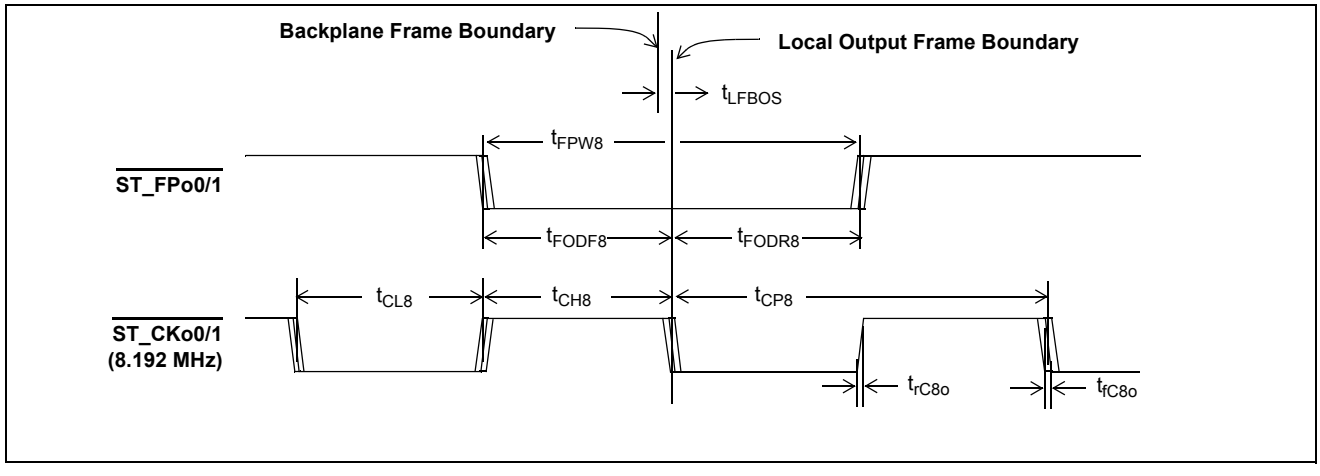


Figure 34 - Local Clock Timing Diagram when ST_CKo0/1 frequency = 8.192 MHz

AC Electrical Characteristics† - Local Frame Pulse and Clock Timing, $\overline{\text{ST\_CKo}}$ = 16.384 MHz

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Local Frame Boundary Offset[1]	t_{LFBOS}	Δ		17+Δ	ns	
2	$\overline{\text{ST\_FPo0/1}}$ Width	t_{FPw16}	61-Δ	61	61+Δ	ns	
3	$\overline{\text{ST\_FPo0/1}}$ Output Delay from Falling edge of $\overline{\text{ST\_FPo0/1}}$ to falling edge of $\overline{\text{ST\_CKo0/1}}$	t_{FODF16}	30.5-Δ/2		30.5+Δ/2	ns	
4	$\overline{\text{ST\_FPo}}$ Output Delay from Falling edge of $\overline{\text{ST\_CKo0/1}}$ to rising edge of $\overline{\text{ST\_FPo0/1}}$	t_{FODR16}	30.5-Δ/2		30.5+Δ/2	ns	
5	$\overline{\text{ST\_CKo0/1}}$ Clock Period	t_{CP16}	61-Δ	61	61+Δ	ns	C_L=30pF
6	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width High	t_{Ch16}	30.5-Δ/2		30.5+Δ/2	ns	
7	$\overline{\text{ST\_CKo0/1}}$ Clock Pulse Width Low	t_{CL16}	30.5-Δ/2		30.5+Δ/2	ns	
8	$\overline{\text{ST\_CKo0/1}}$ Clock Rise/Fall Time	t_{rC16o}, t_{fC16o}			14	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1: No jitter presented on input reference clock.

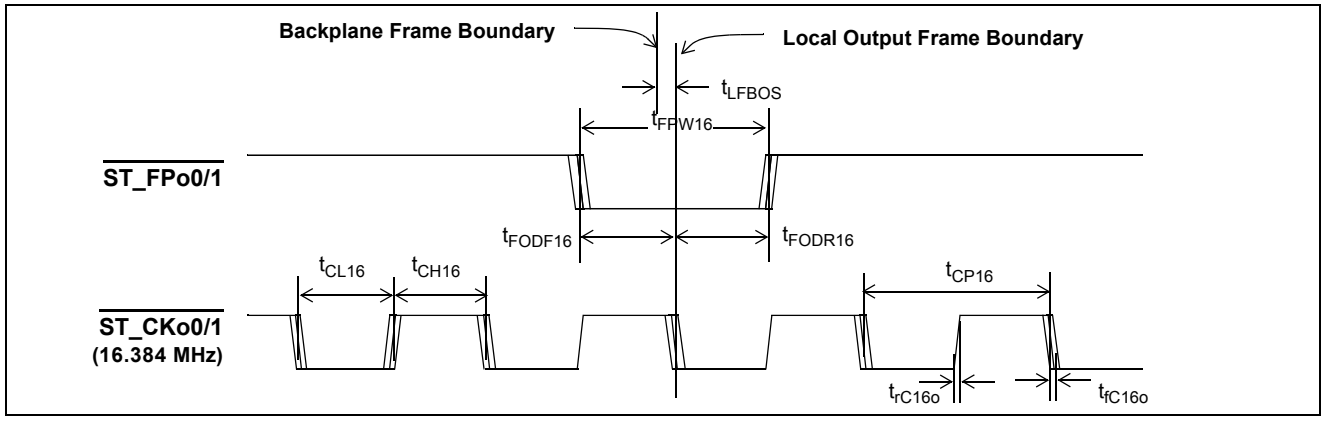


Figure 35 - Local Clock Timing Diagram when ST_CKo frequency = 16.384 MHz

AC Electrical Characteristics† - C1M5o Output Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C1M5o Period	t_{C1M5oP}	648-Δ	648	648+Δ	ns	C_L=30 pF
2	C1M5o High Time	t_{C1M5oH}	324-Δ/2	324	324+Δ/2	ns	
3	C1M5o Low Time	t_{C1M5oL}	324-Δ/2	324	324+Δ/2	ns	
4	C1M5o Rise Time	t_{rC1M5o}			10	ns	
5	C1M5o Fall Time	t_{fC1M5o}			11	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

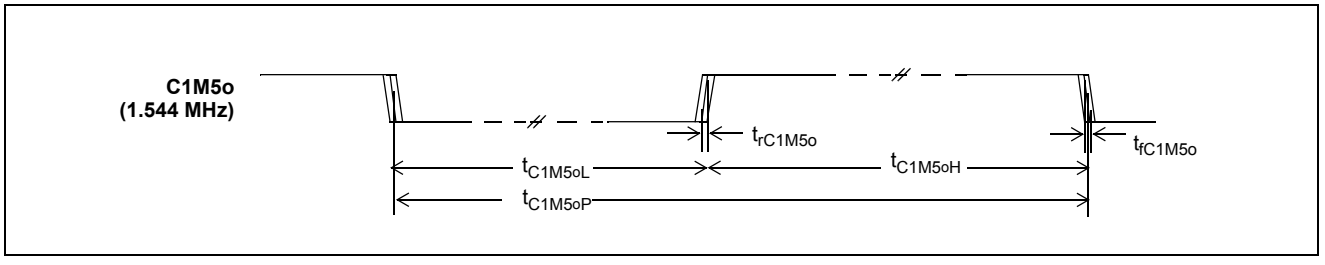


Figure 36 - C1M5o Output Clock Timing Diagram

AC Electrical Characteristics† - Output Clock Jitter Generation (Unfiltered)

	Characteristic	Typ.‡	Max.	Units	Notes
1	Jitter at C1M5o (1.544 MHz)	7.4	8.0	ns-pp	Device locks to1.544 MHZ reference input, and no jitter present on the reference
2	Jitter at $\overline{ST\_CKo0}$-1 (4.096 MHz)	7.1	8.8	ns-pp	
3	Jitter at $\overline{ST\_CKo0}$-1 (8.192 MHz)	7.0	8.3	ns-pp	
4	Jitter at $\overline{ST\_CKo0}$-1 (16.384 MHz)	7.6	9.9	ns-pp	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 8 Mb/s

	Characteristic	Sym.	Min.‡	Typ.‡	Max.	Units	Test Conditions
1	STio0-31 Input Data Sample Point	t_{SAMP8}	91.5	91.5	91.5	ns	
2	STio0-31 Input Setup Time	t_{CIS8}	5+Δ			ns	
3	STio0-31 Input Hold Time	t_{CIH8}	5+Δ			ns	
4	STio0-31 Output Delay Active to Active	t_{DOD8}	1-Δ		5+Δ	ns	C_L = 30 pF, Note 1
5	Per Channel boundary HiZ	t_{DOZ8} t_{ZDO8}		10 10		ns ns	R_L=1K, C_L=30 pF, Note 2

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* Note 1: To meet the H.110 output timing requirement, the output delay time can be reduced further by programming the backplane output advancement registers (BOA0 - 3).

* Note 2: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

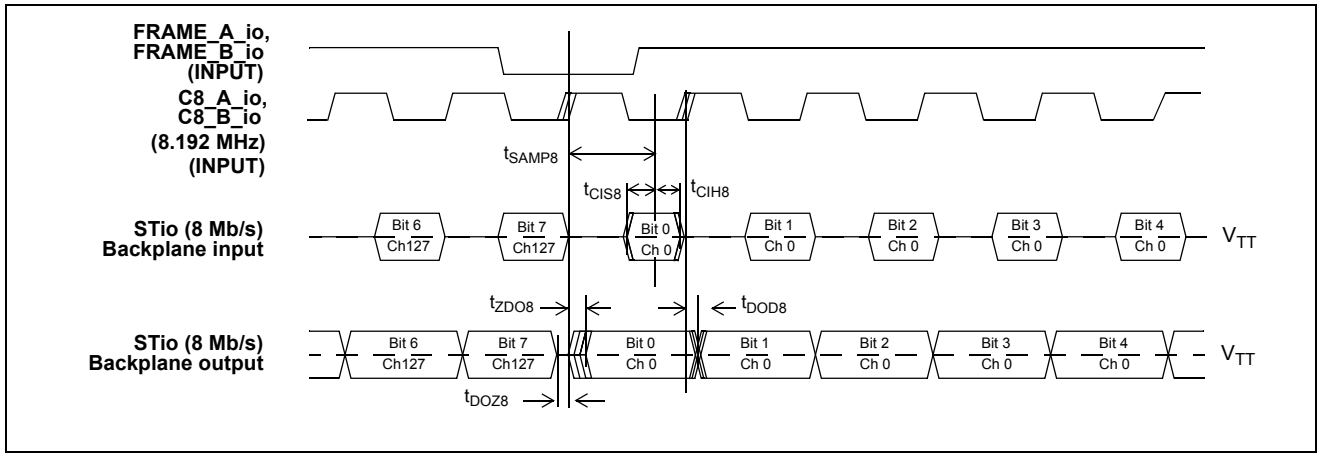


Figure 37 - Backplane Serial Stream Timing when the Data Rate is 8 Mb/s

AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 16 Mb/s

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STio0-15 Input Data Sample Point	t_{SAMP16}	46	46	46	ns	
2	STio0-15 Input Setup Time	t_{CIS16}	5+Δ			ns	
3	STio0-15 Input Hold Time	t_{CIH16}	5+Δ			ns	
4	STio0-15 Output Delay Active to Active	t_{DOD16}	1-Δ		5+Δ	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

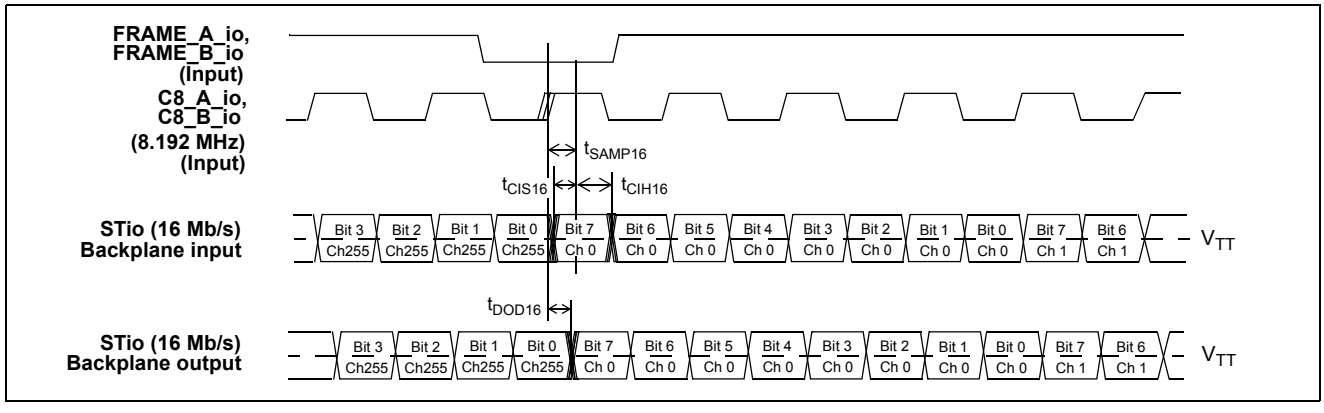


Figure 38 - Backplane Serial Stream Timing when the Data Rate is 16 Mb/s

AC Electrical Characteristics† - Local Serial Stream Output Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STo Delay - Active to Active						
	@2.048 Mb/s	t_{SOD2}	-10-Δ*		1.5-Δ*	ns	C_L = 30 pF
	@4.096 Mb/s	t_{SOD4}	-10-Δ*		1.5-Δ*	ns	C_L = 30 pF
	@8.192 Mb/s	t_{SOD8}	-10-Δ*		1.5-Δ*	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* See Section 7.0, “Local Output Timing Considerations” on page 21

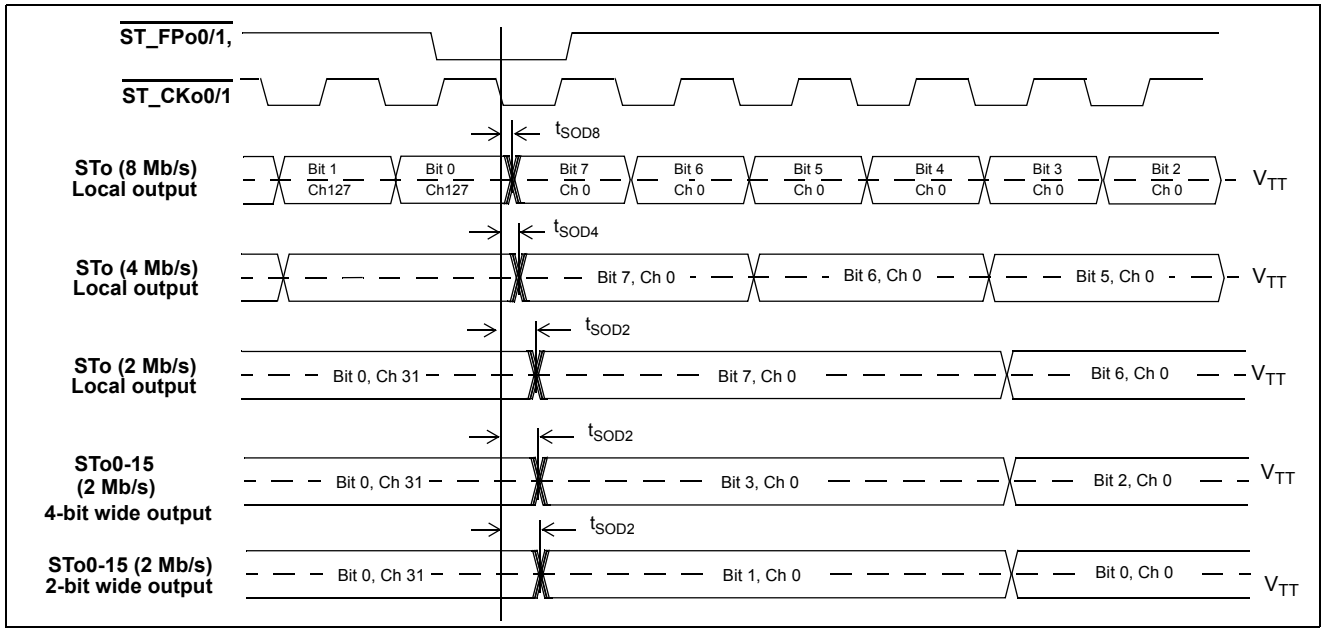


Figure 39 - Local Serial Stream Output Timing

AC Electrical Characteristics† - Local Serial Stream Input Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STi Input Data Sample Point						
	@2.048 Mb/s	t_{SAMP2L}	366	366	366	ns	
	@4.096 Mb/s	t_{SAMP4L}	183	183	183	ns	
	@8.192 Mb/s	t_{SAMP8L}	91.5	91.5	91.5	ns	
2	STi Setup Time						
	@2.048 Mb/s	t_{SIS2}	5+Δ			ns	
	@4.096 Mb/s	t_{SIS4}	5+Δ			ns	
	@8.192 Mb/s	t_{SIS8}	5+Δ			ns	
3	STi Hold Time						
	@2.048 Mb/s	t_{SIH2}	5+Δ			ns	
	@4.096 Mb/s	t_{SIH4}	5+Δ			ns	
	@8.192 Mb/s	t_{SHI8}	5+Δ			ns	

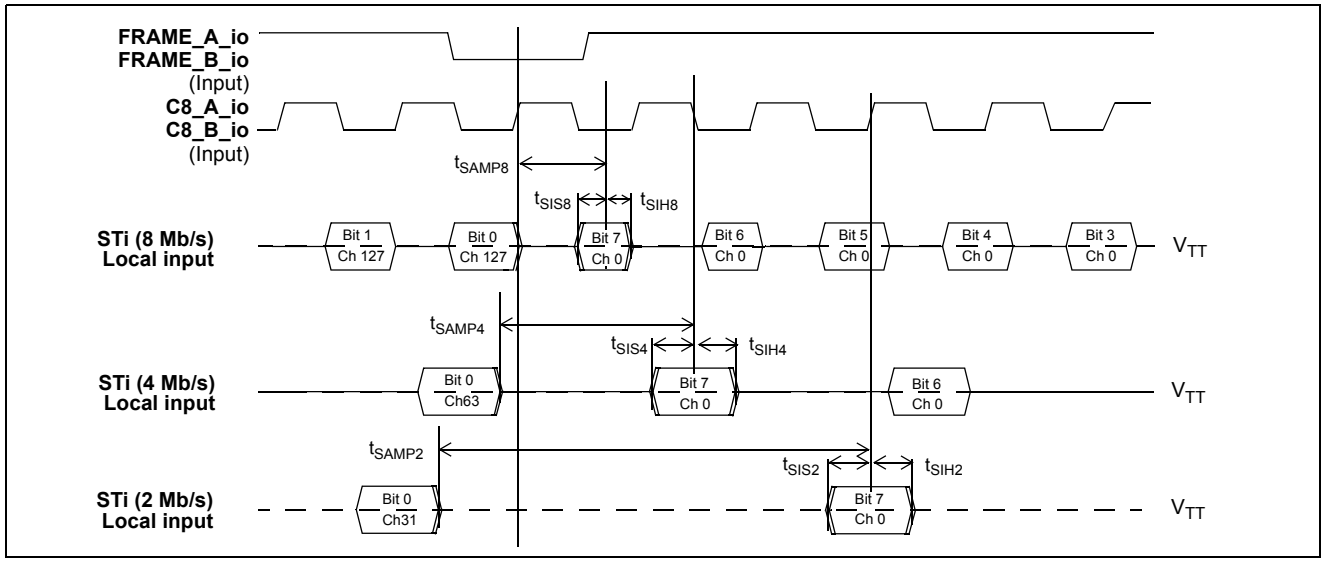


Figure 40 - Local Serial Stream Input Timing

AC Electrical Characteristics† - Local and Backplane Tristate Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STo/STio Delay - Active to High-Z - High-Z to Active 2.048 Mb/s (local) 4.096 Mb/s (local) 8.192 Mb/s (local) 8.192 Mb/s (backplane) 16.384 Mb/s (backplane)	t_{DZ}, t_{ZD}	 -12-Δ -12-Δ -12-Δ -1-Δ -1-Δ		 3.5-Δ 3.5-Δ 3.5-Δ 7+Δ 7+Δ	 ns ns ns ns ns	R_L=1K, C_L=30pF, See Note 1.
2	Output Driver Enable (ODE) Delay - High-Z to Active 2.048 Mb/s (local) 4.096 Mb/s (local) 8.192 Mb/s (local) 8.192 Mb/s (backplane) 16.384 Mb/s (backplane)	t_{ZD_ODE}			 37 37 37 20 20	 ns ns ns ns ns	
2	Output Driver Disable (ODE) Delay - Active to High-Z 2.048 Mb/s (local) 4.096 Mb/s (local) 8.192 Mb/s (local) 8.192 Mb/s (backplane) 16.384 Mb/s (backplane)	t_{DZ_ODE}			 20 20 20 20 20	 ns ns ns ns ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

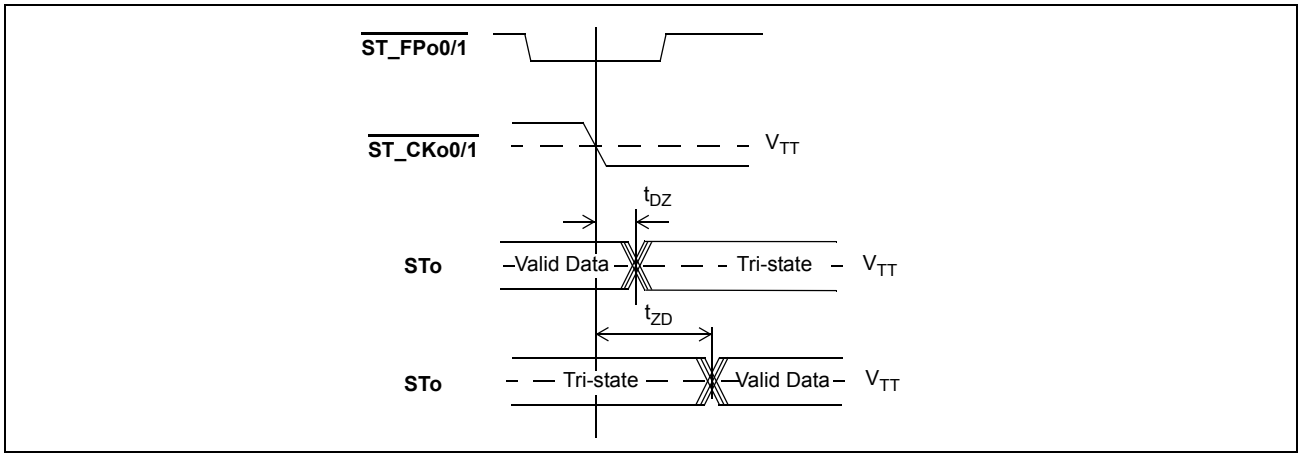


Figure 41 - Local Serial Output and External Control

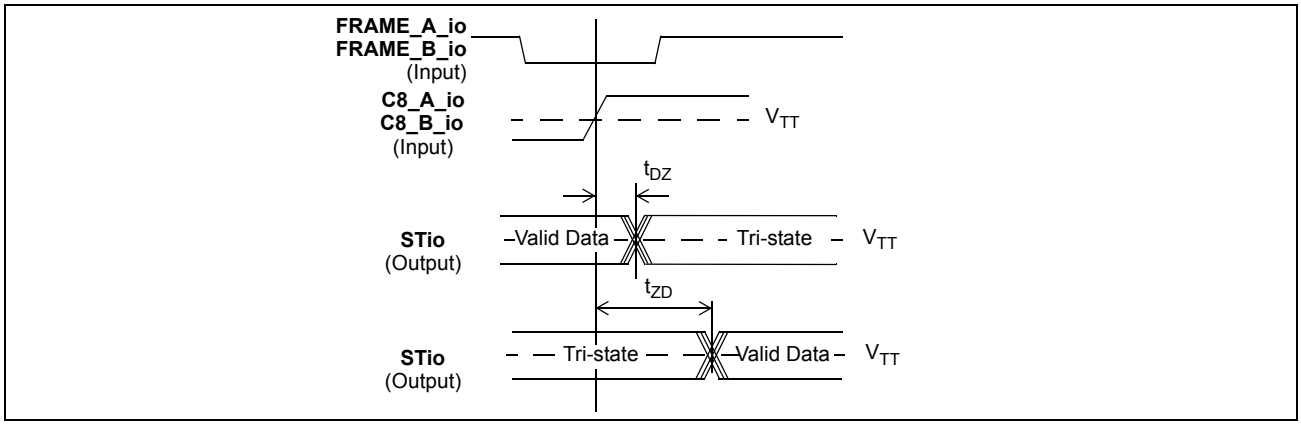


Figure 42 - Backplane Serial Output and External Control

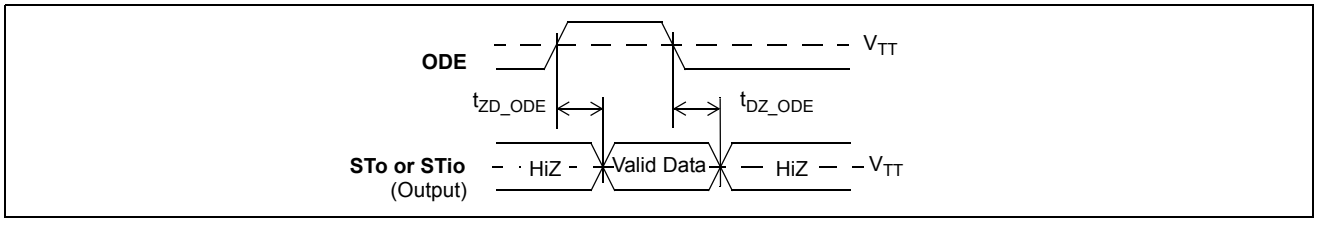


Figure 43 - Output Driver Enable (ODE)

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[1]
1	$\overline{CS}$ setup from $\overline{DS}$ falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from $\overline{DS}$ falling	t_{RWS}	15			ns	
3	Address setup from $\overline{DS}$ falling	t_{ADS}	5			ns	
4	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
6	Address hold after $\overline{DS}$ rising	t_{ADH}	5			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	20			ns	C_L=30pF
8	Data hold on read	t_{DHR}			20	ns	C_L=30pF, R_L=1K See Note 2
9	Valid Write Data Setup	t_{WDS}			20	ns	
10	Data hold on write	t_{DHW}	8			ns	
11	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory	t_{AKD}		 97/82 158/114	 110/95 171/127	 ns ns	 C_L=30pF C_L=30pF
12	Acknowledgment Hold Time	t_{AKH}			30	ns	C_L=30pF, R_L=1K, See Note 2

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*Note 1: A delay of 100 microseconds must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.
*Note 2: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

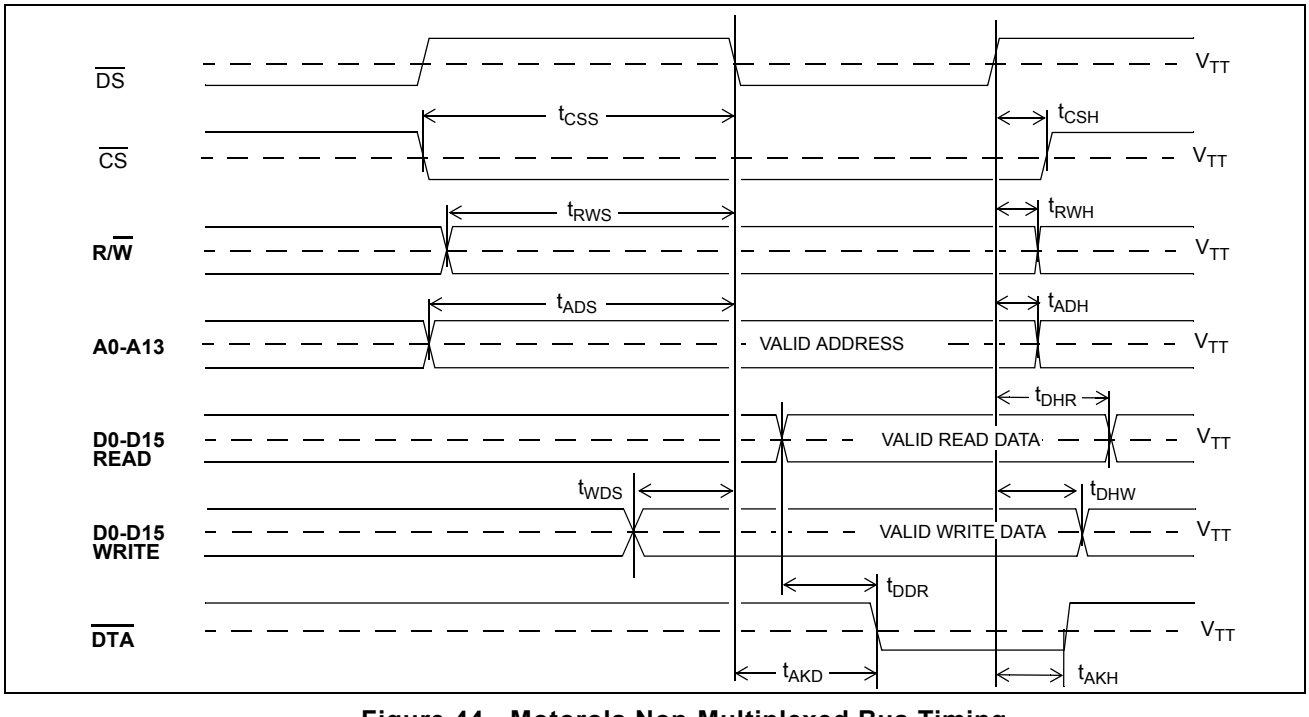


Figure 44 - Motorola Non-Multiplexed Bus Timing

AC Electrical Characteristics† - JTAG Test Port and $\overline{\text{Reset}}$ Pin Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	200			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	80			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	80			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	20			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L=30pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	20			ns	C_L=30pF
10	$\overline{\text{Reset}}$ pulse width	t_{RSTW}	400			ns	C_L=30pF

† Characteristics are over recommended operating conditions unless otherwise stated.

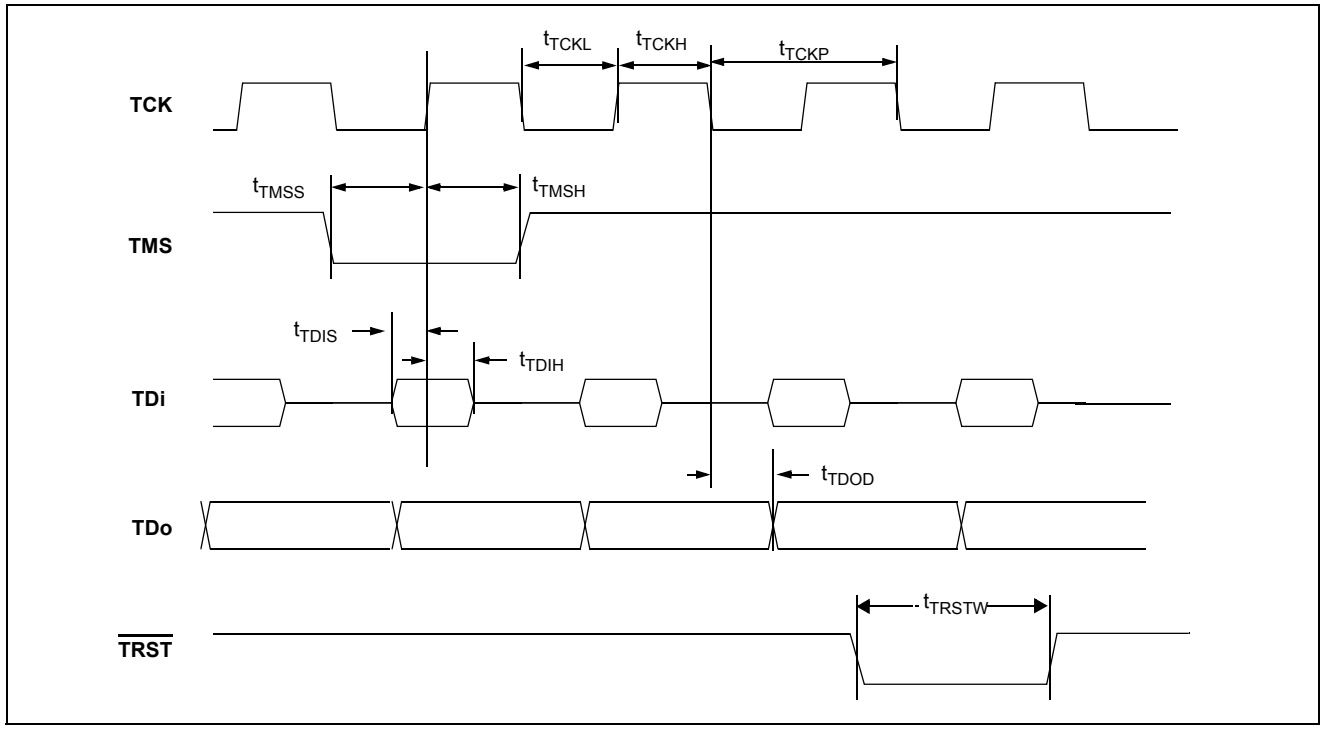


Figure 45 - JTAG Test Port Timing Diagram

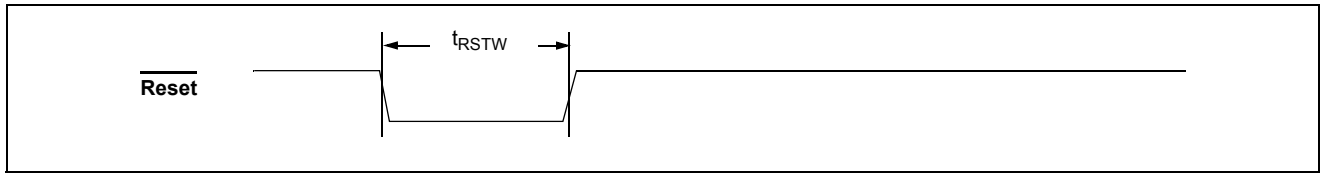
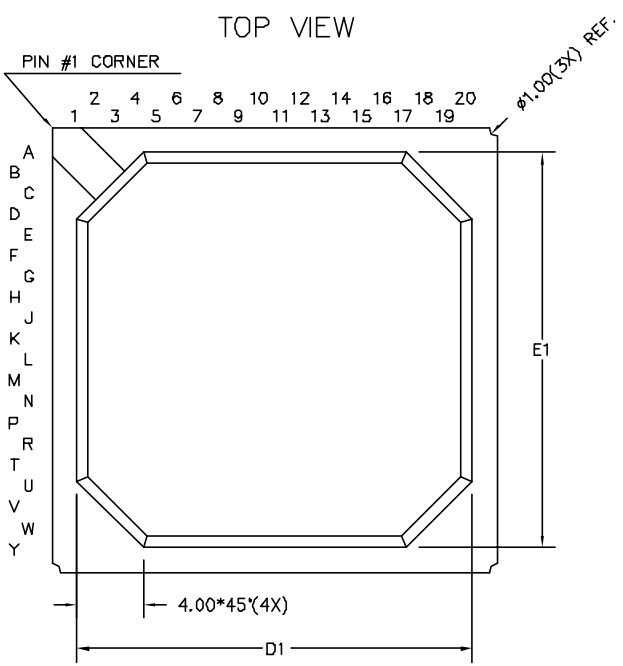
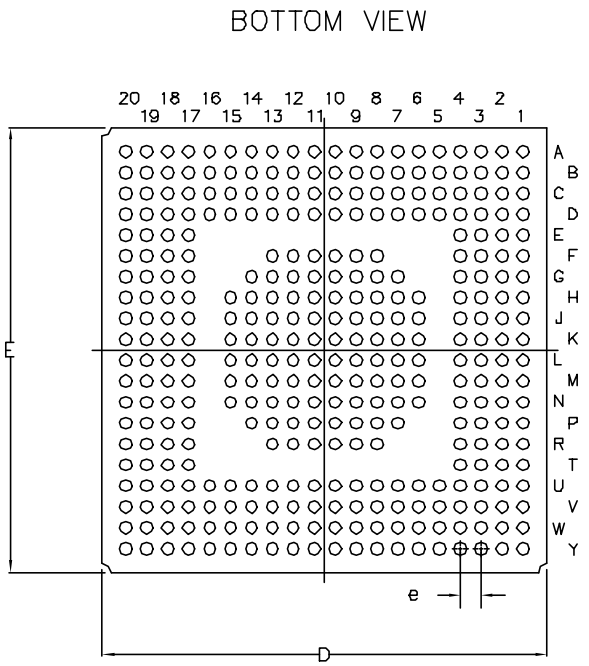


Figure 46 - Reset Pin Timing Diagram

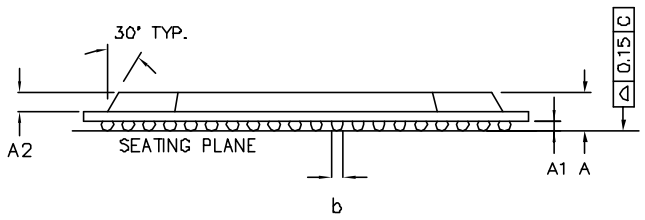
24.0 Trademarks

CompactPCI® is a registered trademark of PICMG-PCI Industrial Computer Manufacturers Group, Inc.





DIMENSION	MIN	MAX
A	2.13	2.53
A1	0.50	0.70
A2	1.17 REF	
D	26.80	27.20
D1	24.00 REF	
E	26.80	27.20
E1	24.00 REF	
b	0.60	0.90
e	1.27	
N	344	
Conforms to JEDEC MS – 034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.56 MM.

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