

# NX5L2750C

Analog switch with negative swing audio capability

Rev. 1 — 6 September 2013

Product data sheet

## 1. General description

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The NX5L2750C is a dual low-ohmic single-pole double-throw analog switch suitable for use as an analog or digital 2 : 1 multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ).

The NX5L2750C is capable of switching audio signals with negative swing without the need of a coupling capacitor.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current  $I_{CC}$ . This makes it possible for the NX5L2750C to switch 5 V audio signals with a 1.8 V digital controller, eliminating the need for logic level translation.

## 2. Features and benefits

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- Supply voltage range from 1.8 V to 5.0 V
- 0.8  $\Omega$  typical ON resistance
- 100 MHz typical bandwidth or data frequency
- CMOS low-power consumption
- 1.8 V control logic at  $V_{CC} = 3.6$  V
- Break-before-make switching
- ESD protection:
  - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
  - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from  $-40$  °C to  $+85$  °C

## 3. Applications

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- Cellular phones, PDA
- Portable media players
- Personal media players



4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NX5L2750CGU	−40 °C to +85 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 × 1.80 × 0.50 mm	SOT1160-1

5. Marking

Table 2. Marking

Type number	Marking code
NX5L2750CGU	LA

6. Functional diagram

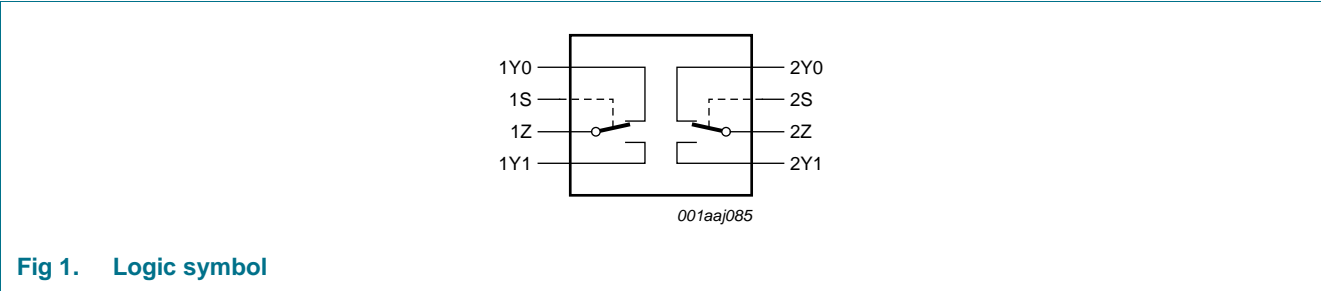


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning

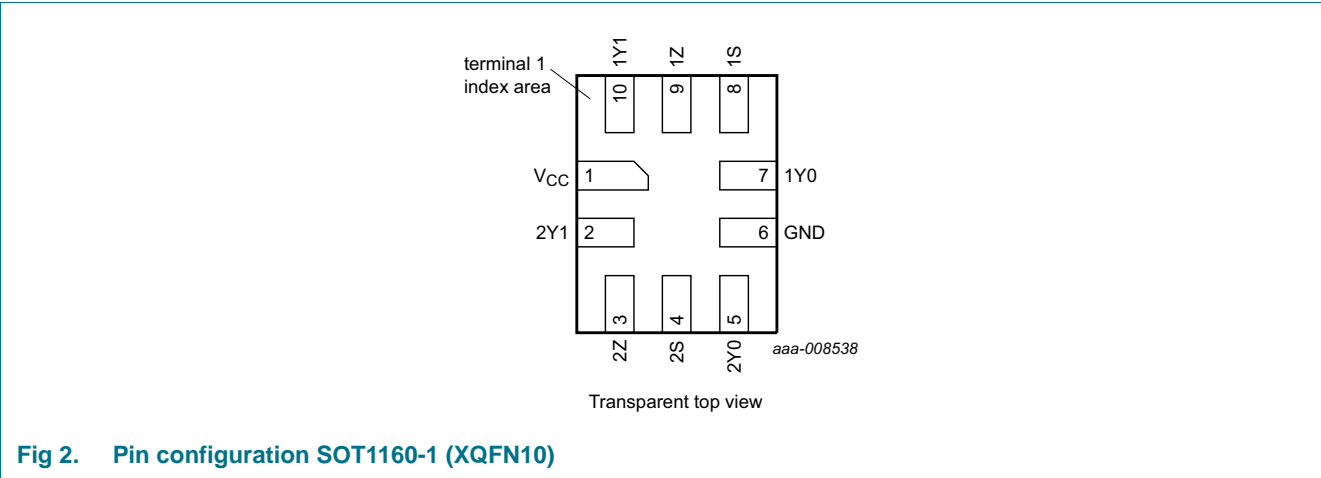


Fig 2. Pin configuration SOT1160-1 (XQFN10)

## 7.2 Pin description

**Table 3.** Pin description

Symbol	Pin	Description
V <sub>CC</sub>	1	supply voltage
2Y0, 1Y0	5, 7	independent input or output
2Z, 1Z	3, 9	common output or input
2S, 1S	4, 8	select input
GND	6	ground (0 V)
2Y1, 1Y1	2, 10	independent input or output

## 8. Functional description

**Table 4.** Function table<sup>[1]</sup>

Input nS	Channel on
L	nY0 = nZ
H	nY1 = nZ

[1] H = HIGH voltage level; L = LOW voltage level.

## 9. Limiting values

**Table 5.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+5.5	V
V <sub>I</sub>	input voltage	pins nS	<sup>[1]</sup> -0.5	+5.5	V
V <sub>SW</sub>	switch voltage		-4.0	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SK</sub>	switch clamping current	V <sub>I</sub> < -4.0 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±50	mA
I <sub>SW</sub>	switch current	T <sub>amb</sub> = 25 °C	-	±250	mA
		T <sub>amb</sub> = 25 °C; peak current (pulsed at 1 ms duration; < 10 % duty cycle)	-	±500	mA
I <sub>CC</sub>	supply current		-	+50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

## 10. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.8	5.0	V
$V_I$	input voltage	pins nS	0	5.0	V
$V_{SW}$	switch voltage		[1] -2.5	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+85	°C

[1] The voltage across the switch should be  $< 5.5$  V.

## 11. Static characteristics

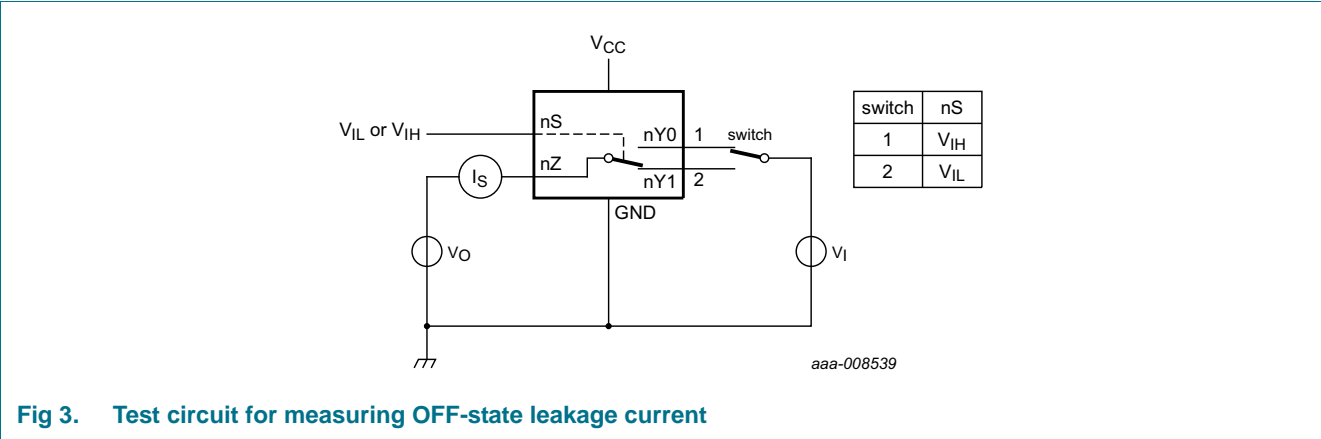
**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			Unit
			Min	Typ[1]	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.7\text{ V to }4.3\text{ V}$	1.4	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.7\text{ V to }4.3\text{ V}$	-	-	0.6	V
$V_{IK}$	input clamping voltage	$V_{CC} = 3.0\text{ V}; I_I = -18\text{ mA}$	-	-	-1.2	V
$I_I$	input leakage current	pins nS; $V_I = 0\text{ V to }V_{CC}$ ; $V_{CC} = 0\text{ V to }4.3\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 2.7\text{ V}; V_I = -2.5\text{ V or }2.5\text{ V}; V_O = 2.5\text{ V or }-2.5\text{ V}$ ; see <a href="#">Figure 3</a>	-	-	$\pm 250$	nA
$I_{CC}$	supply current	$V_I = V_{CC}\text{ or GND}; V_{SW} = \text{GND or }V_{CC}; V_{CC} = 2.7\text{ V}$			2	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	$V_I = 2.6\text{ V}; V_{SW} = \text{GND or }V_{CC}; V_{CC} = 4.3\text{ V}$	-	-	10	$\mu\text{A}$
		$V_I = 1.8\text{ V}; V_{SW} = \text{GND or }V_{CC}; V_{CC} = 4.3\text{ V}$	-	-	15	$\mu\text{A}$
$C_I$	input capacitance	pins nS	-	1.5	-	pF
$C_{S(OFF)}$	OFF-state capacitance	pins nY0 and nY1; $V_{CC} = 3.3\text{ V}; V_I = 0\text{ V to }3.3\text{ V}$	-	35	-	pF
$C_{S(ON)}$	ON-state capacitance	pins nZ; $V_{CC} = 3.3\text{ V}; V_I = 0\text{ V to }3.3\text{ V}$	-	75	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 3.3\text{ V}$ .

11.1 Test circuits



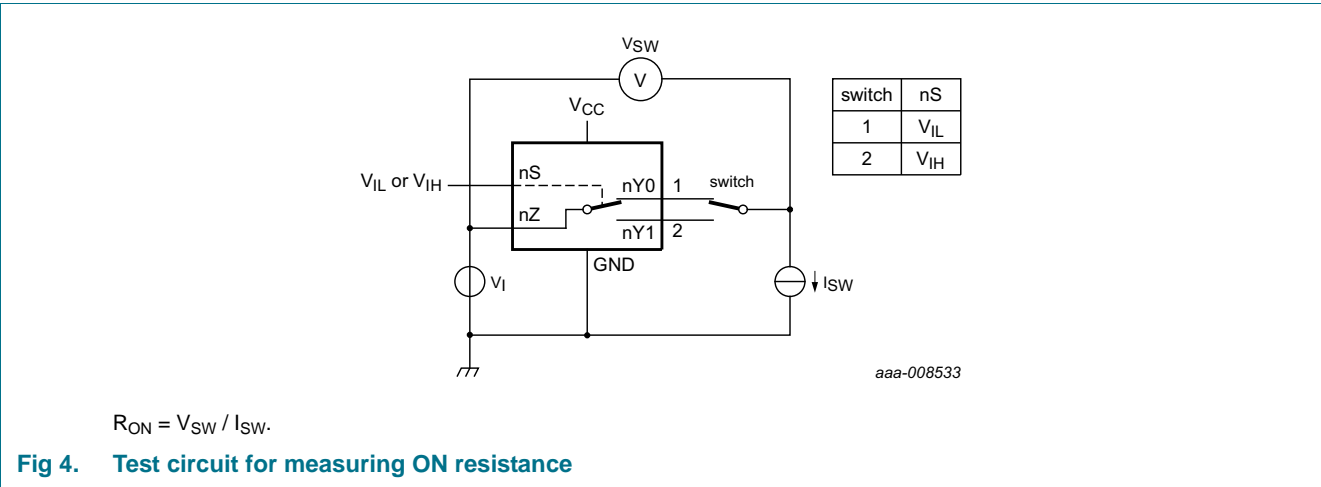
11.2 ON resistance

Table 8. ON resistance
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Table with 6 columns: Symbol, Parameter, Conditions, and a group of three columns for temperature ranges (-40 °C to +85 °C) with sub-columns Min, Typ, and Max, plus a Unit column.

- [1] Typical values are measured at Tamb = 25 °C.
- [2] Measured at identical VCC, temperature and input voltage.

11.3 ON resistance test circuit and graphs



## 12. Dynamic characteristics

**Table 9. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ <sup>[1]</sup>	Max	
$t_{en}$	enable time	nS to nZ; see <a href="#">Figure 5</a>				
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ <a href="#">[2]</a>	-	80	160	ns
		$V_{CC} = 3.6\text{ V to }4.3\text{ V}$ <a href="#">[3]</a>	-	70	120	ns
$t_{dis}$	disable time	nS to nZ; see <a href="#">Figure 5</a>				
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ <a href="#">[2]</a>	-	25	50	ns
		$V_{CC} = 3.6\text{ V to }4.3\text{ V}$ <a href="#">[3]</a>	-	25	50	ns
$t_{b-m}$	break-before-make time	see <a href="#">Figure 6</a> <a href="#">[4]</a>				
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	15	55	-	ns
		$V_{CC} = 3.6\text{ V to }4.3\text{ V}$	12	45	-	ns

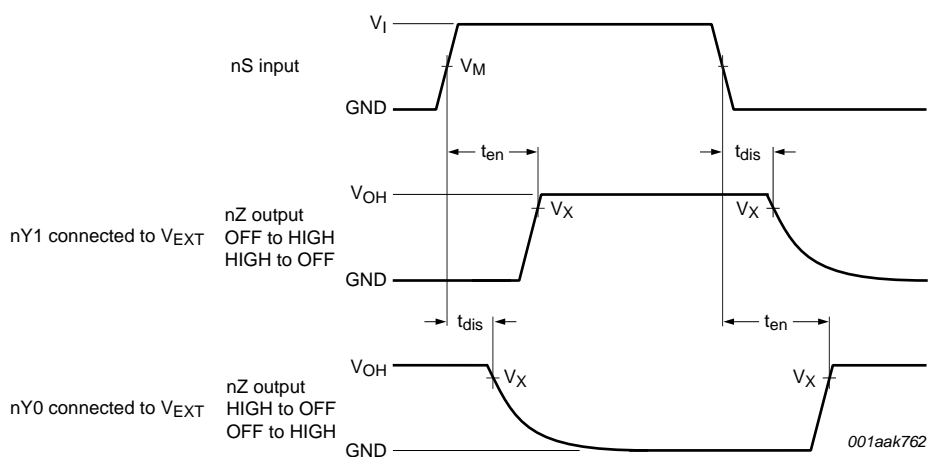
[1] Typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .

[3] Typical values are measured at  $V_{CC} = 4.3\text{ V}$ .

[4] Guaranteed by design.

### 12.1 Waveform and test circuits



Measurement points are given in [Table 10](#).

Logic level:  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with the output load.

**Fig 5. Enable and disable times**

**Table 10. Measurement points**

Supply voltage	Input		Output
$V_{CC}$	$V_M$	$V_I$	$V_X$
2.7 V to 4.3 V	$0.5V_{CC}$	$V_{CC}$	$0.9V_{OH}$

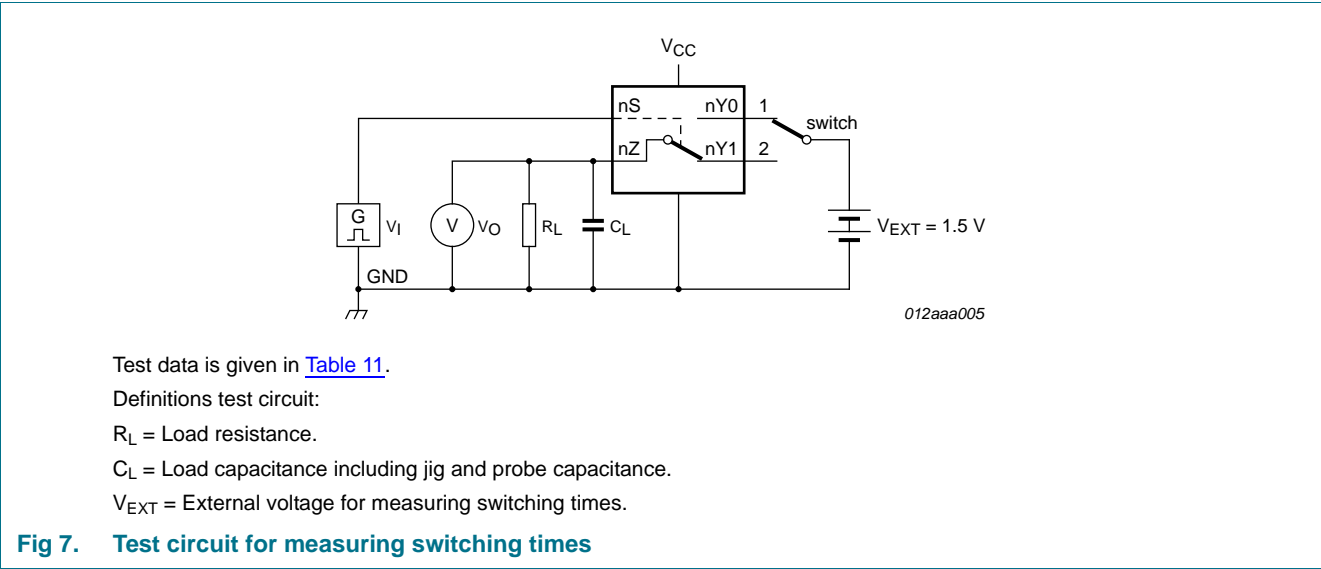
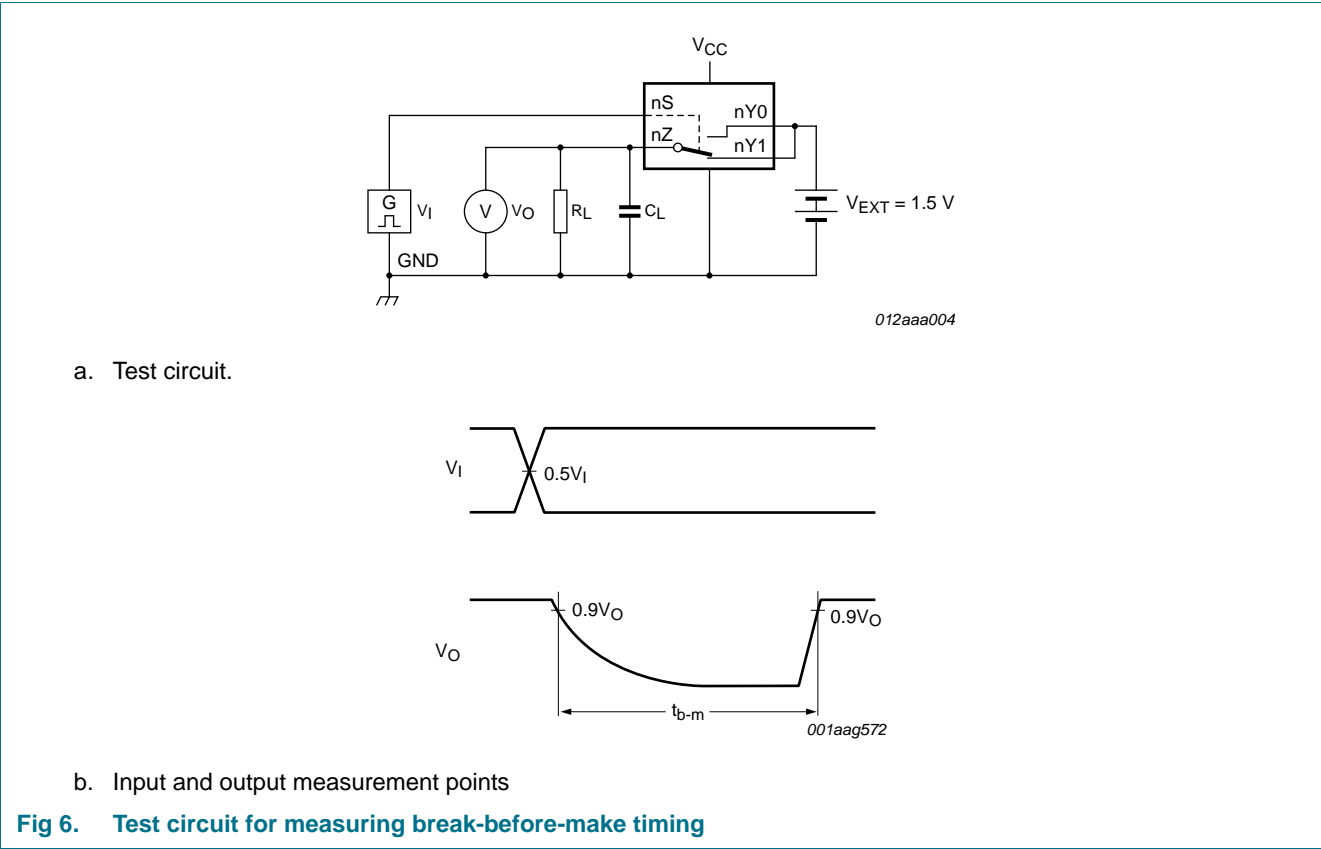


Table 11. Test data

Supply voltage	Input		Load	
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$
2.7 V to 4.3 V	$V_{CC}$	$\leq 2.5 \text{ ns}$	35 pF	50 $\Omega$

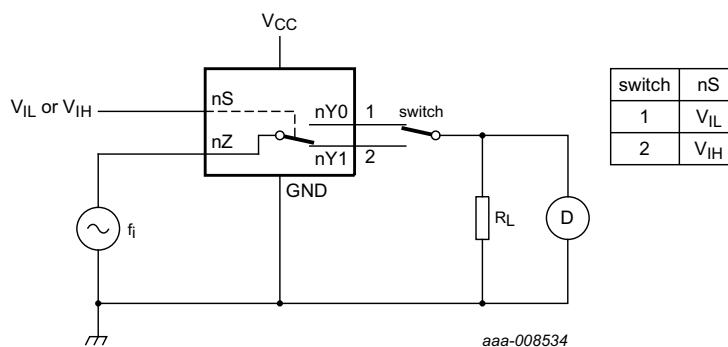
## 12.2 Additional dynamic characteristics

**Table 12. Additional dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $V_I = \text{GND}$  or  $V_{CC}$  (unless otherwise specified);  $t_r = t_f \leq 2.5 \text{ ns}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

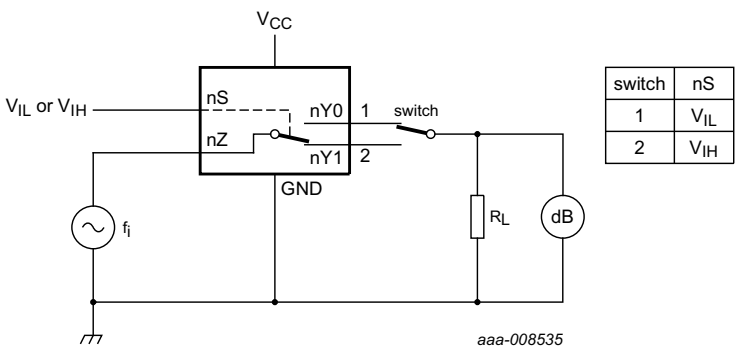
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 20 \text{ Hz to } 20 \text{ kHz}$ ; $R_L = 32 \text{ } \Omega$ ; see <a href="#">Figure 8</a>				
		$V_{CC} = 2.7 \text{ V}$ ; $V_I = 2 \text{ V (p-p)}$	-	0.07	-	%
		$V_{CC} = 4.3 \text{ V}$ ; $V_I = 2 \text{ V (p-p)}$	-	0.03	-	%
$f_{(-3\text{dB})}$	–3 dB frequency response	$R_L = 50 \text{ } \Omega$ ; see <a href="#">Figure 9</a>				
		$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$	-	100	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	$f_i = 100 \text{ kHz}$ ; $R_L = 50 \text{ } \Omega$ ; see <a href="#">Figure 10</a>				
		$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$	-	–60	-	dB
Xtalk	crosstalk	between switches; $f_i = 100 \text{ kHz}$ ; $R_L = 50 \text{ } \Omega$ ; see <a href="#">Figure 11</a>				
		$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$	-	–60	-	dB
$Q_{inj}$	charge injection	$f_i = 1 \text{ MHz}$ ; $C_L = 0.1 \text{ nF}$ ; $R_L = 1 \text{ M}\Omega$ ; $V_{gen} = 0 \text{ V}$ ; $R_{gen} = 0 \text{ } \Omega$ ; see <a href="#">Figure 12</a>				
		$V_{CC} = 2.7 \text{ V}$	-	3	-	pC
		$V_{CC} = 3.3 \text{ V}$	-	4	-	pC
		$V_{CC} = 4.3 \text{ V}$	-	5	-	pC

## 12.3 Test circuits



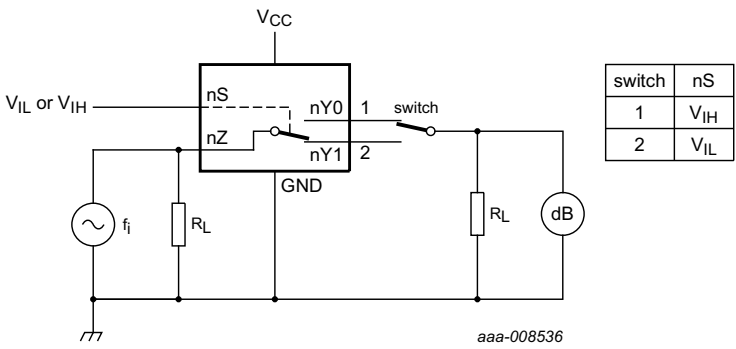
**Fig 8. Test circuit for measuring total harmonic distortion**





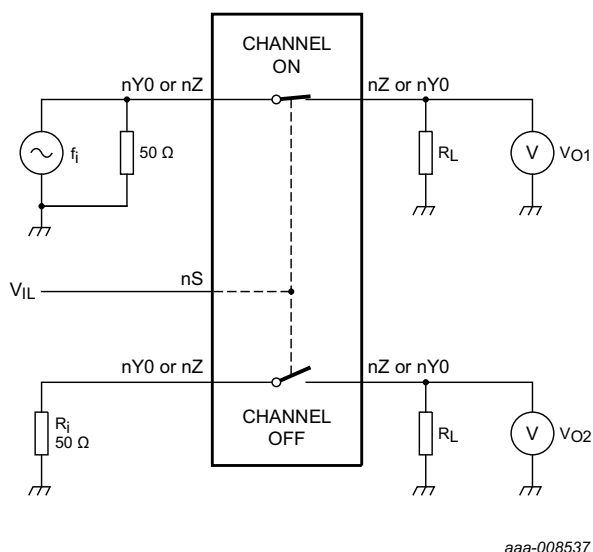
Adjust  $f_i$  voltage to obtain 0 dBm level at output. Increase  $f_i$  frequency until dB meter reads -3 dB.

Fig 9. Test circuit for measuring the frequency response when channel is in ON-state



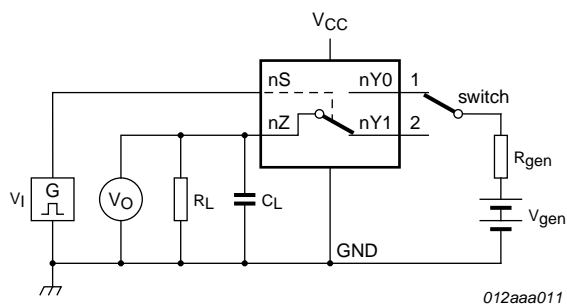
Adjust  $f_i$  voltage to obtain 0 dBm level at input.

Fig 10. Test circuit for measuring isolation (OFF-state)

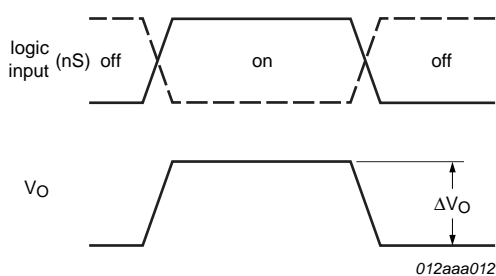


$20 \log_{10} (V_{O2} / V_{O1})$  or  $20 \log_{10} (V_{O1} / V_{O2})$ .

**Fig 11. Test circuit for measuring crosstalk between switches**



a. Test circuit



b. Input and output pulse definitions

Definition:  $Q_{inj} = \Delta V_O \times C_L$ .

$\Delta V_O$  = output voltage variation.

$R_{gen}$  = generator resistance.

$V_{gen}$  = generator voltage.

**Fig 12. Test circuit for measuring charge injection**

13. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads;  
10 terminals; body 1.40 x 1.80 x 0.50 mm

SOT1160-1

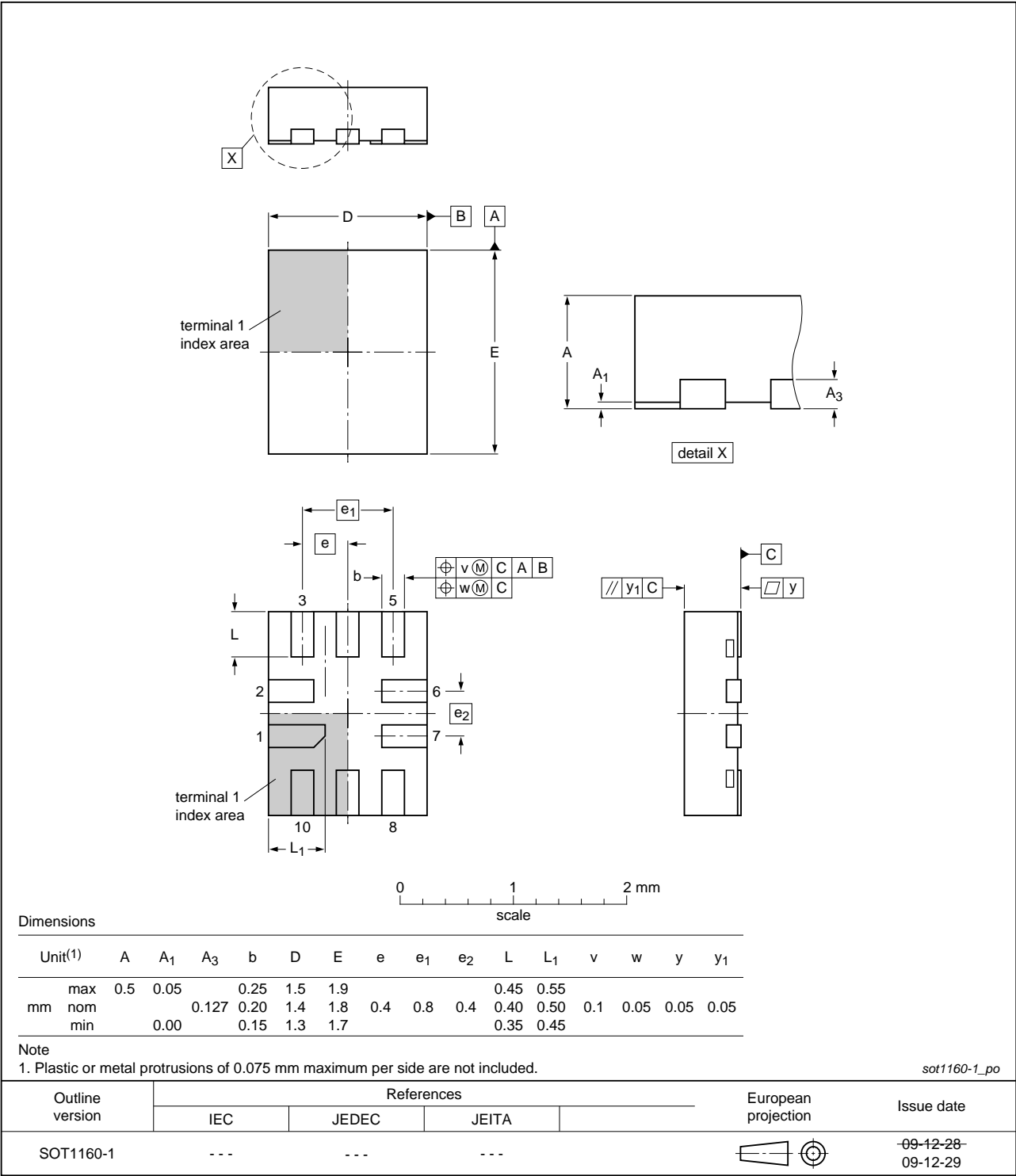


Fig 13. Package outline SOT1160-1 (XQFN10)

## 14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

## 15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5L2750C v.1	20130906	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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