

2-Mbit (128K x 16) Static RAM

Features

- **High speed**
 - 55 ns
- **Temperature Ranges**
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- **Wide voltage range**
 - 2.7V – 3.6V
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in a Pb-free and non Pb-free 44-pin TSOP Type II (forward pinout) and 48-ball FBGA packages**

Functional Description^[1]

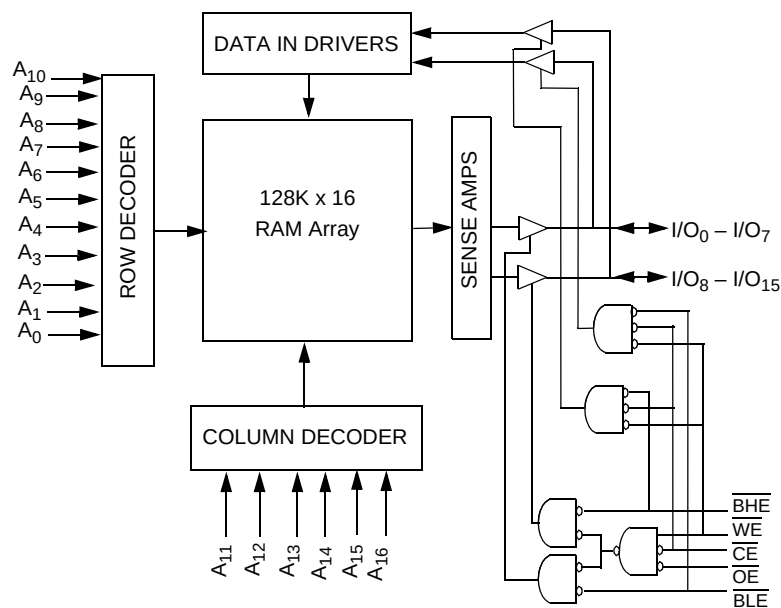
The CY62136V is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{\text{CE}}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram

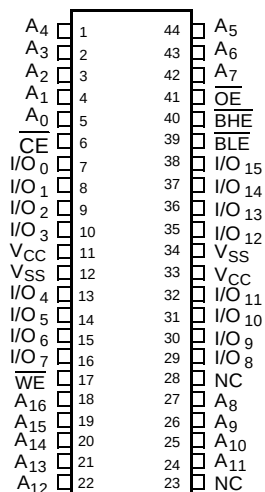
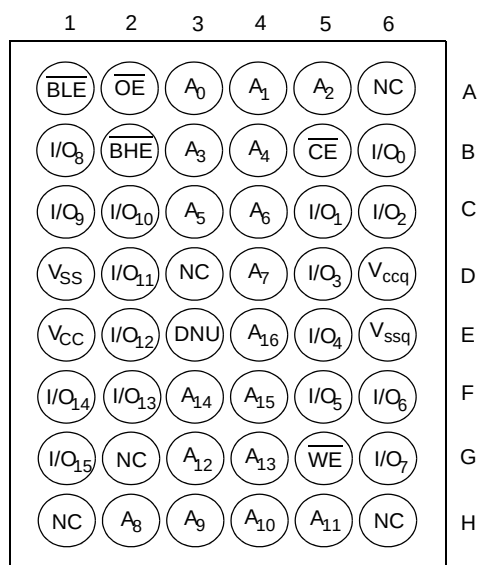


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	V _{CC} Range (V)			Speed	Grades	Power Dissipation (Industrial)			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
	Min.	Typ. ^[2]	Max.			Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62136VLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
				70	Industrial	7	15	1	15
					Automotive	7	20	1	20

Pin Configurations^[3, 4]
**TSOP II (Forward)
Top View**

**48-ball FBGA
Top View**

Notes:

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.
- NC pins are not connected on the die.
- E3 (DNU) pin have to be left floating or tied to V_{SS} to ensure proper operation.

Pin Definitions

Pin Number	Type	Description
1–5, 18–22, 24–27, 42–45	Input	A₀–A₁₆ . Address Inputs
7–10, 13–16, 29–32, 35–38	Input/Output	I/O₀–I/O₁₅ . Data lines. Used as input or output lines depending on operation
23	No Connect	NC . This pin is not connected to the die
17	Input/Control	$\overline{WE}$. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
6	Input/Control	$\overline{CE}$. When LOW, selects the chip. When HIGH, deselects the chip
40, 39	Input/Control	$\overline{BHE}$, $\overline{BLE}$. $\overline{BHE}$ = LOW selects higher order byte WRITES or READs on the SRAM $\overline{BLE}$ = LOW selects lower order byte WRITES or READs on the SRAM
41	Input/Control	$\overline{OE}$. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are Tri-stated, and act as input data pins
12, 34	Ground	V_{SS} . Ground for the device
11, 33	Power Supply	V_{CC} . Power supply for the device

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs

in High-Z State^[5] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[5] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature [T_A] ^[7]	V_{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62136V-55			CY62136V-70			Unit	
				Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V	2.4			2.4			V	
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V			0.4			0.4	V	
V _{IH}	Input HIGH Voltage		V _{CC} = 3.6V	2.2		V _{CC} +0.5V	2.2		V _{CC} +0.5V	V	
V _{IL}	Input LOW Voltage		V _{CC} = 2.7V	−0.5		0.8	−0.5		0.8	V	
I _{Ix}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		Industrial	−1	+1	−1		+1	μA	
				Automotive			−10		+10	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		Industrial	−1	+1	−1		+1	μA	
				Automotive			−10		+10	μA	
I _{CC}	V _{CC} Operating Supply Current	f = f _{Max} = 1/t _{RC} ,	V _{CC} = 3.6V, I _{OUT} = 0 mA, CMOS Levels	Industrial		7	20		7	15	mA
				Automotive					7	20	mA
		f = 1 MHz,				1	2		1	2	mA
I _{SB1}	Automatic CE Power-down Current—CMOS Inputs	CE ≥ V _{CC} −0.3V, V _{IN} ≥ V _{CC} −0.3V or V _{IN} ≤ 0.3V, f = f _{Max}					100			100	μA
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	CE ≥ V _{CC} −0.3V V _{IN} ≥ V _{CC} −0.3V or V _{IN} ≤ 0.3V, f = 0	V _{CC} = 3.6V	Industrial		1	15		1	15	μA
				Automotive					1	20	

Capacitance^[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance^[6]

Parameter	Description	Test Conditions	FBGA	TSOPII	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 2-layer printed circuit board	41.17	60	$^\circ C/W$
Θ_{JC}	Thermal Resistance (Junction to Case)		11.74	22	$^\circ C/W$

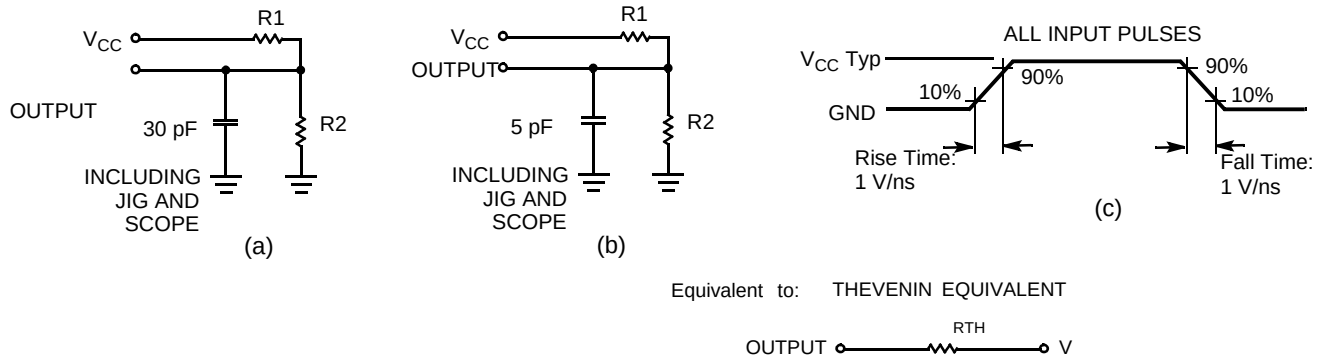
Notes:

5. $V_{IL}(\text{min}) = -2.0V$ for pulse durations less than 20 ns.

6. Tested initially and after any design or process changes that may affect these parameters.

7. T_A is the "Instant-On" case temperature.

AC Test Loads and Waveforms

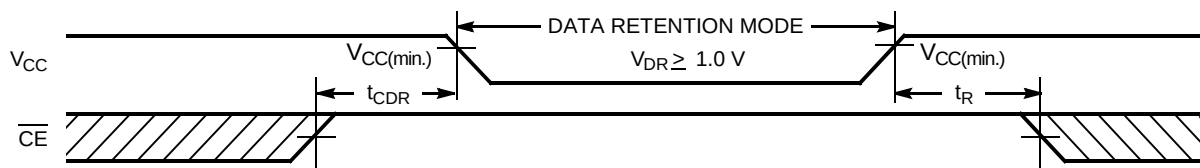


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[9]	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, No input may exceed $V_{CC} + 0.3V$		0.5	7.5	μA
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		70			ns

Data Retention Waveform



Notes:

- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100 \mu s$ or stable at $V_{CC(min.)} \geq 100 \mu s$.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.

Switching Characteristics Over the Operating Range ^[9]

Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low-Z ^[10]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[10, 11]		25		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low-Z ^[10]	10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High-Z ^[10, 11]		25		25	ns
t _{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-down		55		70	ns
t _{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		25		35	ns
t _{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z ^[10, 11]	5		5		ns
t _{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z ^[12]		25		25	ns
Write Cycle ^[12, 13]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t _{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		60		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[10, 11]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[10]	5		10		ns

Notes:

10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.

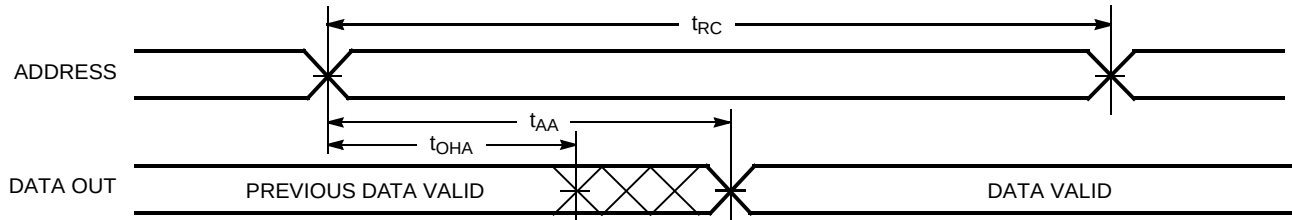
11. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

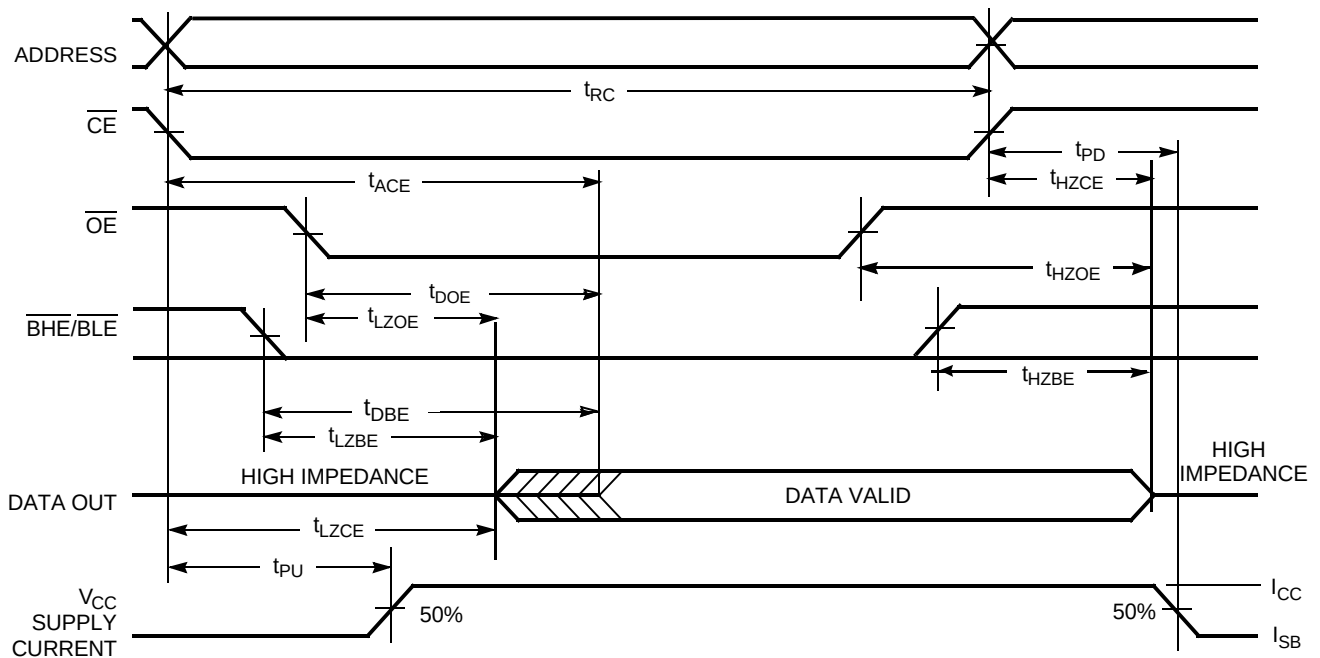
13. The minimum write cycle time for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[14, 15]



Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[15, 16]

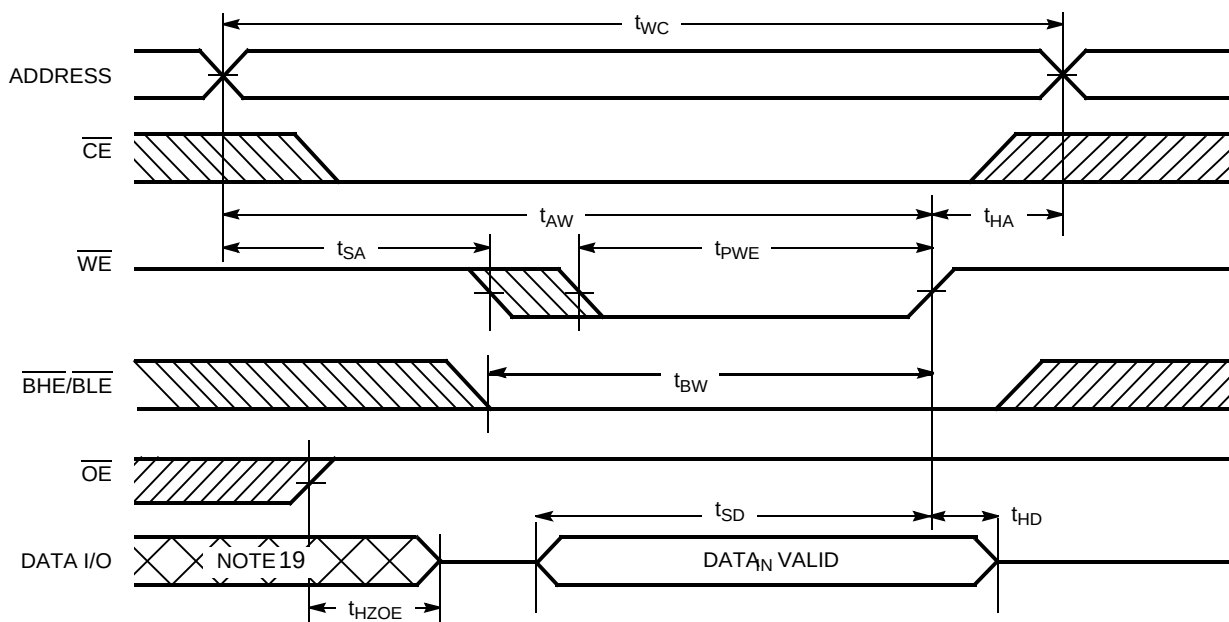


Notes:

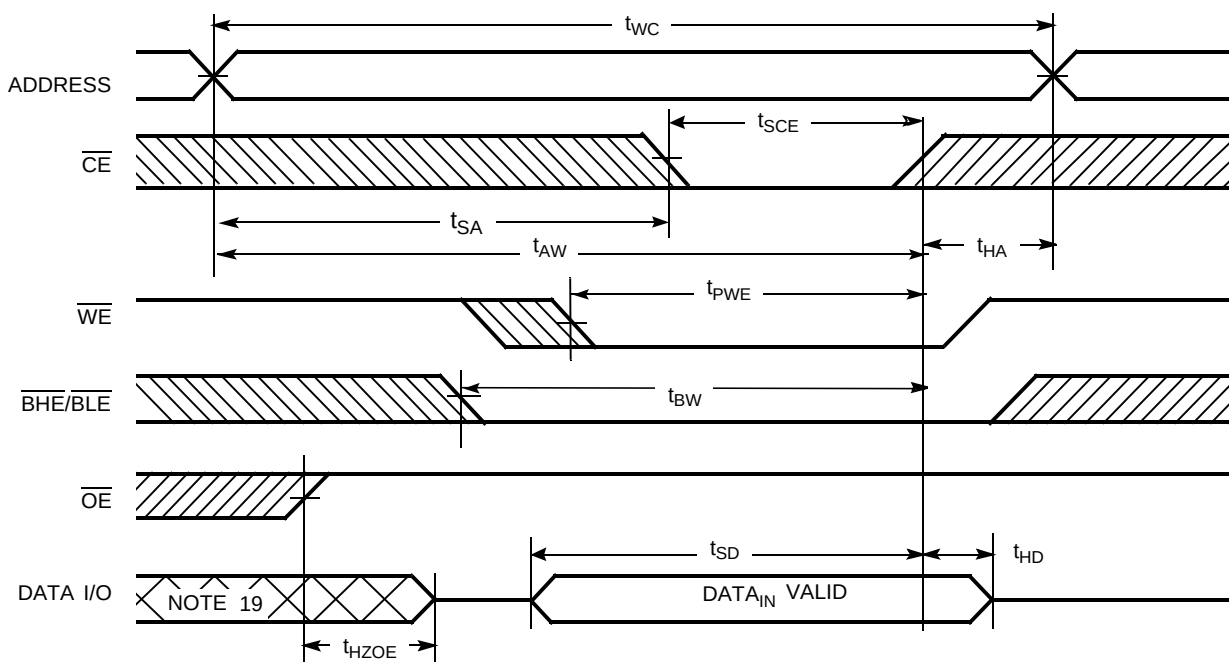
14. Device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}$.
15. WE is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)^[12, 17, 18]



Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[12, 17, 18]

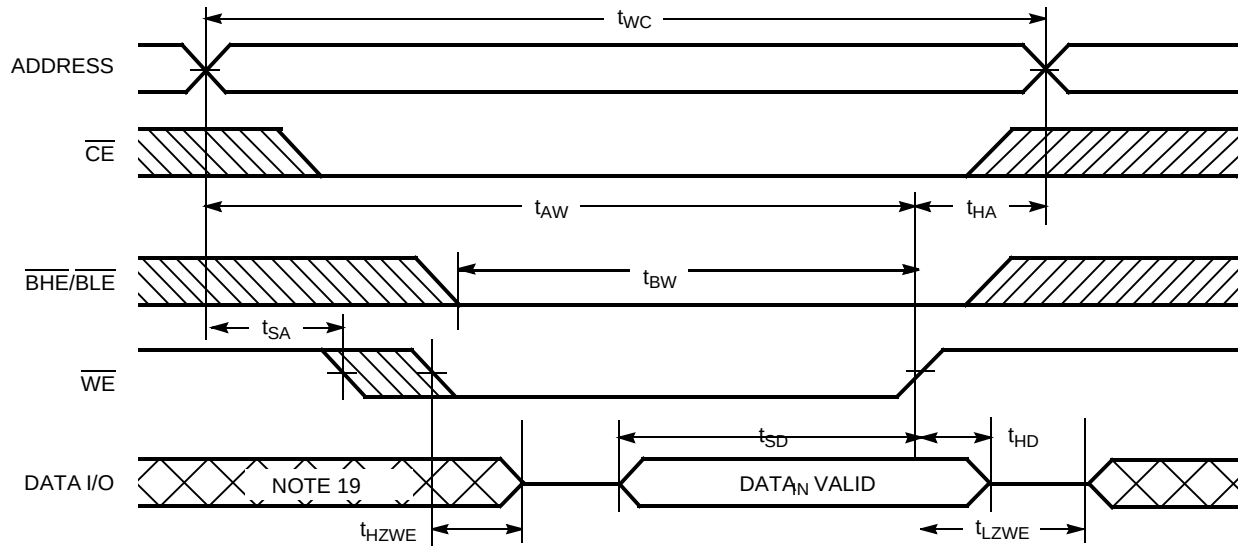


Notes:

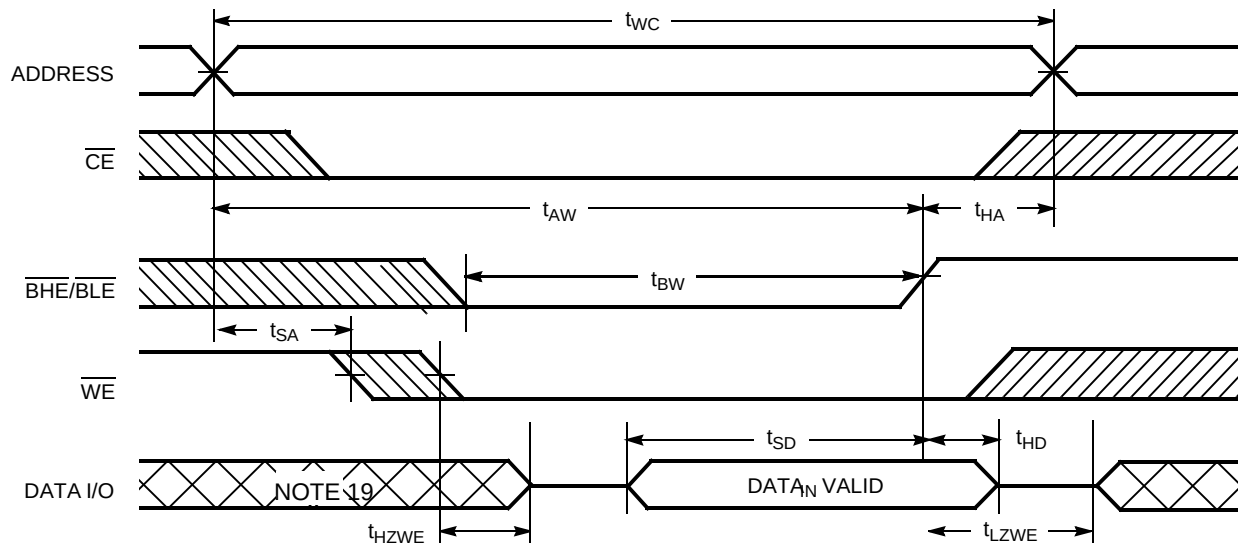
17. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

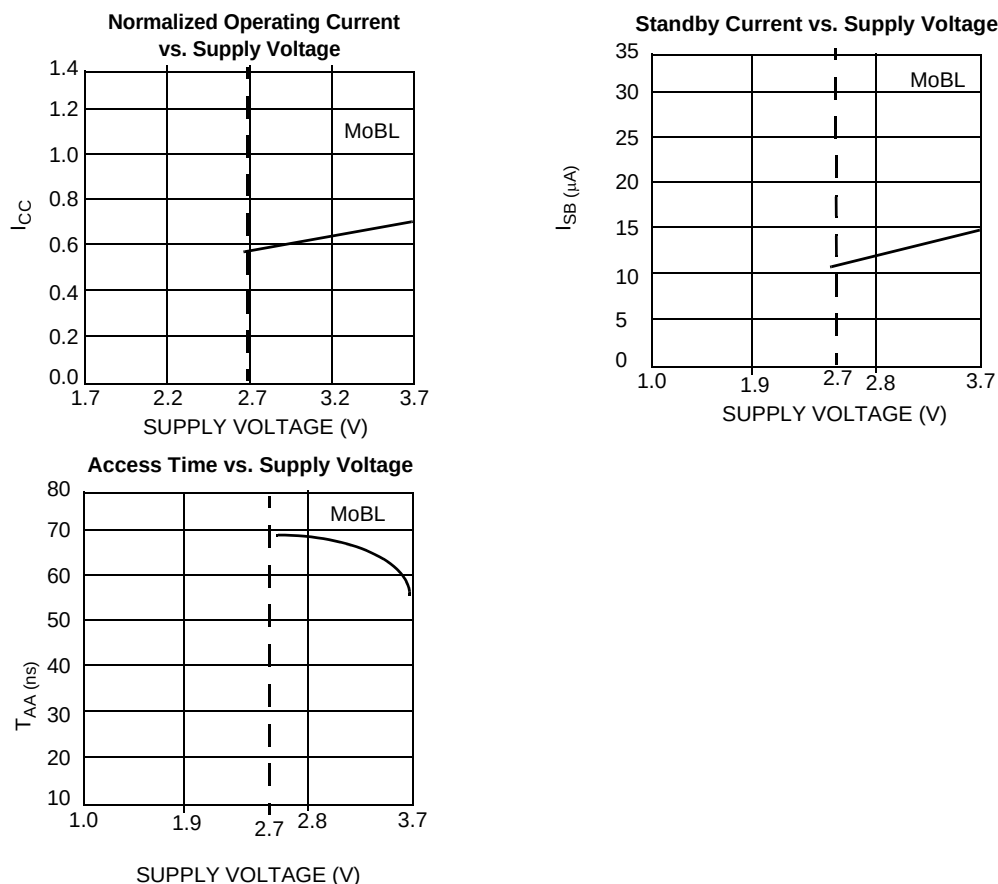
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[13, 18]



Write Cycle No. 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[19]



Typical DC and AC Characteristics



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	High Z (I/O_8 – I/O_{15}); Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	High Z (I/O_8 – I/O_{15}); Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active (I_{CC})

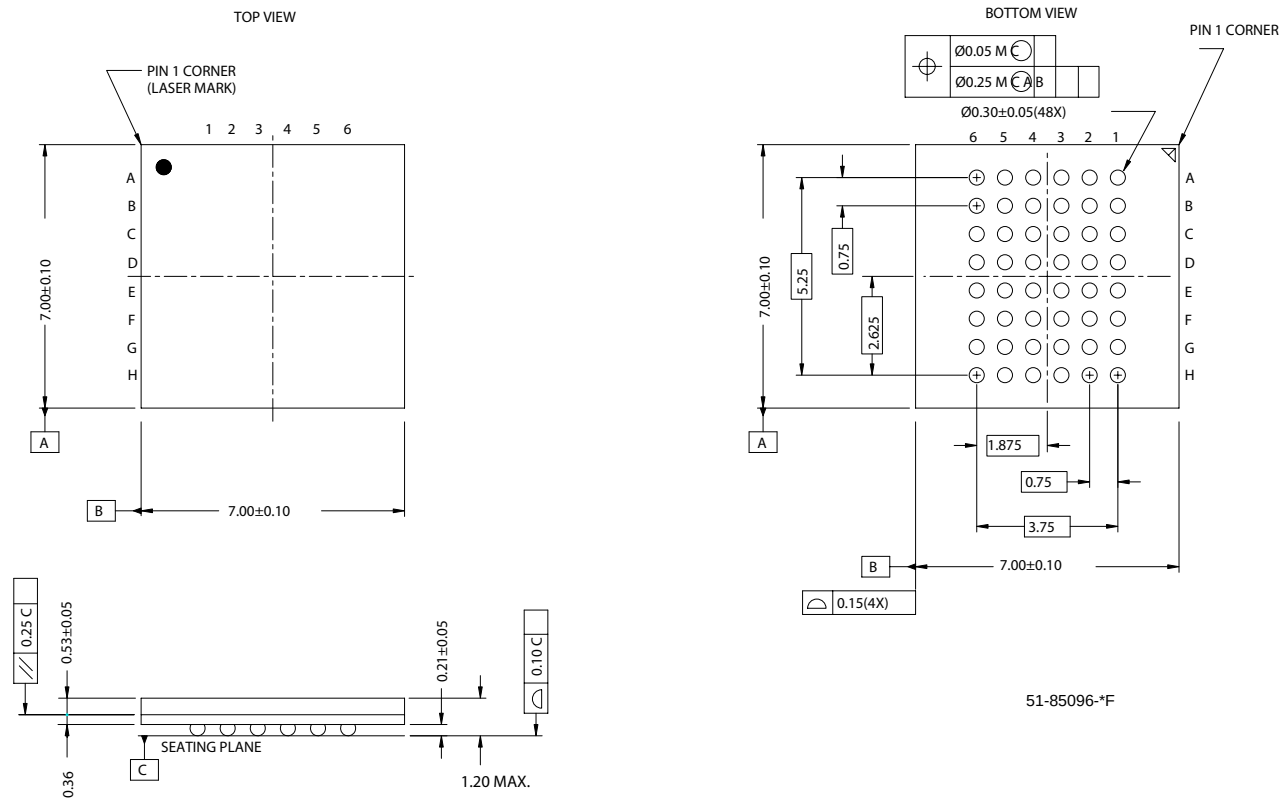
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62136VLL-55BAI	51-85096	48-ball Fine-Pitch Ball Grid Array (7 x 7 x 1.2 mm)	Industrial
	CY62136VLL-55ZI	51-85087	44-pin TSOP II	
	CY62136VLL-55ZXI		44-pin TSOP II (Pb-free)	
70	CY62136VLL-70BAI	51-85096	48-ball Fine-Pitch Ball Grid Array (7 x 7 x 1.2 mm)	Industrial
	CY62136VLL-70ZI	51-85087	44-pin TSOP II	
	CY62136VLL-70ZXI		44-pin TSOP II (Pb-free)	
	CY62136VLL-70ZSE		44-pin TSOP II	Automotive
	CY62136VLL-70ZSXE		44-pin TSOP II (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

48-ball FBGA (7 x 7 x 1.2 mm) (51-85096)





Document History Page

Document Title: CY62136V MoBL® 2-Mbit (128K x 16) Static RAM Document Number: 38-05087				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107347	05/25/01	SZV	Changed from Spec #: 38-00728 to 38-05087
*A	116509	09/04/02	GBI	Added footnote 1 Added SL power bin Deleted fBGA package; replacement fBGA package available in CY62136CV30
*B	269729	See ECN	SYT	Added Automotive Information for 70-ns Speed Bin. Added Footnotes # 3 and # 6. Corrected Typo in Electrical Characteristics for I _{CC} (Max)-55 ns from 15 to 20 mA. Added SL row for I _{SB2} in the Electrical Characteristics table. Changed Package Name from Z44 to ZS44. Replaced 'Z' with 'ZS' in the Ordering Code.
*C	344595	See ECN	SYT	Added Lead-Free Package on page# 9 Changed Package Name from ZS44 to Z44 for the 44 TSOP II Package Replaced 'ZS' with 'Z' in the Ordering Code for Industrial
*D	486789	See ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court". Added FBGA Package for Industrial Operating range. Removed SL Power bin. Updated Ordering Information table.