TC74HC02P QUAD 2-INPUT NOR GATE

The TC74HC02 is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

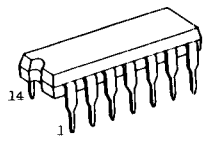
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

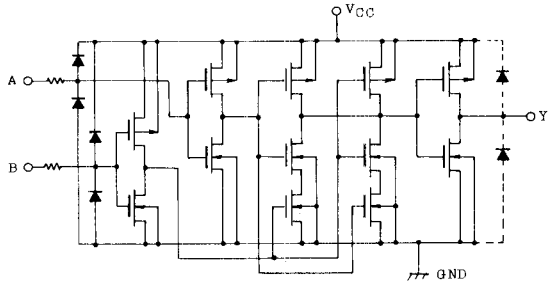
FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~ 6V
- Pin and Function Compatible with 74LS02

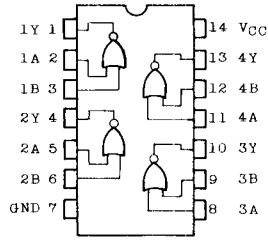


DIP(5-21F)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

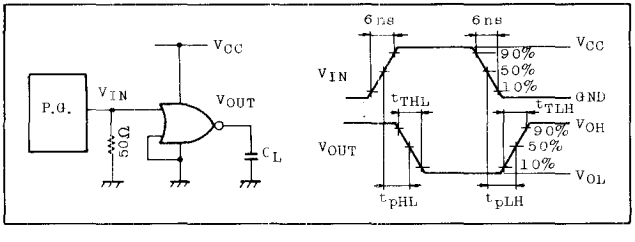
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.32	-	0.37	
			I_{OL}=5.2mA	6.0	-	0.18	0.32	-	0.37	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

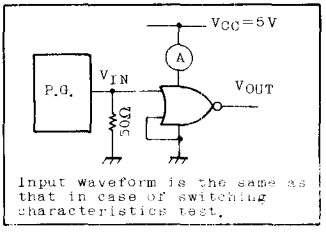
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	22	75	-	90	ns
			4.5	-	8	15	-	18	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	33	90	-	110	ns
			4.5	-	10	18	-	22	
	t_{pHL}		6.0	-	9	16	-	19	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT

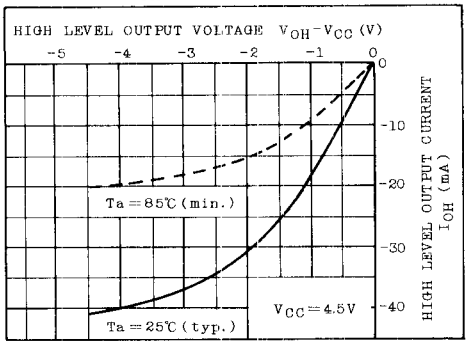


$I_{CC(opr)}$ TEST CIRCUIT

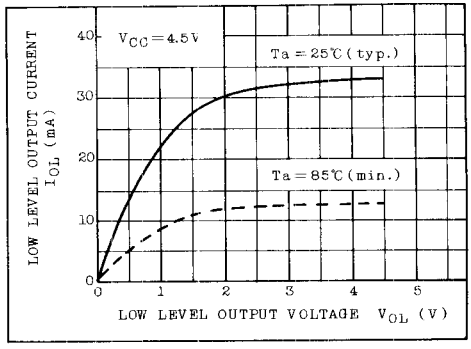


Input waveform is the same as that in case of switching characteristics test.

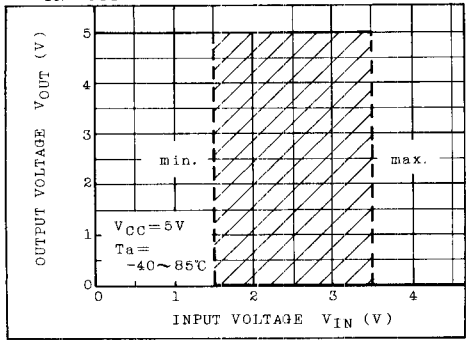
I_{OH} CHARACTERISTICS



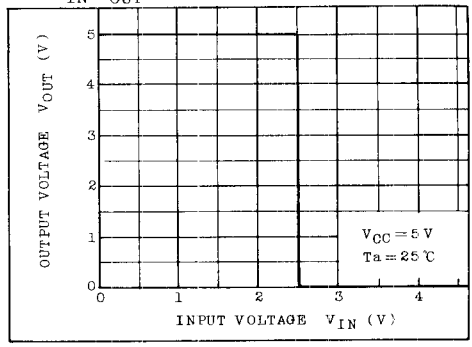
I_{OL} CHARACTERISTICS



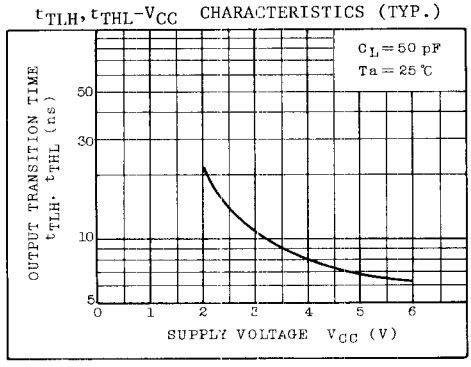
V_{IN}-V_{OUT} CHARACTERISTICS (MIN., MAX.)



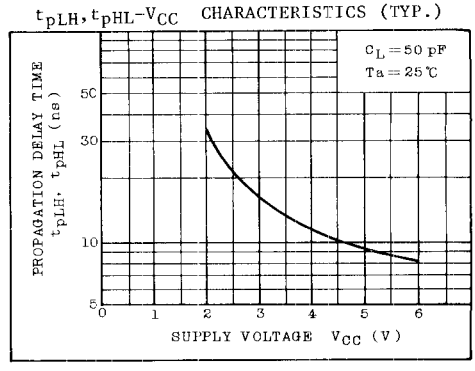
V_{IN}-V_{OUT} CHARACTERISTICS (TYP.)



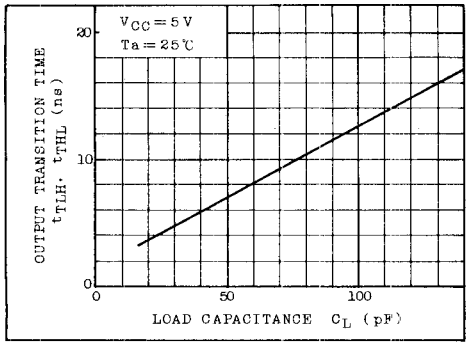
t_{TLH}, t_{THL}-V_{CC} CHARACTERISTICS (TYP.)



t_{pLH}, t_{pHL}-V_{CC} CHARACTERISTICS (TYP.)



t_{TLH}, t_{THL}-C_L CHARACTERISTICS (TYP.)



t_{pLH}, t_{pHL}-C_L CHARACTERISTICS (TYP.)