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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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H5N2504DL, H5N2504DS

Silicon N Channel MOS FET
High Speed Power Switching

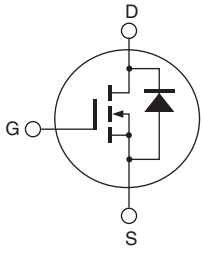
ADE-208-1375A (Z)

2nd. Edition
Jun. 2002

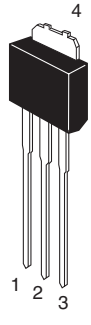
Features

- Low on-resistance
- Low leakage current
- High speed switching
- Low gate charge
- Avalanche ratings

Outline

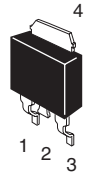


DPAK-2



H5N2504DL

DPAK-S



H5N2504DS

1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	7	A
Drain peak current	$I_{D\ (pulse)}$ Note1	28	A
Body-drain diode reverse drain current	I_{DR}	7	A
Body-drain diode reverse drain peak current	$I_{DR\ (pulse)}$ Note1	28	A
Avalanche current	I_{AP} Note3	7	A
Channel dissipation	Pch Note2	30	W
Channel to case Thermal Impedance	θ ch-c	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Tch ≤ 150°C

Electrical Characteristics

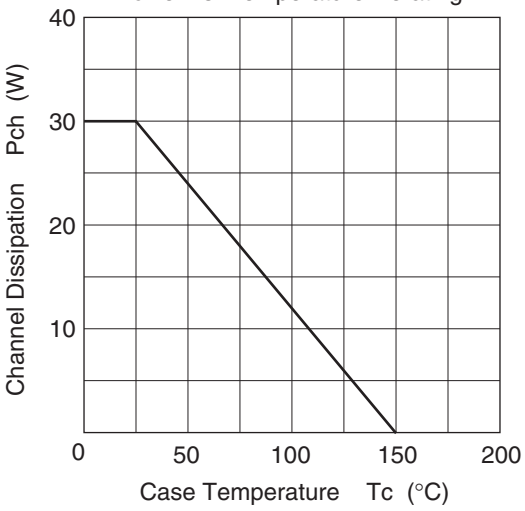
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 250 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.48	0.63	Ω	I_D = 3.5 A, V_{GS} = 10 V [Note4]
	$R_{DS(on)}$	—	0.5	0.67	Ω	I_D = 3.5 A, V_{GS} = 4 V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	5	8.5	—	S	I_D = 3.5 A, V_{DS} = 10 V [Note4]
Input capacitance	Ciss	—	570	—	pF	V_{DS} = 25 V
Output capacitance	Coss	—	60	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	12	—	pF	f = 1 MHz
Turn-on delay time	td(on)	—	13	—	ns	I_D = 3.5 A
Rise time	tr	—	18	—	ns	V_{GS} = 10 V
Turn-off delay time	td(off)	—	70	—	ns	R_L = 35.7 Ω
Fall time	tf	—	8	—	ns	Rg = 10 Ω
Total gate charge	Qg	—	21	—	nC	V_{DD} = 200 V
Gate to source charge	Qgs	—	2	—	nC	V_{GS} = 10 V
Gate to drain charge	Qgd	—	6	—	nC	I_D = 7 A
Body-drain diode forward voltage	V_{DF}	—	0.85	1.30	V	I_F = 7 A, V_{GS} = 0
Body-drain diode reverse recovery time	trr	—	120	—	ns	I_F = 7 A, V_{GS} = 0 diF/dt = 100 A/µs
Body-drain diode reverse recovery charge	Qrr	—	0.48	—	µC	

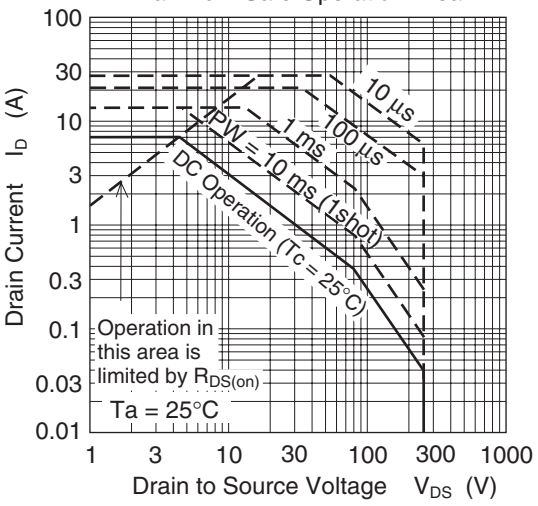
Notes: 4. Pulse test

Main Characteristics

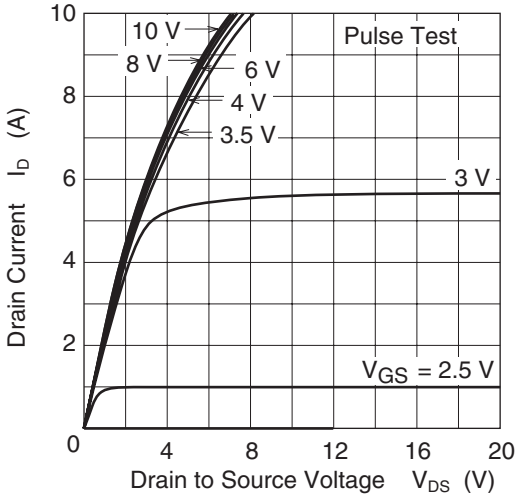
Power vs. Temperature Derating



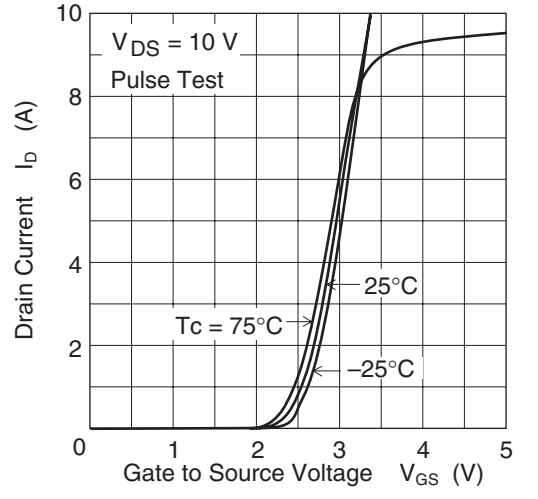
Maximum Safe Operation Area



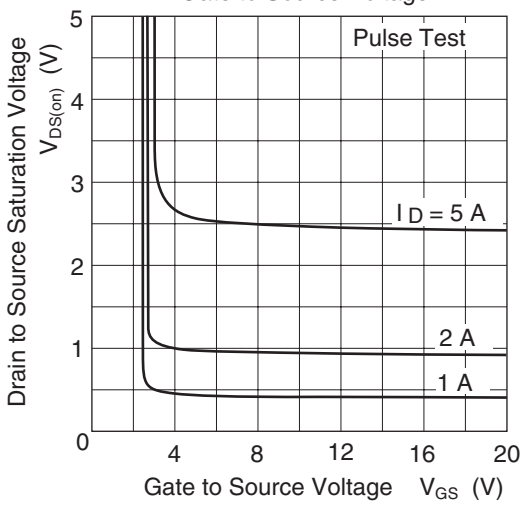
Typical Output Characteristics



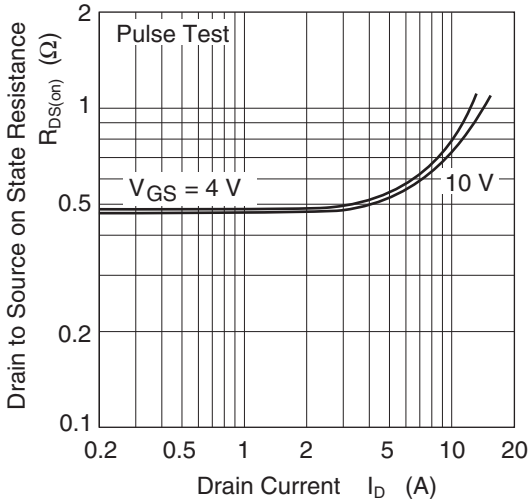
Typical Transfer Characteristics



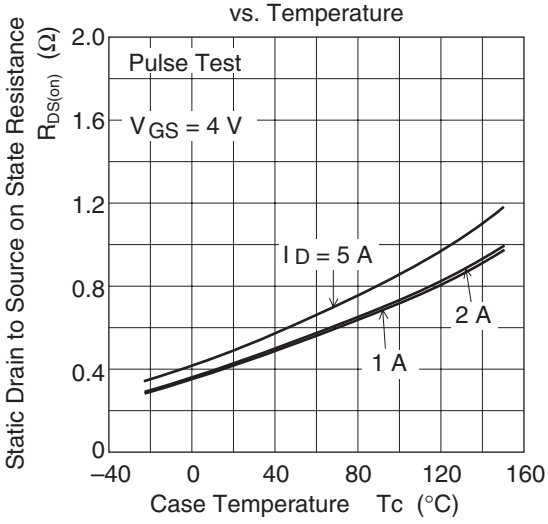
Drain to Source Saturation Voltage vs. Gate to Source Voltage



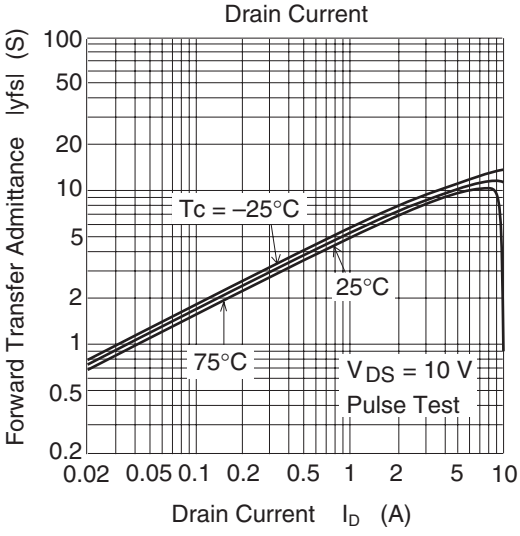
Static Drain to Source on State Resistance vs. Drain Current



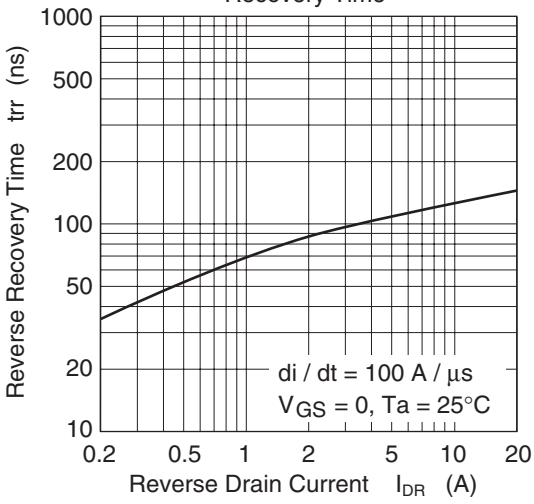
Static Drain to Source on State Resistance vs. Temperature



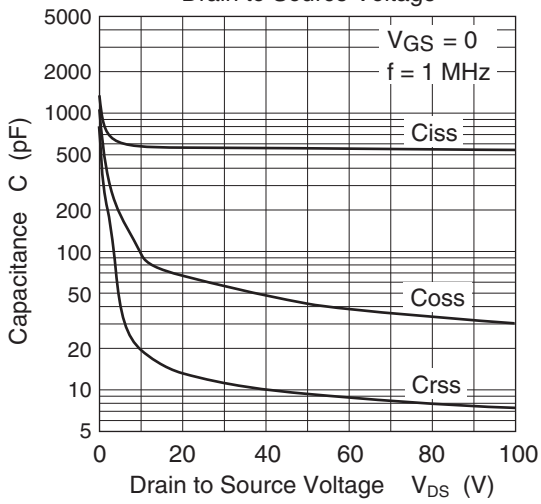
Forward Transfer Admittance vs. Drain Current



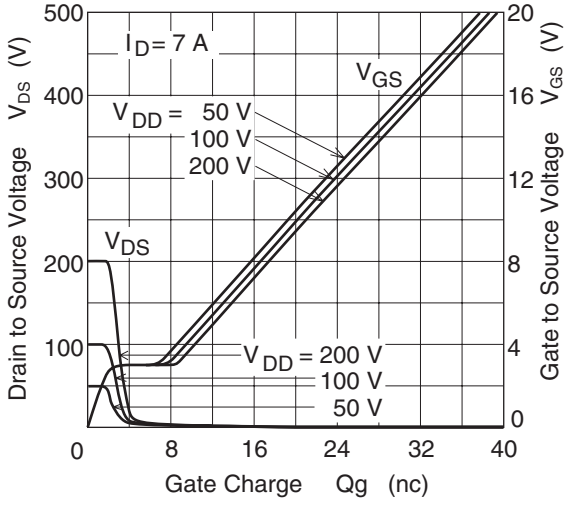
Body-Drain Diode Reverse Recovery Time



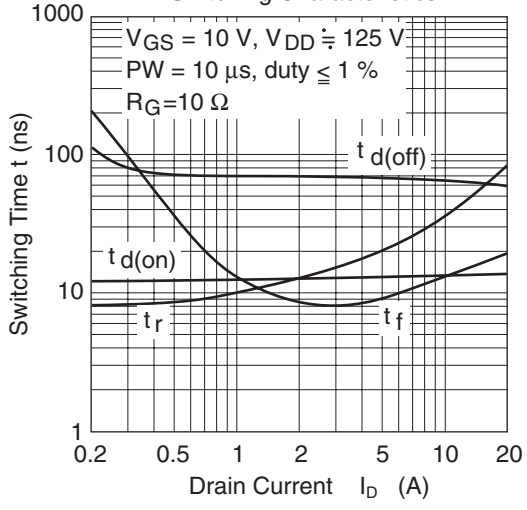
Typical Capacitance vs. Drain to Source Voltage



Dynamic Input Characteristics



Switching Characteristics



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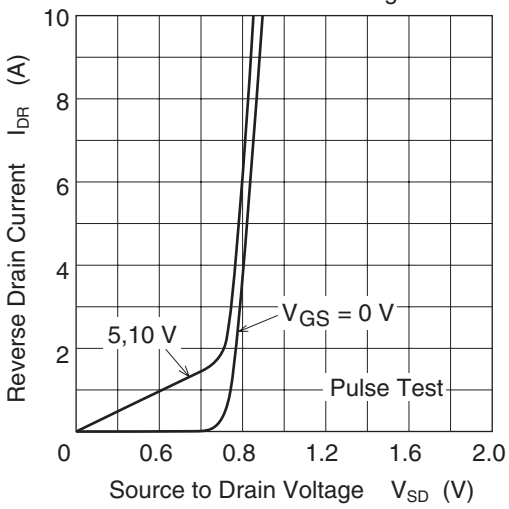
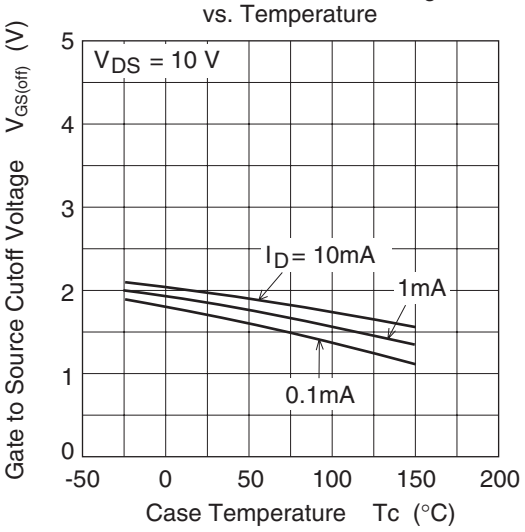
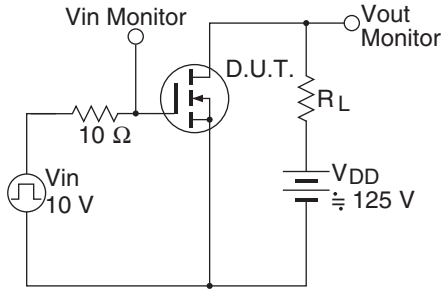
Reverse Drain Current vs. Source to Drain Voltage



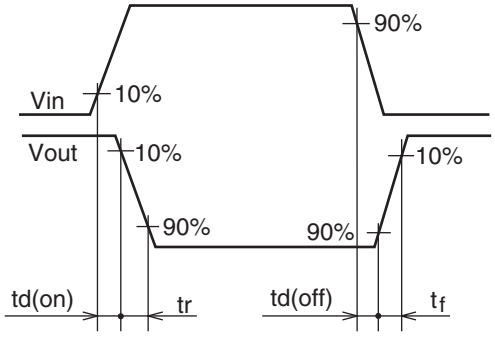
Gate to Source Cutoff Voltage vs. Temperature

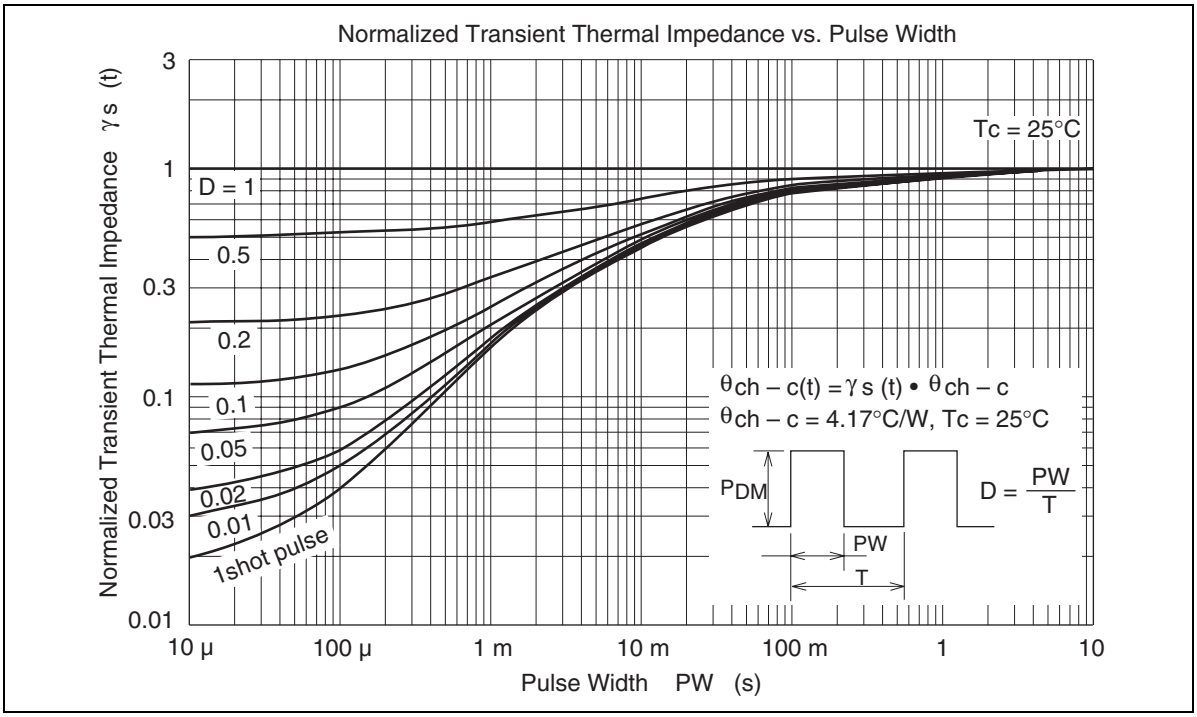


Switching Time Test Circuit



Waveform



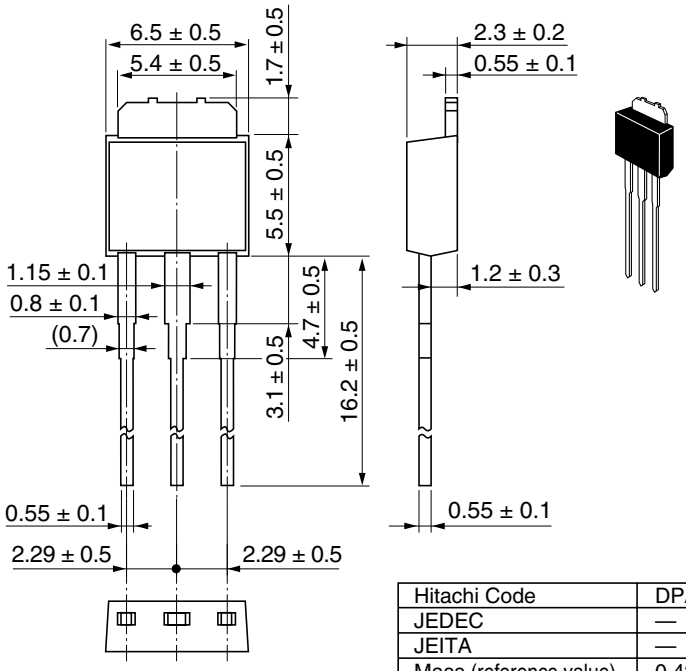

Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 4.17°C/W, Tc = 25°C
PDM
D = PW / T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Package Dimensions

• H5N2504DL

As of January, 2002

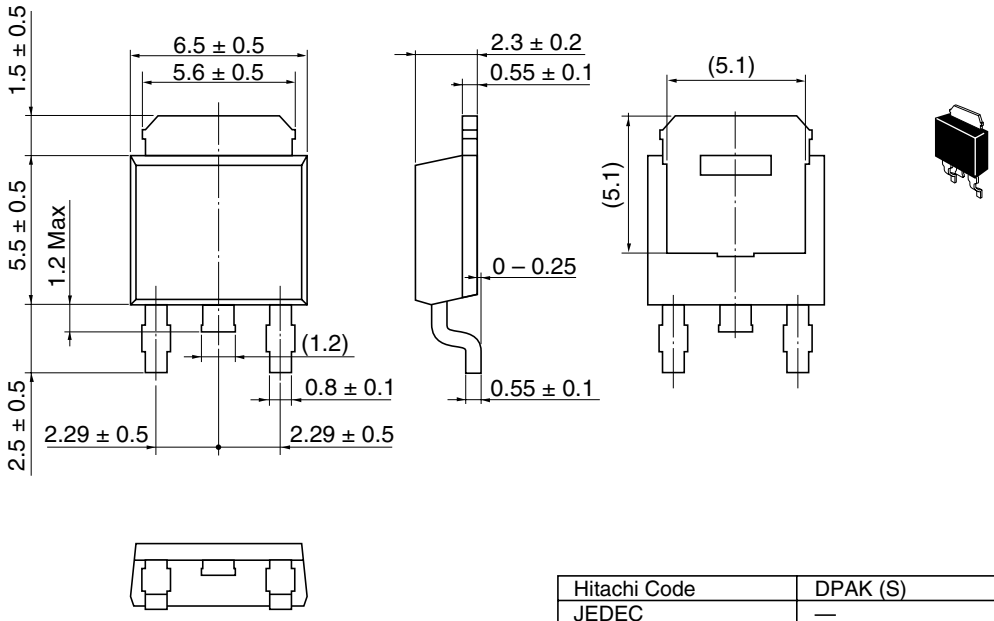
Unit: mm



Hitachi Code	DPAK (L)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	0.42 g

• H5N2504DS

Unit: mm



Hitachi Code	DPAK (S)
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.28 g

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