

Low Voltage Quad Buffer with 5 V Tolerant Inputs and Outputs

74LCX125

Description

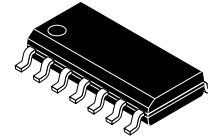
The LCX125 contains four independent non-inverting buffers with 3-STATE outputs. The inputs tolerate Voltages up to 5.5 V Allowing the interface of 5 V Systems to 3 V Systems.

The 74LCX125 is fabricated with an advanced CMOS technology to achieve high Speed operation while Maintaining CMOS Low Power Dissipation.

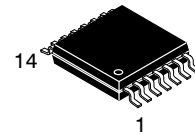
Features

- 5 V Tolerant Inputs and Outputs
- 1.65 V–5.5 V V_{CC} Specifications Provided
- 6.0 ns t_{PD} max. ($V_{CC} = 3.3$ V), 10 μ A I_{CC} max.
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal*
- ± 24 mA Output Drive ($V_{CC} = 3.0$ V)
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD Performance:
 - ◆ Human body model > 2000 V
- Pb-Free DQFN Package
- These are Pb-Free Devices

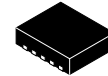
*To ensure the High-Impedance State During Power up or down, OE Should be tied to V_{CC} through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.



SOIC14,
CASE 751EF



TSSOP-14, WB
CASE 948G



QFN14, 3.0X2.5, 0.5P
CASE 510CB

MARKING DIAGRAM



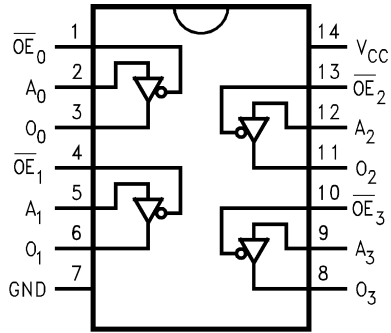
Z = Assembly Plan Code
 XY = Date Code (Year & Week)
 KK = Lot Run Traceability Code
 XXXXXX = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

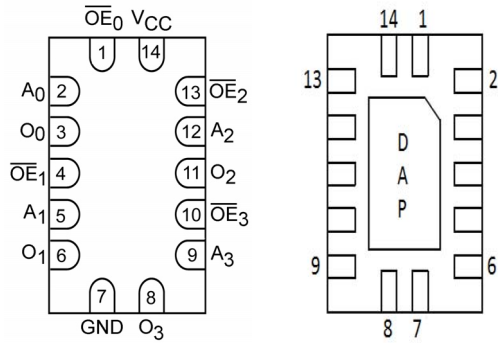
Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP



(Top View)
Figure 1.

Pad Assignments for DQFN



(Top Through View)

(Bottom View)

Figure 3.

IEEE/IEC

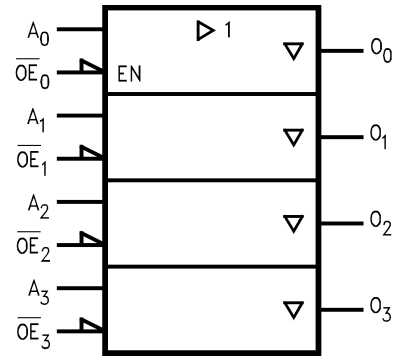


Figure 2. Logic Symbol

Table 1. PIN DESCRIPTION

Pin Names	Description
A_n	Inputs
$\overline{OE}_n$	Output Enable Inputs
O_n	Outputs
DAP	No Connect

NOTE: Die Attach Pad (DIE)

TRUTH TABLE

Inputs		Outputs
$\overline{OE}_n$	A_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = HIGH Voltage Level
Z = HIGH Impedance
X = Immaterial

74LCX125

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	–0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)	–0.5 to +6.5	V
V_O	DC Output Voltage (Note 1) Active-Mode (High or Low State) Tri-State Mode Power-Down Mode ($V_{CC} = 0$ V)	–0.5 to $V_{CC} + 0.5$ –0.5 to +6.5 –0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_I < GND$	–50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	–50	mA
I_O	DC Output Source/Sink Current	±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 1) SOIC-14 QFN14 TSSOP-14	116 130 150	°C/W
P_D	Power Dissipation in Still Air at 125°C SOIC-14 QFN14 TSSOP-14	1077 962 833	mW
MSL	Moisture Sensitivity	Level 1	–
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51–7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	3.3 3.3	5.5 5.5	V
V_I	Digital Input Voltage	0	–	5.5	V
V_O	Output Voltage Active Mode (High or Low State) Tri-State Mode Power Down Mode ($V_{CC} = 0$ V)	0 0 0	– – –	V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature	–40	–	+125	°C
t_r, t_f	Input Rise or Fall Rate $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V V_I from 0.8 V to 2.0 V, $V_{CC} = 3.0$ V $V_{CC} = 4.5$ V to 5.5 V	0 0 0 0	– – – –	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40 °C to +85 °C		T _A = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V _{CC}	–	0.65 x V _{CC}	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V _{CC}	–	0.70 x V _{CC}	–	
V _{IL}	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V _{CC}	–	0.35 x V _{CC}	V
			2.3 – 2.7	–	0.7	–	0.7	
			3.0 – 3.6	–	0.8	–	0.8	
			4.5 – 5.5	–	0.30 x V _{CC}	–	0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	V _{CC} – 0.1	–	V _{CC} – 0.1	–	V
		I _{OH} = -100 µA	1.65	1.29	–	1.29	–	
		I _{OH} = -4 mA	2.3	1.8	–	1.8	–	
		I _{OH} = -8 mA	2.7	2.2	–	2.2	–	
		I _{OH} = -12 mA	3.0	2.4	–	2.4	–	
		I _{OH} = -16 mA	3.0	2.2	–	2.2	–	
		I _{OH} = -32 mA	4.5	3.7	–	3.7	–	
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	–	0.1	–	0.1	V
		I _{OL} = 100 µA	1.65	–	0.24	–	0.24	
		I _{OL} = 4 mA	2.3	–	0.3	–	0.3	
		I _{OL} = 8 mA	2.7	–	0.4	–	0.4	
		I _{OL} = 12 mA	3.0	–	0.4	–	0.4	
		I _{OL} = 16 mA	3.0	–	0.55	–	0.55	
		I _{OL} = 32 mA	4.5	–	0.6	–	0.6	
I _{OZ}	3-State Output Leakage Current	V _I = V _{IH} or V _{IL} , V _O = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	µA
I _I	Input Leakage Current	V _I = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	µA
I _{OFF}	Power Off Leakage Current	V _I = 5.5 V or V _O = 5.5 V	0	–	10	–	10	µA
I _{CC}	Quiescent Supply Current	V _I = 5.5 V or GND	3.6	–	10	–	10	µA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6 V	2.3 to 3.6	–	500	–	500	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V _{CC} (V)	T _A = -40 °C to +85 °C		T _A = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	See Figures 4 and 5	1.65 to 1.95	–	11.0	–	11.0	ns
			2.3 to 2.7	–	7.2	–	7.2	
			2.7	–	6.5	–	6.5	
			3.0 to 3.6	–	6.0	–	6.0	
			4.5 to 5.5	–	4.7	–	4.7	

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V _{CC} (V)	T _A = -40 °C to +85 °C		T _A = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
t _{pZH} , t _{pZL}	Output Enable Time	See Figures 4 and 5	1.65 to 1.95	–	11.3	–	11.3	ns
			2.3 to 2.7	–	9.1	–	9.1	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	6.0	–	6.0	
t _{pHZ} , t _{pLZ}	Output Disable Time	See Figures 4 and 5	1.65 to 1.95	–	9.0	–	9.0	ns
			2.3 to 2.7	–	7.2	–	7.2	
			2.7	–	7.0	–	7.0	
			3.0 to 3.6	–	6.0	–	6.0	
			4.5 to 5.5	–	5.0	–	5.0	
t _{OSHL} , t _{OSLH}	Output to Output Skew		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

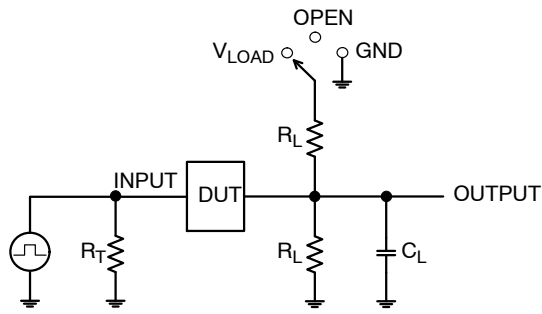
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Test Conditions	T _A = 25 °C	Unit
				Typ	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	0.8	V
		2.5	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	0.6	
V _{OLV}	Quiet Output Dynamic Peak V _{OL}	3.3	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	–0.8	V
		2.5	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	–0.6	

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0 V or V _{CC}	7.0	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8.0	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC} , f = 10 MHz	25.0	pF

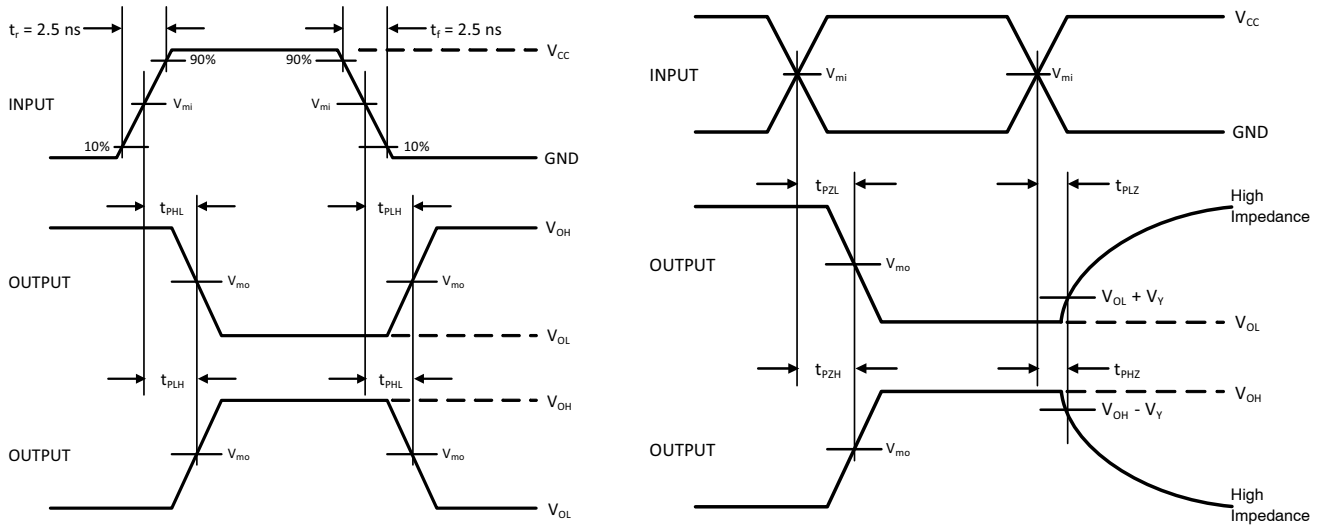
74LCX125



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

Figure 4. Test Circuit



V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_m, V	V_Y, V
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	0.3

Figure 5. Switching Waveforms

74LCX125

SCHEMATIC DIAGRAM (GENERIC FOR LCX FAMILY)

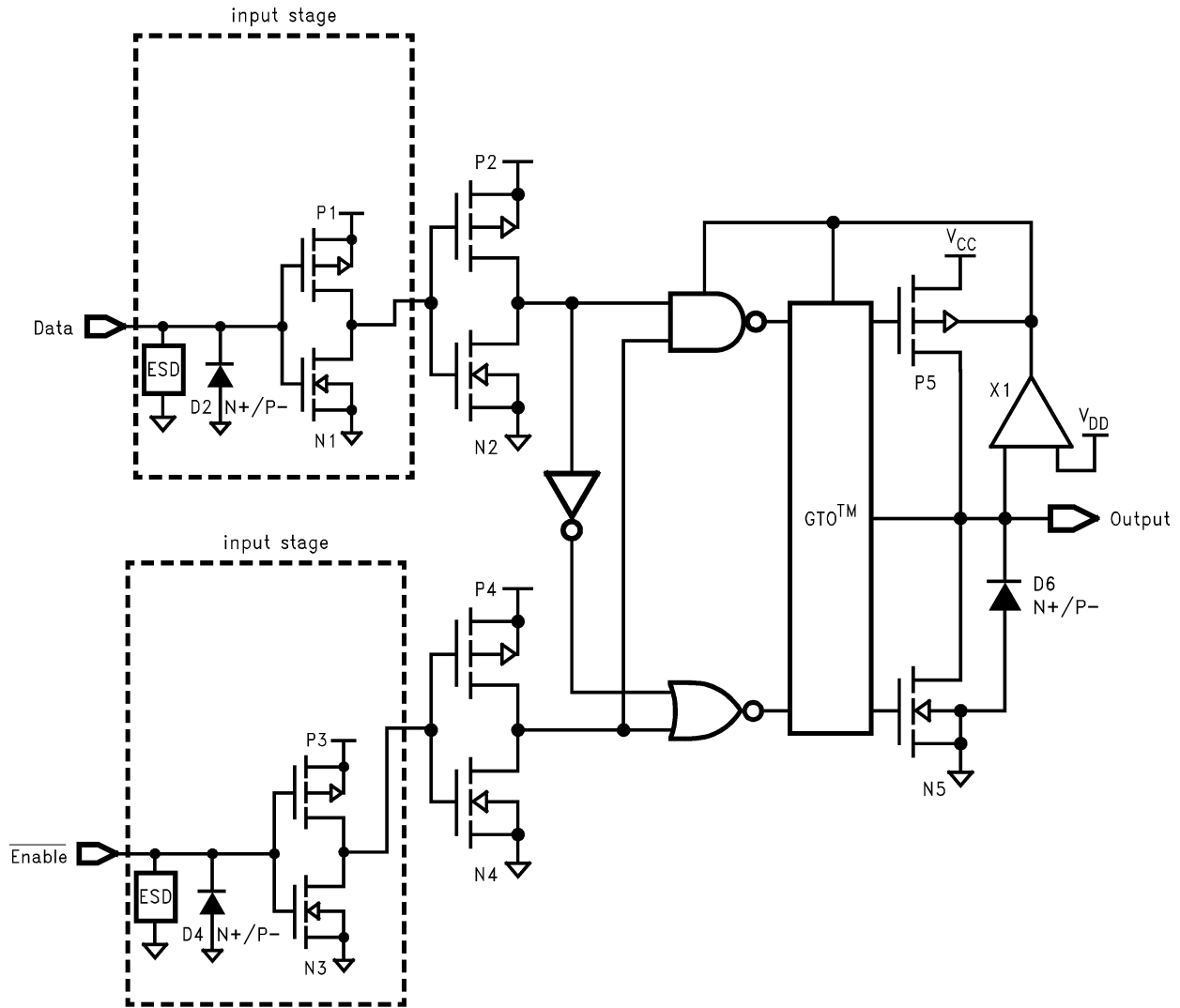


Figure 6. Schematic Diagram

ORDERING INFORMATION

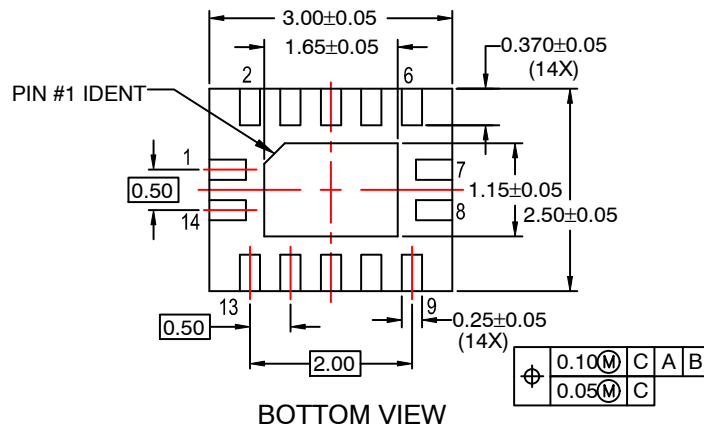
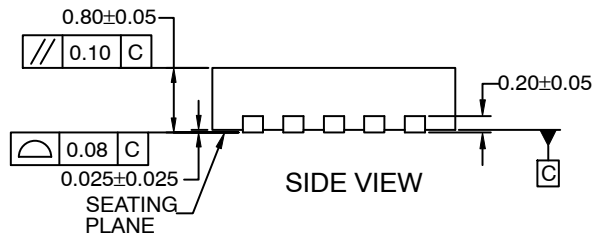
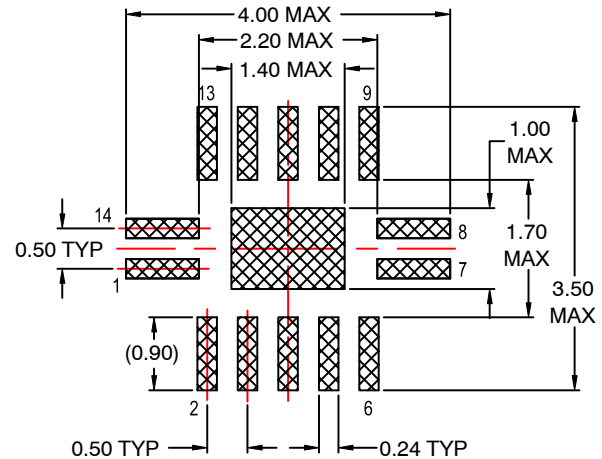
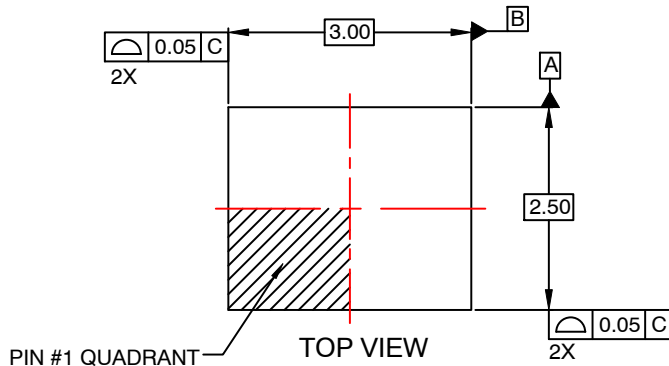
Product Number	Package	Shipping [†]
74LCX125MTCX	TSSOP-14 WB (Pb-Free/Halide Free)	2500 / Tape and Reel
74LCX125BQX (Note 5)	QFN-14 (Pb-Free/Halide Free)	3000 / Tape and Reel
74LCX125MTC	TSSOP-14 WB (Pb-Free/Halide Free)	2350 Units / Tube

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

5. DQFN package available in Tape and Reel only.

QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

DATE 31 AUG 2016



NOTES:

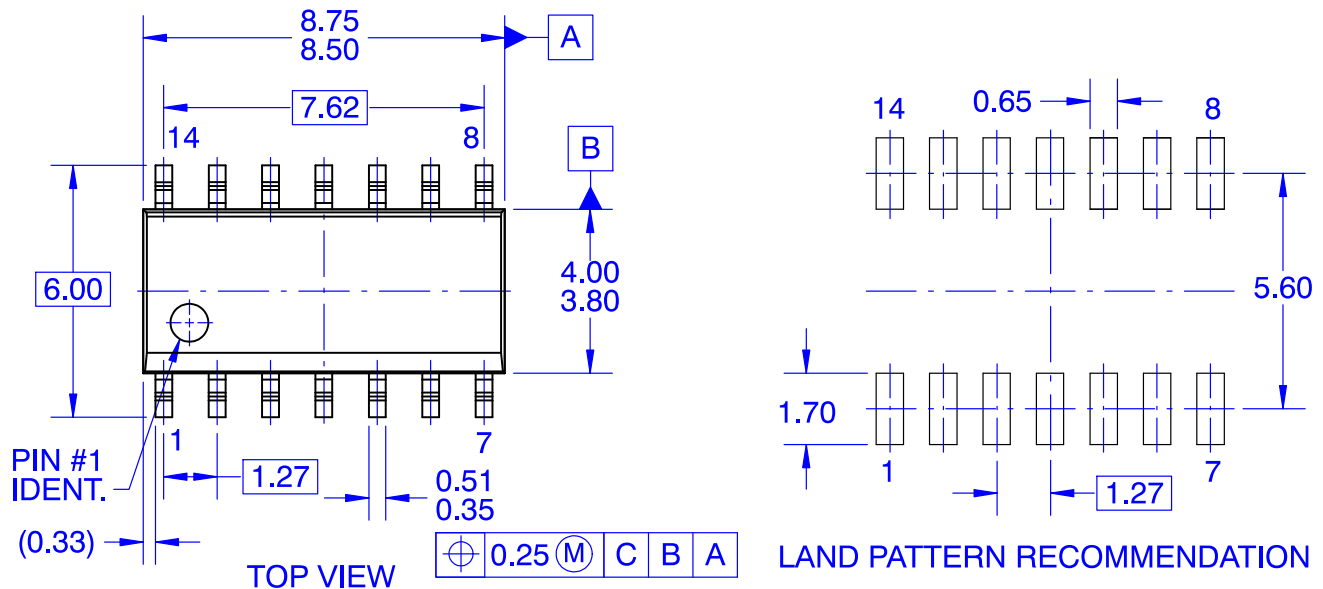
- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
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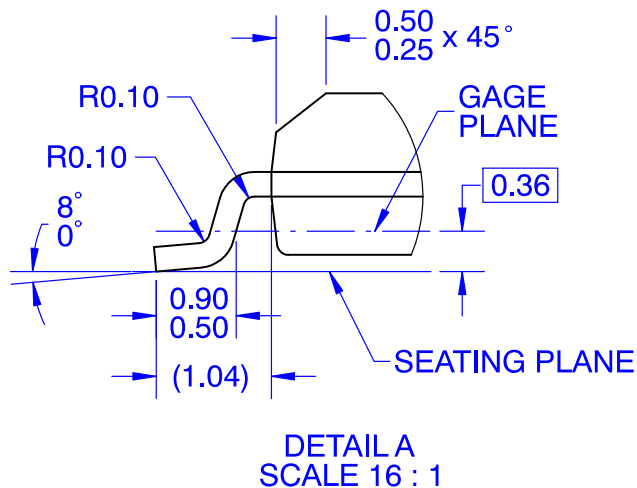
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



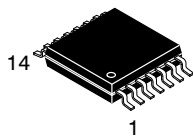
NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



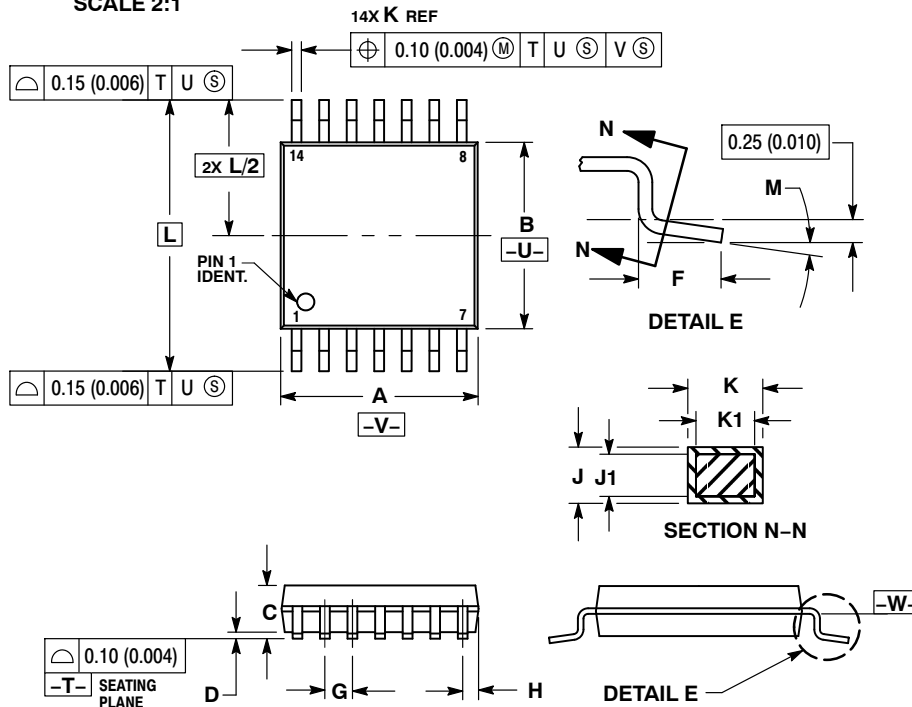
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TSSOP-14 WB
CASE 948G
ISSUE C

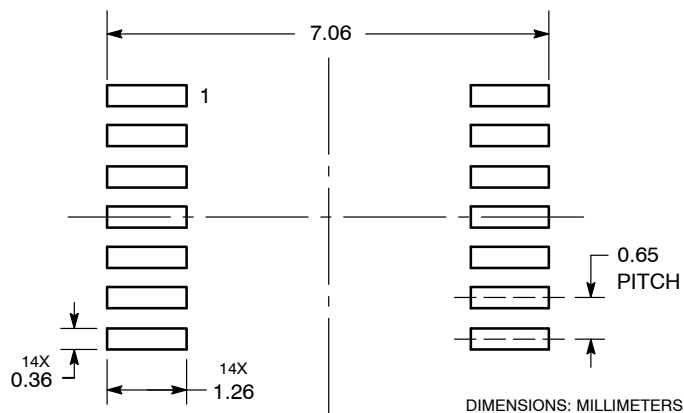
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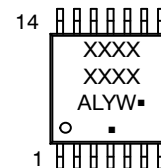

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION: TSSOP-14 WB

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