RFD14N05, RFD14N05SM, RFP14N05

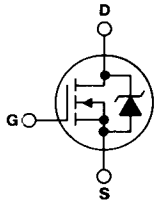
File Number **2268**

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

14 A, 50 V
$r_{ds(on)} = 0.1\Omega$

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



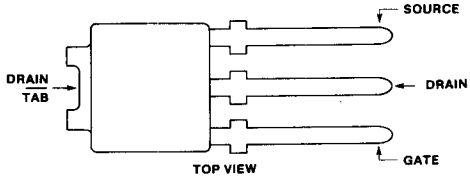
92CS-42658

N-CHANNEL ENHANCEMENT MODE

The RFD14N05, RFD14N05SM, and RFP14N05 n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

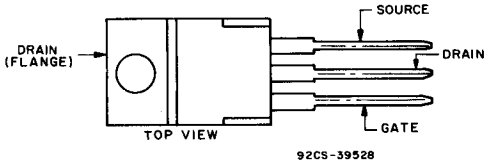
The RFD14N05 is supplied in the JEDEC TO-251 plastic package, the RFD14N05SM in the JEDEC TO-252 plastic package and the RFP14N05 in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



JEDEC TO-251AA

TERMINAL DESIGNATION



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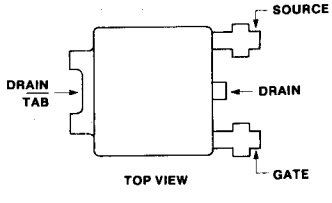
JEDEC TO-220AB



JEDEC TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

DRAIN-SOURCE VOLTAGE, V_{DSS}	50 V
DRAIN-GATE VOLTAGE, R_{GS} = 1 MΩ, V_{DGR}	50 V
GATE-SOURCE VOLTAGE, V_{GS}	±20 V
DRAIN CURRENT:	
RMS Continuous, I_D	14 A
Pulsed, I_{DM}	35 A
SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}*	100 mj
AVALANCE CURRENT, I_{AS}	14 A
POWER DISSIPATION, P_T:	
At T_C = 25°C	40 W
Derate above T_C = 25°C	0.32 W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C

*V_{DD} = 10 volts, starting T_j = 25°C, L = 820 μHy I_{peak} = 14A, see figures 12 and 13.

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 10 V		—	0.1	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A I_{g1} = I_{g2} = 0.2 A V_{GS} (clamp) + 10 V, − 0.6 V R_L = 3.57 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	
Rise Time	t_r			—	26 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	45 (typ.)	
Fall Time	t_f			—	17 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{DD} = 40 V	V_{GS} = 0-20 V	—	40	nC
Gate Charge at 10 V	$Q_g(10)$	I_D = 14 A	V_{GS} = 0-10 V	—	25	
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-2 V	—	1.5	
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, R_L = 0.2 μH R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A V_{GS} (clamp) + 10 V, −0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	
		TO-220		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 100 A/μs	—	125	ns

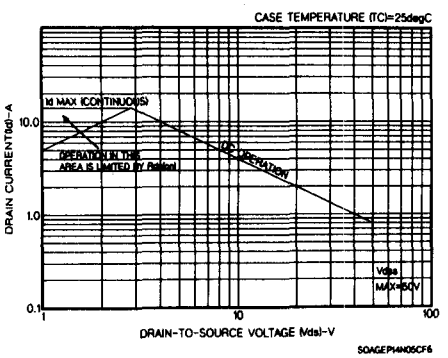


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

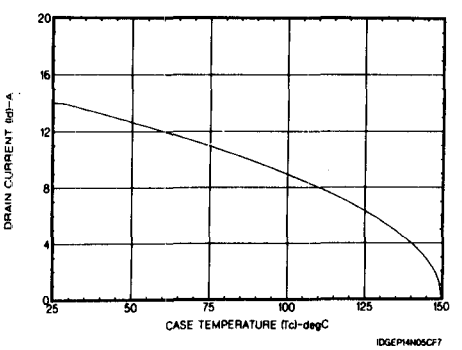


Fig. 2 - Maximum continuous drain current vs. temperature.

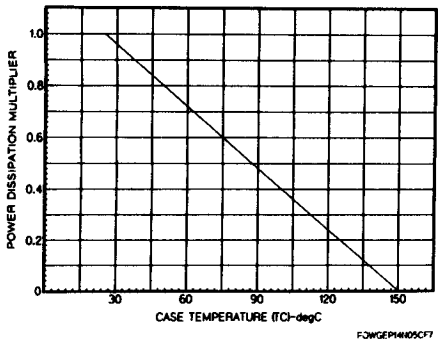


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

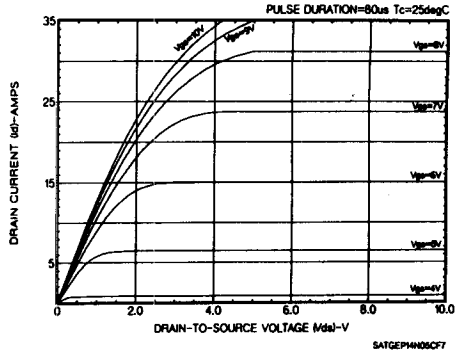


Fig. 4 - Typical saturation characteristics.

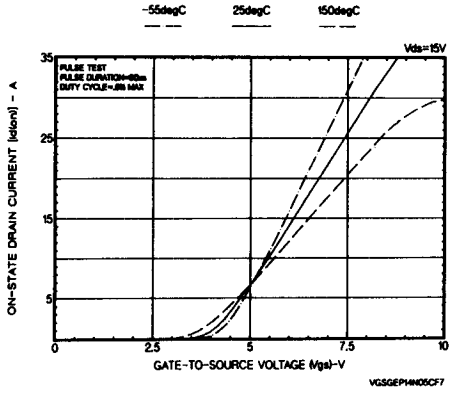


Fig. 5 - Typical transfer characteristics.

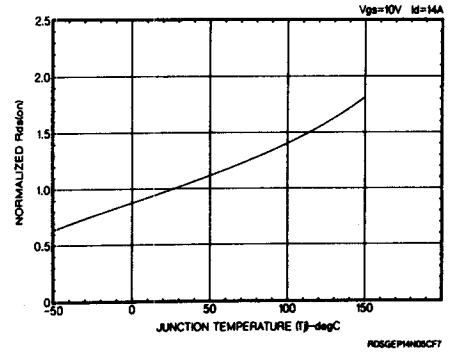


Fig. 6 - Normalized $R_{ds}(on)$ vs. junction temperature.

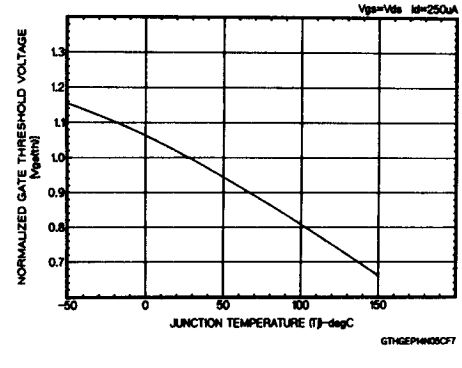


Fig. 7 - Normalized gate threshold voltage.

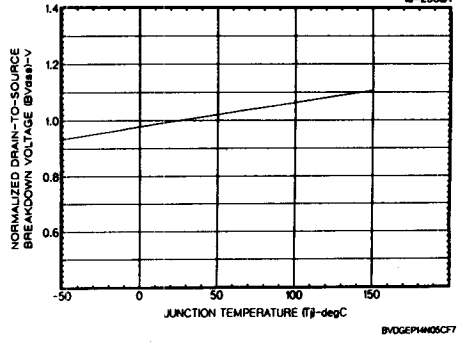


Fig. 8 - Normalized drain source breakdown voltage vs. temperature.

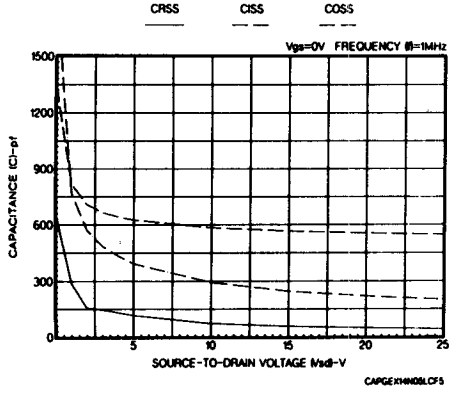


Fig. 9 - Typical capacitance vs. voltage.

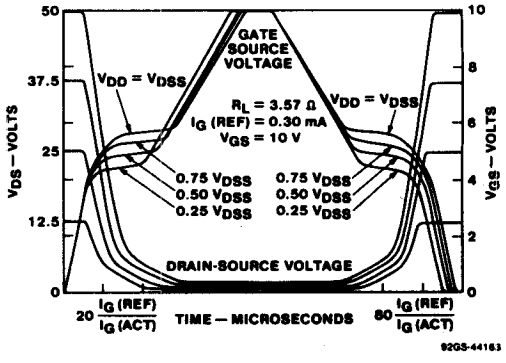


Fig. 10 - Normalized switching waveforms for constant gate-current. (Refer to RCA application notes AN-7254 and AN-7260.)

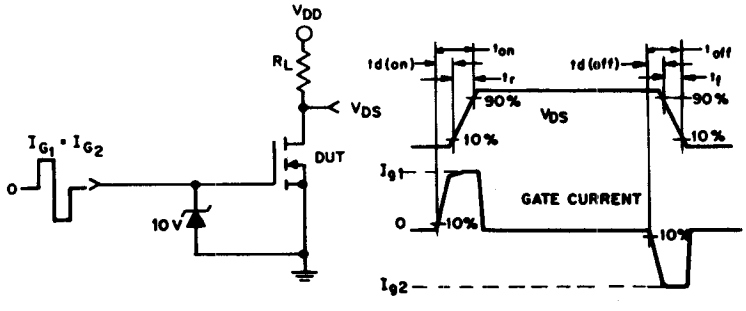


Fig. 11 - Resistive switching.

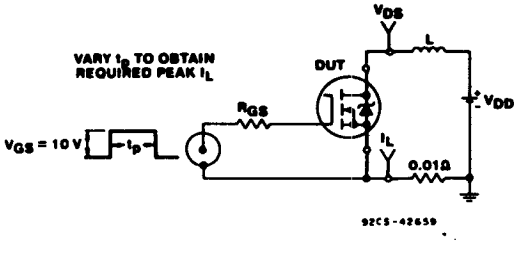


Fig. 12 - Unclamped energy test circuit.

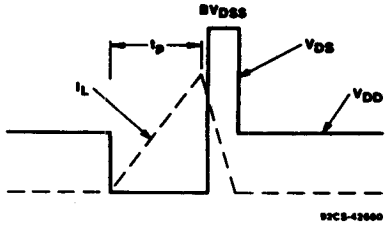


Fig. 13 - Unclamped energy waveforms.