

LM837 Low Noise Quad Operational Amplifier

Check for Samples: [LM837](#)

FEATURES

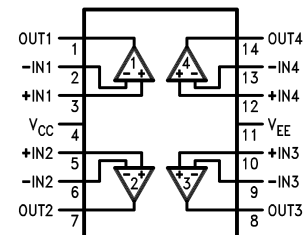
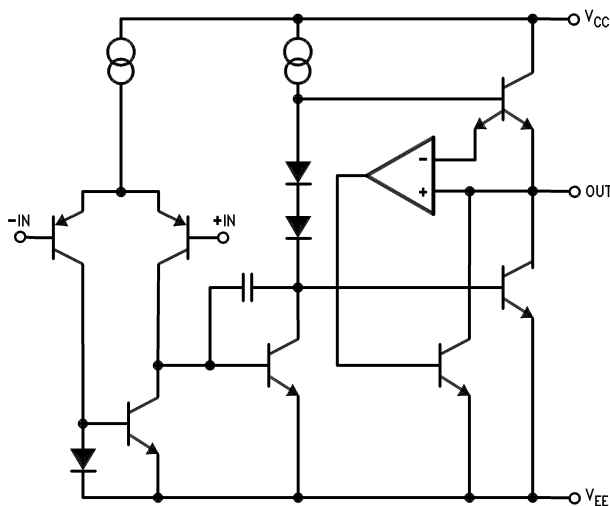
- **High Slew Rate** 10 V/ μ s (typ); 8 V/ μ s (min)
- **Wide Gain Bandwidth Product** 25 MHz (typ); 15 MHz (min)
- **Power Bandwidth** 200 kHz (typ)
- **High Output Current** ± 40 mA
- **Excellent Output Drive Performance** $>600\Omega$
- **Low Input Noise Voltage** 4.5 nV/ $\sqrt{\text{Hz}}$
- **Low Total Harmonic Distortion** 0.0015%
- **Low Offset Voltage** 0.3 mV

DESCRIPTION

The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600 Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and can therefore be used to upgrade existing systems with little or no change.

Schematic and Connection Diagrams



**Figure 1. PDIP Package
Top View
See Package Number
D0014A or NFF0014A**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage, V_{CC}/V_{EE}	±18V
Differential Input Voltage, $V_{ID}^{(3)}$	±30V
Common Mode Input Voltage, $V_{IC}^{(3)}$	±15V
Power Dissipation, $P_D^{(4)}$	1.2W (N) 830 mW (M)
Operating Temperature Range, T_{OPR}	–40°C to +85°C
Storage Temperature Range, T_{STG}	–60°C to +150°C
Soldering Information PDIP Package Soldering (10 seconds)	260°C
SOIC Package Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD rating to be determined.	
See http://www.ti.com for other methods of soldering surface mount devices.	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Unless otherwise specified the absolute maximum input voltage is equal to the power supply voltage.
- (4) For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM837N, 90°C/W; LM837M, 150°C/W.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Large Signal Voltage Gain	$R_L = 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{V}$	90	110		dB
V_{OM}	Output Voltage Swing	$R_L = 2\text{ k}\Omega$	±12	±13.5		V
		$R_L = 600\Omega$	±10	±12.5		V
V_{CM}	Common Mode Input Voltage		±12	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{IN} = \pm 12\text{V}$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 15 \sim 5$, $-15 \sim -5$	80	100		dB
I_S	Power Supply Current	$R_L = \infty$, Four Amps		10	15	mA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

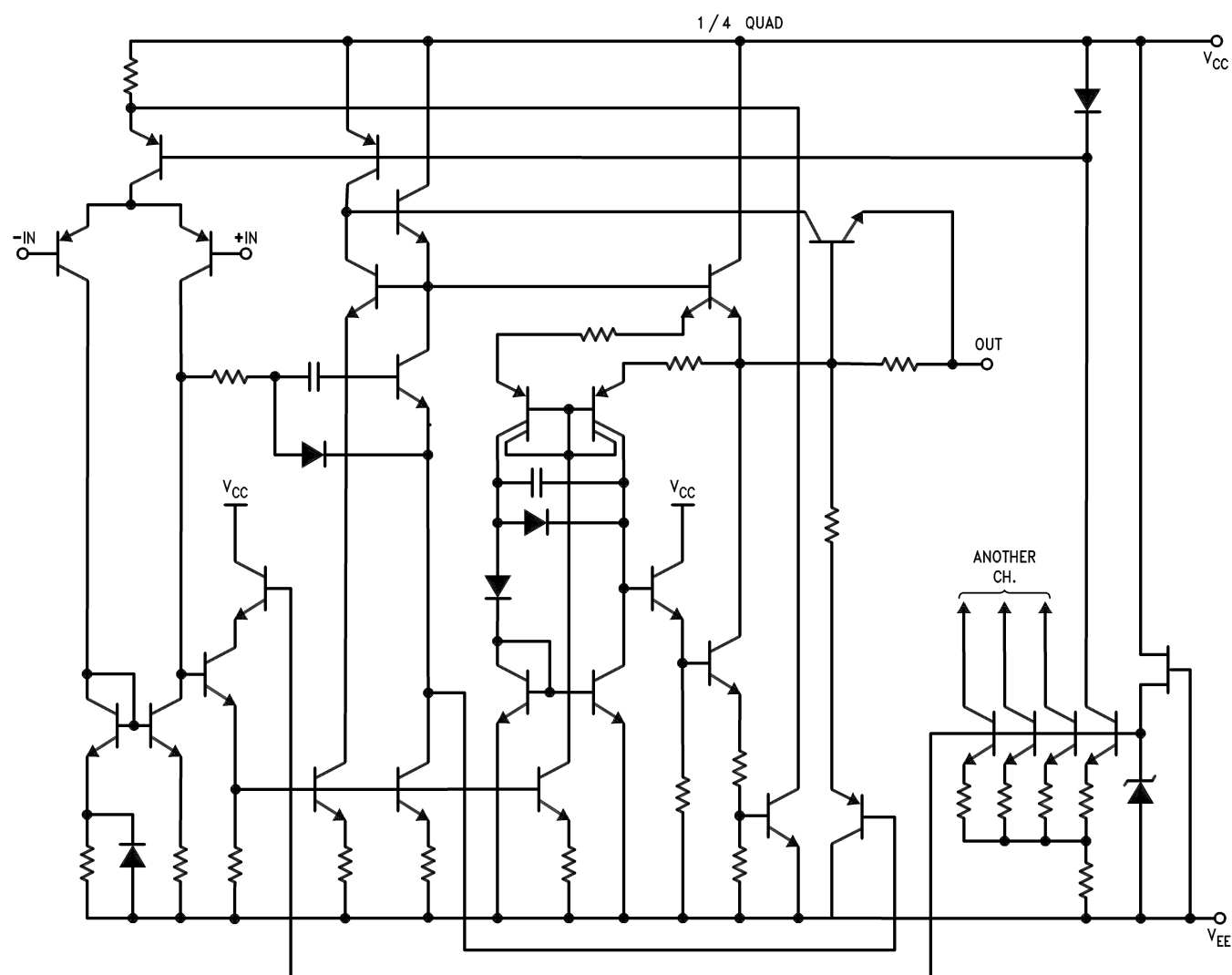
Symbol	Parameter	Condition	Min	Typ	Max	Units
SR	Slew Rate	$R_L = 600\Omega$	8	10		V/μs
GBW	Gain Bandwidth Product	$f = 100\text{ kHz}$, $R_L = 600\Omega$	15	25		MHz

DESIGN ELECTRICAL CHARACTERISTICS

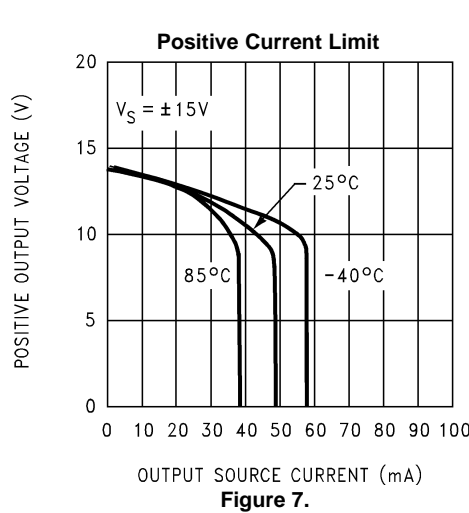
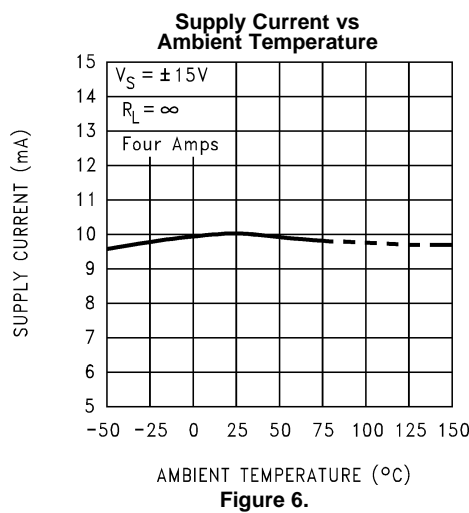
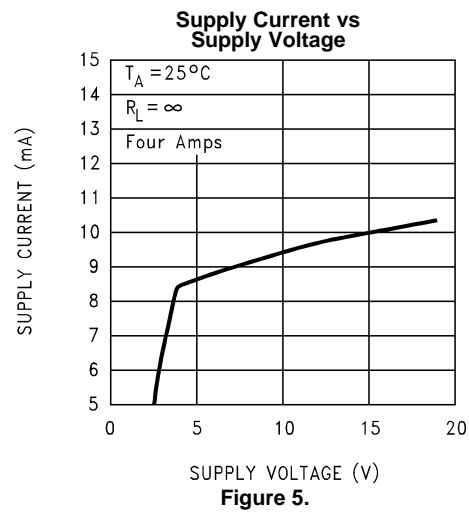
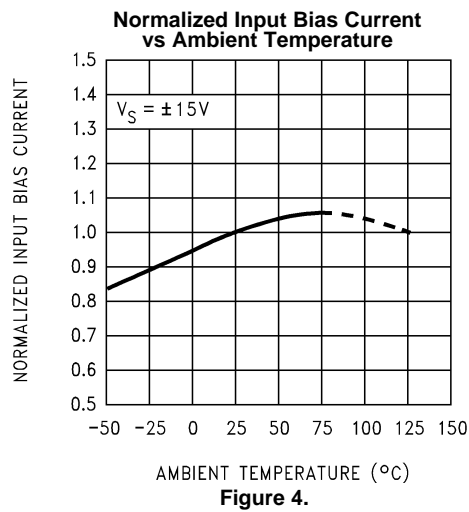
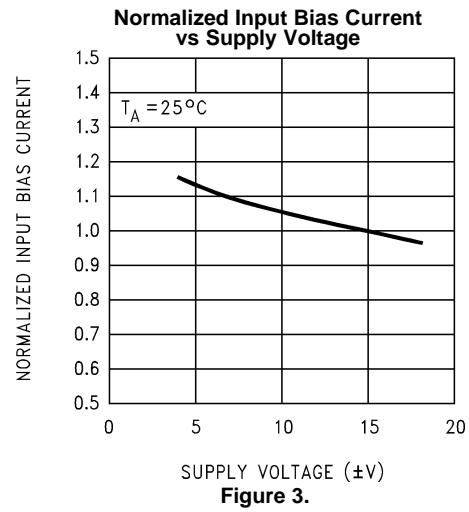
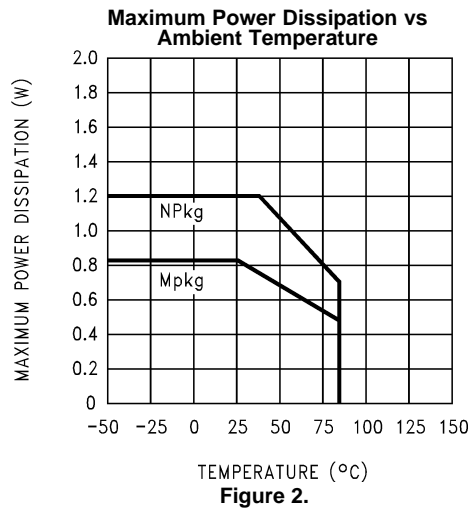
 $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ ⁽¹⁾

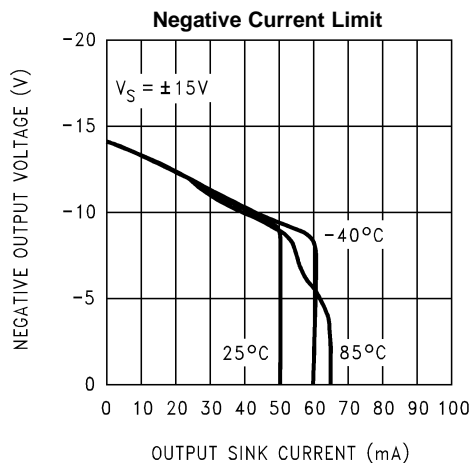
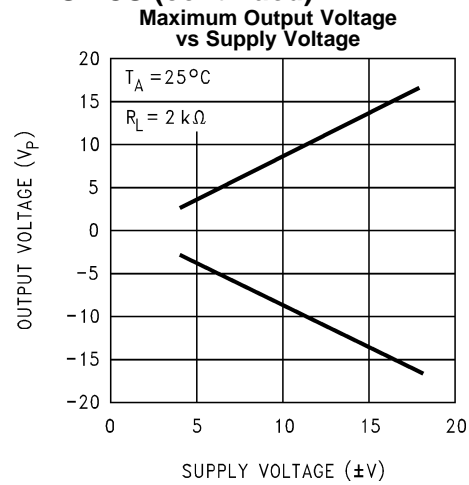
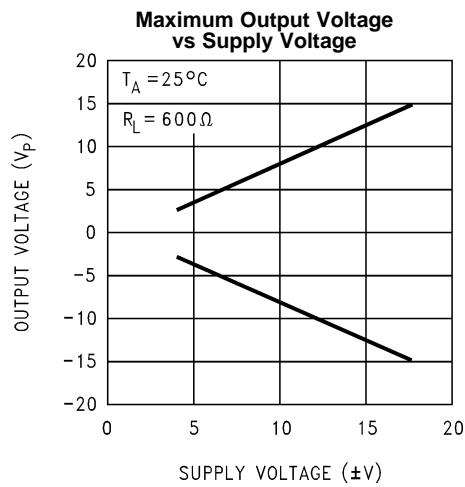
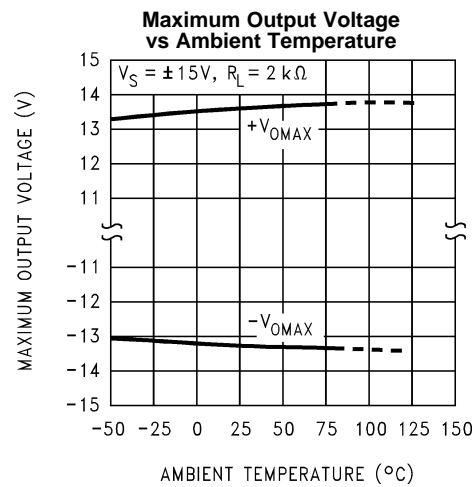
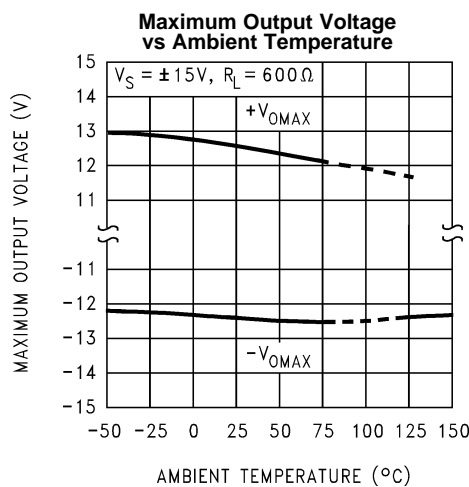
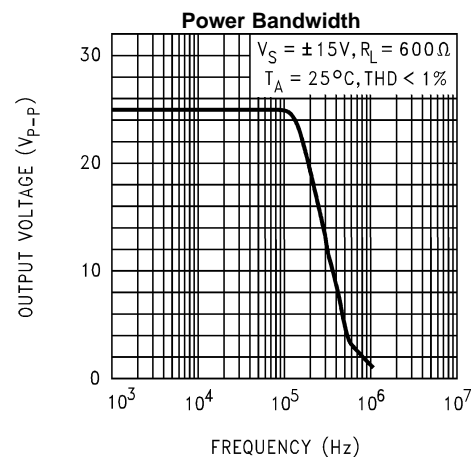
Symbol	Parameter	Condition	Min	Typ	Max	Units
PBW	Power Bandwidth	$V_O = 25\text{ V}_{P-P}$, $R_L = 600\Omega$, THD < 1%		200		kHz
e_{n1}	Equivalent Input Noise Voltage	JIS A, $R_S = 100\Omega$		0.5		μV
e_{n2}	Equivalent Input Noise Voltage	$f = 1\text{ kHz}$		4.5		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Equivalent Input Noise Current	$f = 1\text{ kHz}$		0.7		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$A_V = 1$, $V_{OUT} = 3\text{ V}_{rms}$, $f = 20 \sim 20\text{ kHz}$, $R_L = 600\Omega$		0.0015		%
f_U	Zero Cross Frequency	Open Loop		12		MHz
Φ_m	Phase Margin	Open Loop		45		deg
	Input-Referred Crosstalk	$f = 20 \sim 20\text{ kHz}$		-120		dB
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage			2		$\mu\text{V}/^\circ\text{C}$

(1) The following parameters are not tested or ensured.

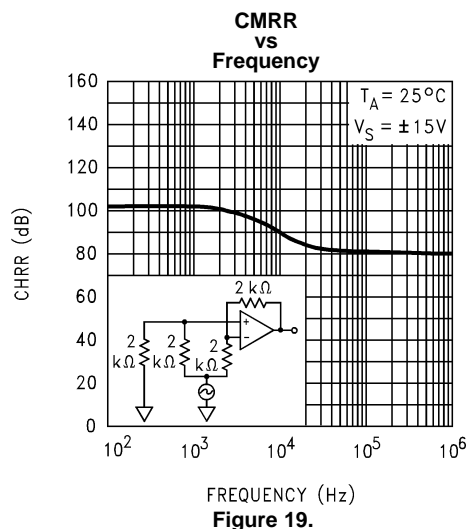
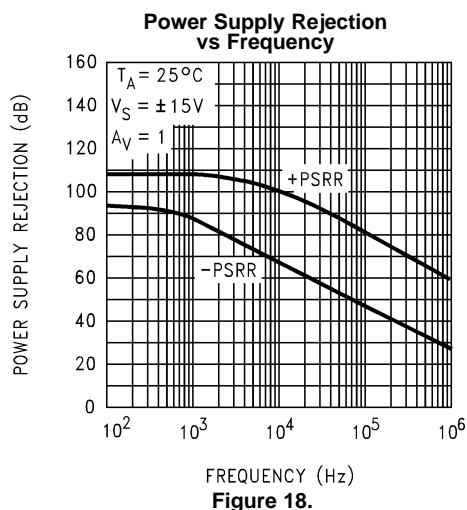
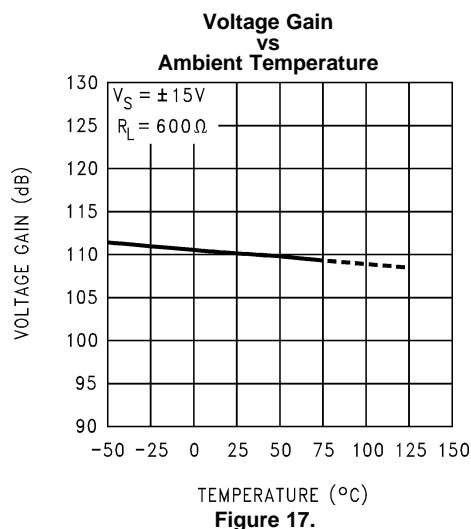
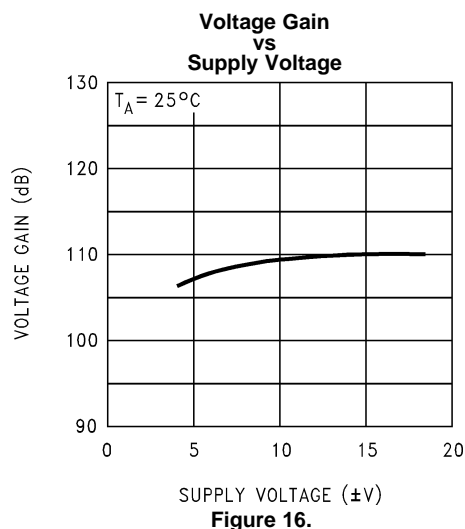
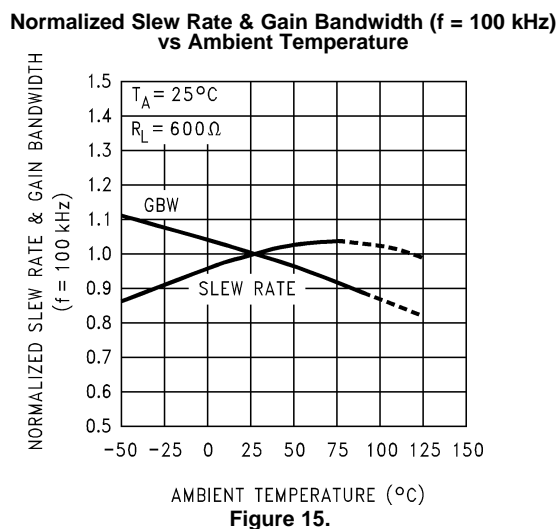
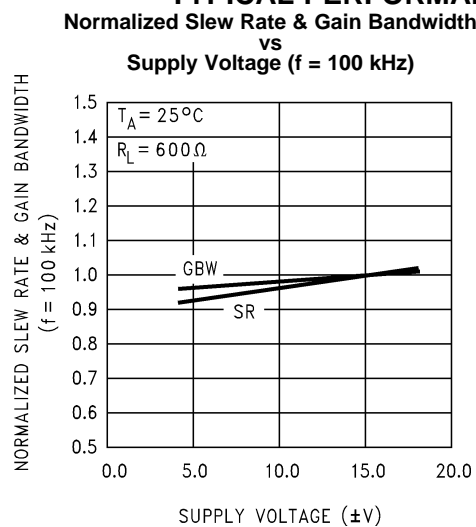
DETAILED SCHEMATIC

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (continued)**Figure 8.****Figure 9.****Figure 10.****Figure 11.****Figure 12.****Figure 13.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

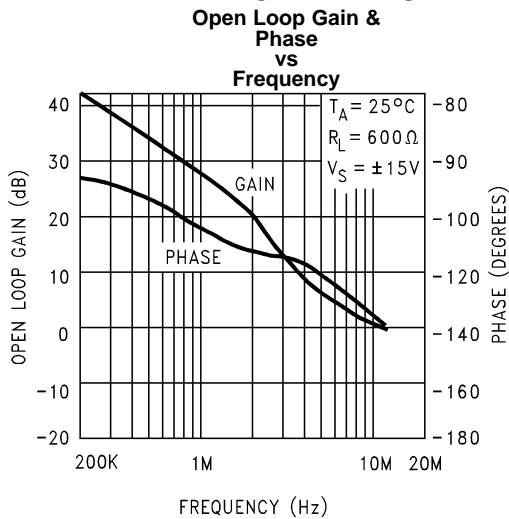


Figure 20.

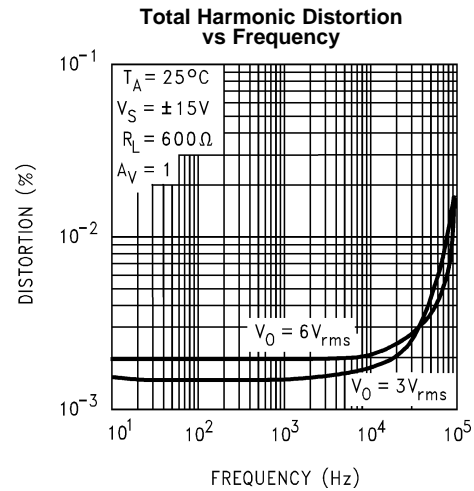


Figure 21.

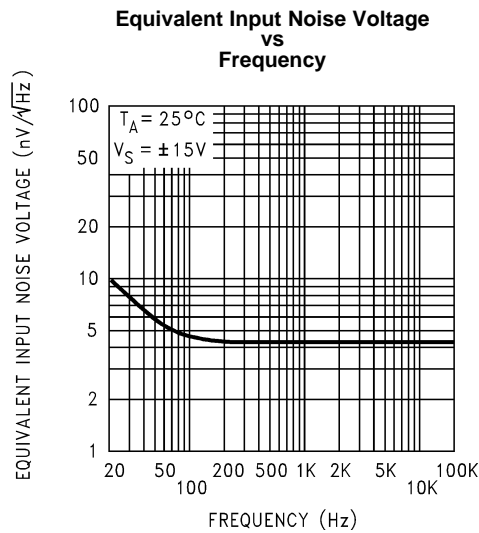


Figure 22.

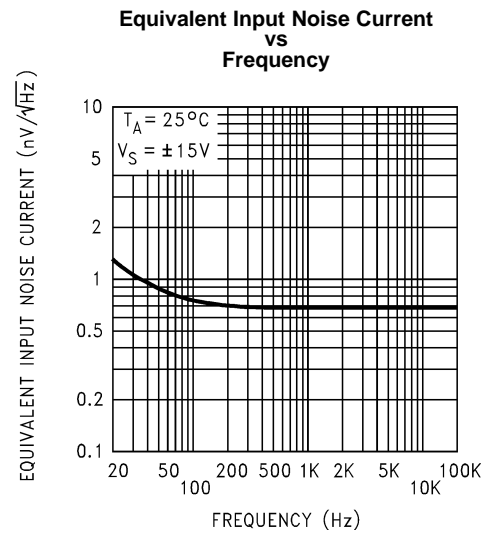


Figure 23.

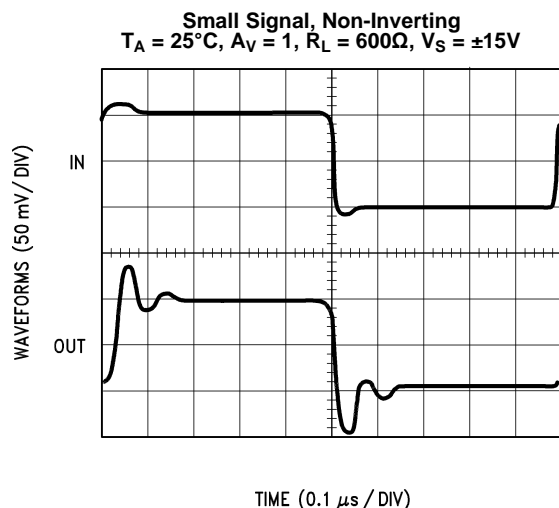


Figure 24.

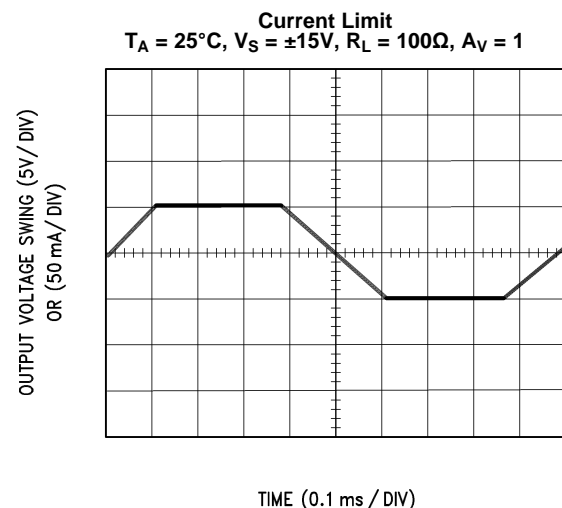


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

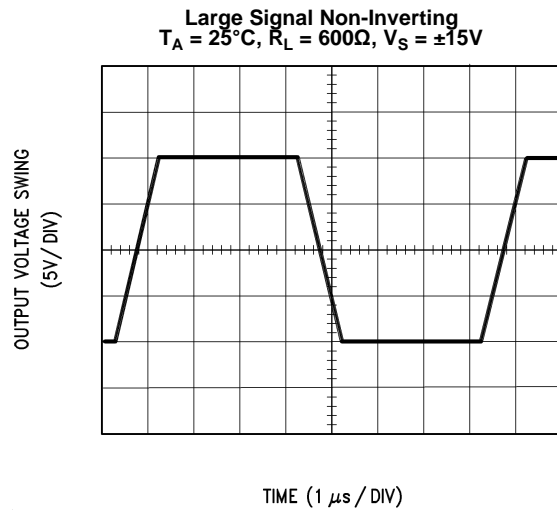


Figure 26.

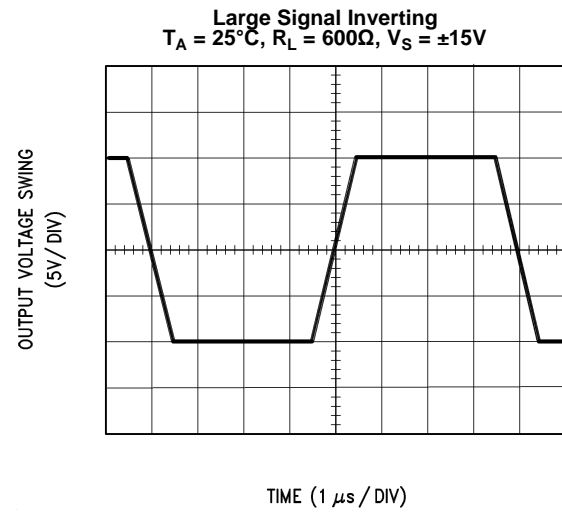


Figure 27.

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C

Page

- Changed layout of National Data Sheet to TI format [5](#)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM837MX/NOPB	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM837M
LM837MX/NOPB.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM837M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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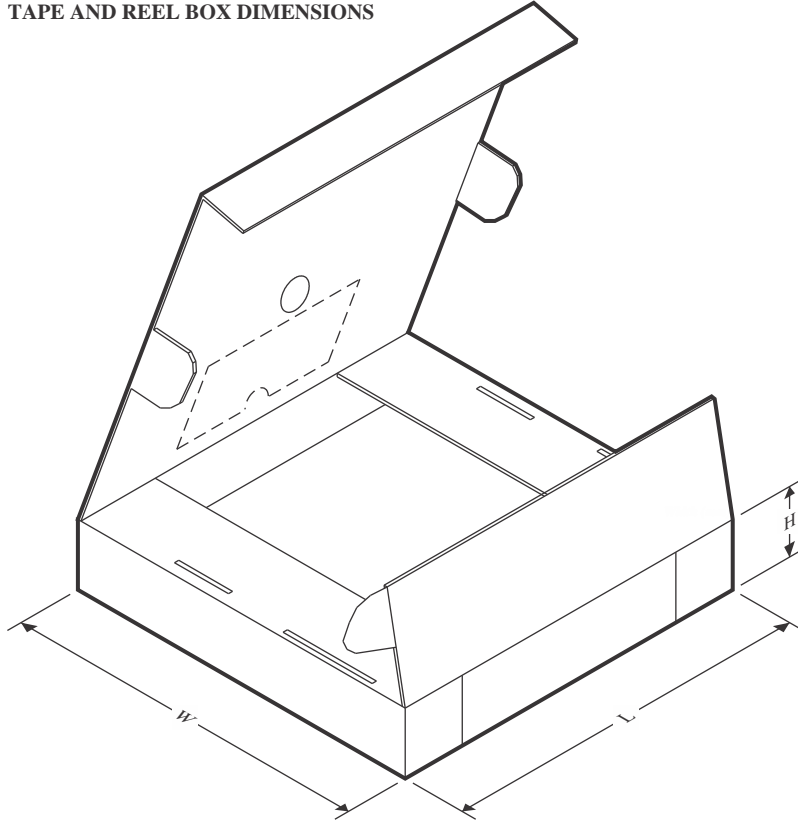
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM837MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

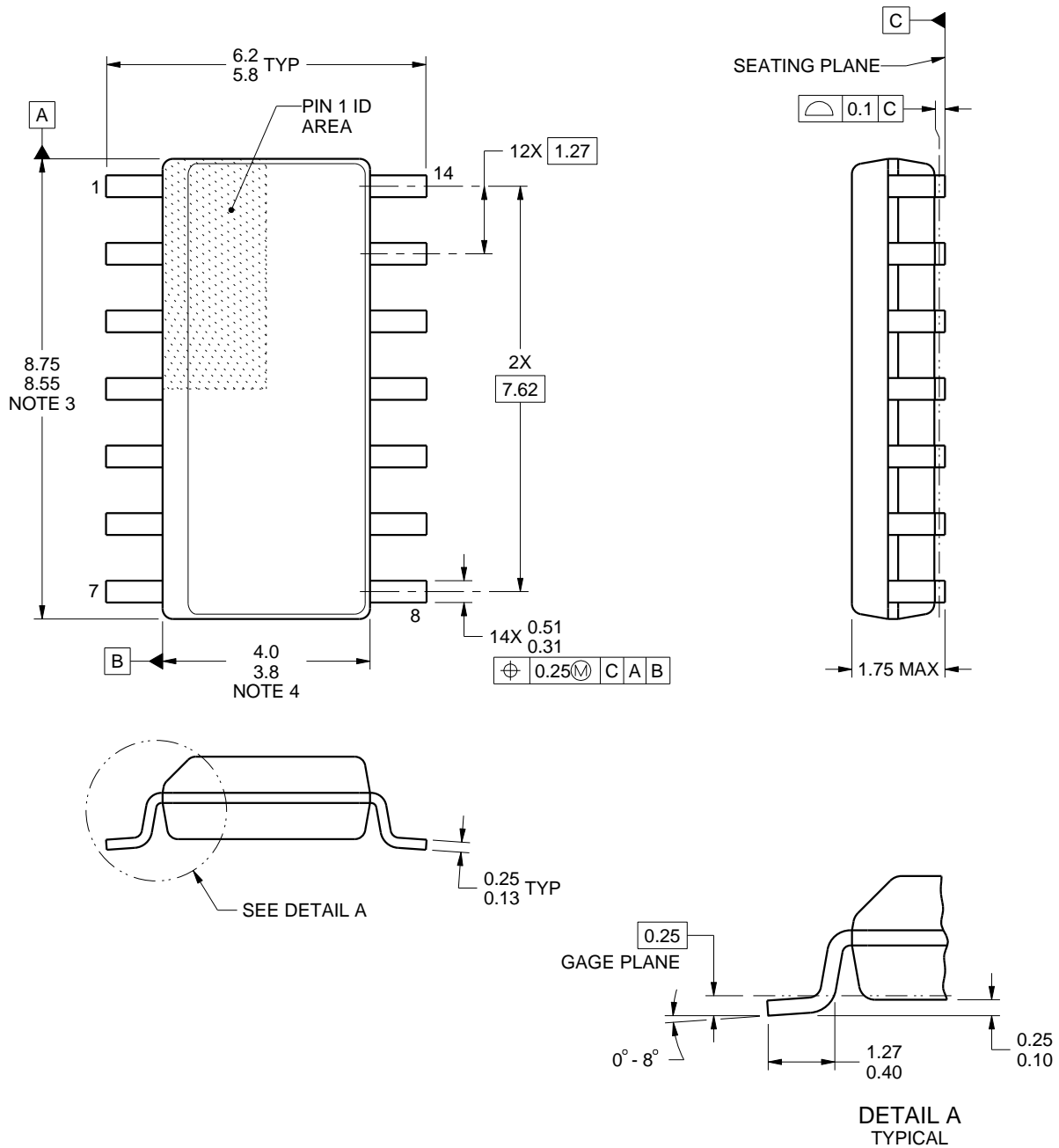
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM837MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

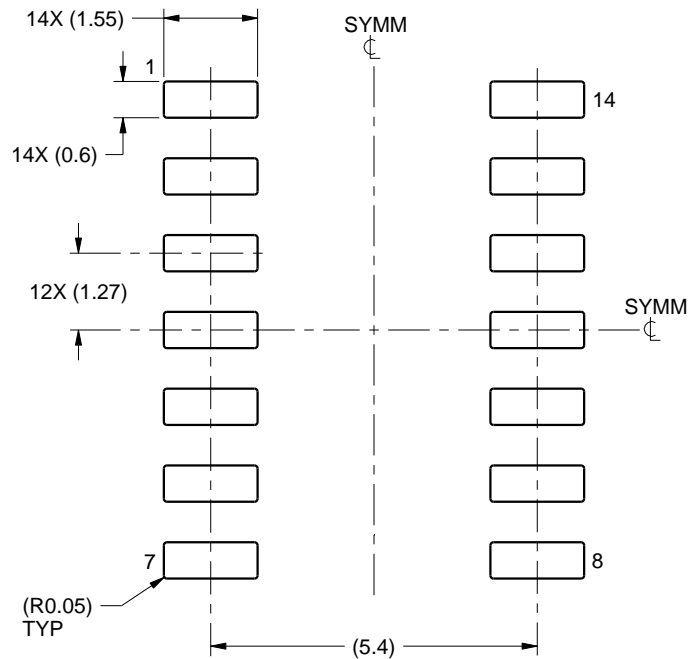
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

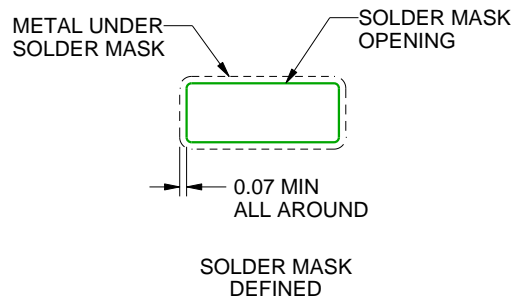
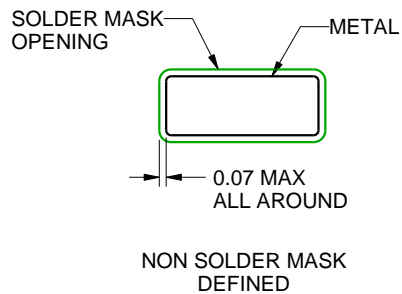
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

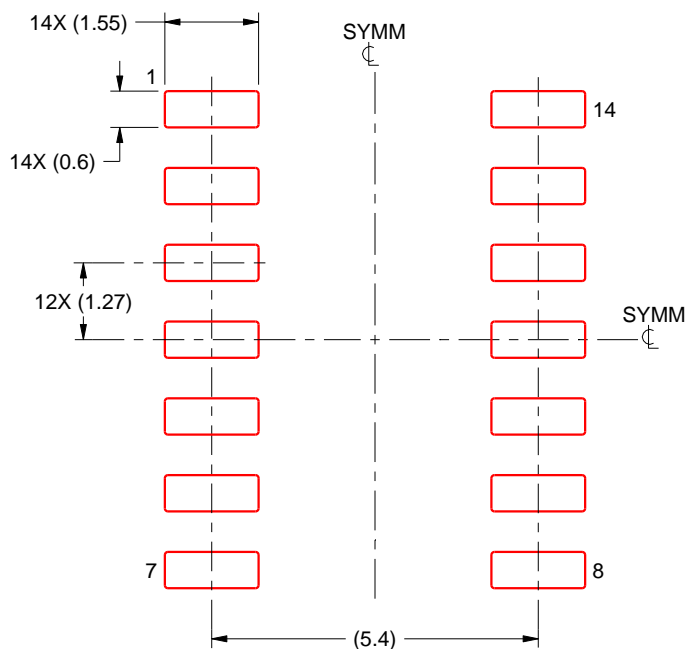
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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