

HAT2173H

Silicon N Channel Power MOS FET Power Switching

REJ03G0030-0100Z

Rev.1.00

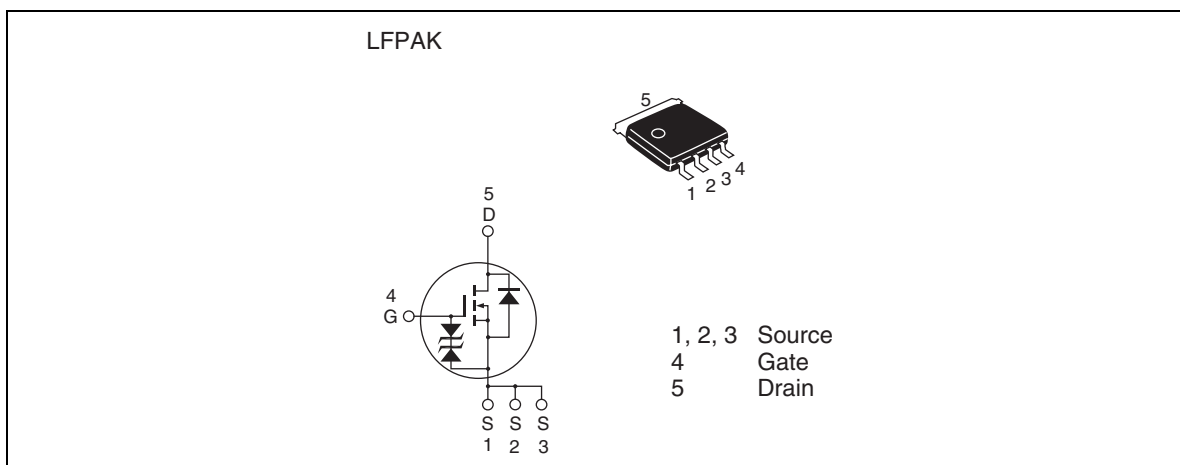
May.06.2003

Features

- Capable of 8V gate drive
- Low drive current
- High density mounting
- Low on-resistance

$R_{DS(on)} = 12 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



HAT2173H

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	25	A
Drain peak current	I _{D(pulse)} ^{Note1}	100	A
Body-drain diode reverse drain current	I _{DR}	25	A
Avalanche current	I _{AP} ^{Note 2}	25	A
Avalanche energy	E _{AR} ^{Note 2}	62.5	mJ
Channel dissipation	P _{ch} ^{Note3}	30	W
Channel to Case Thermal Resistance	θ _{ch-C}	4.17	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
3. T_c = 25°C

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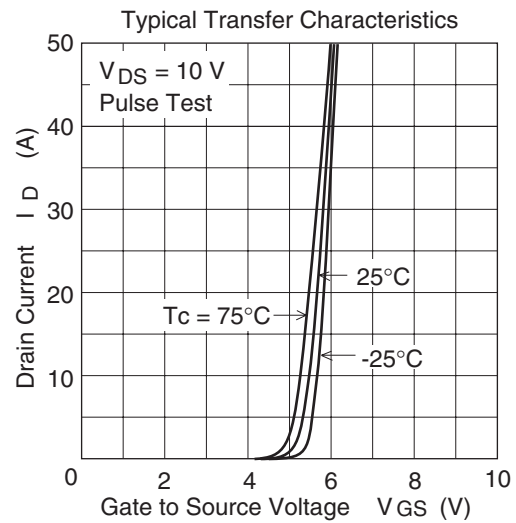
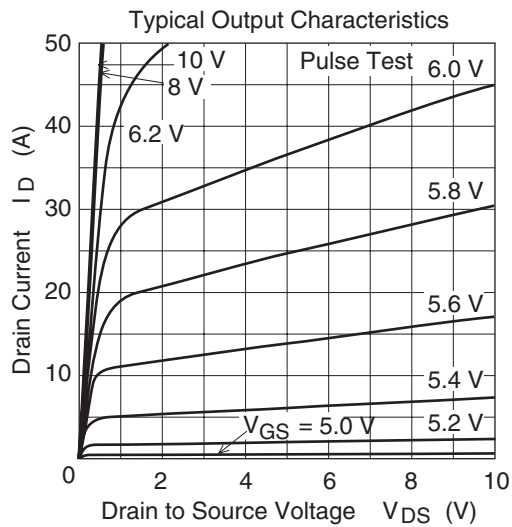
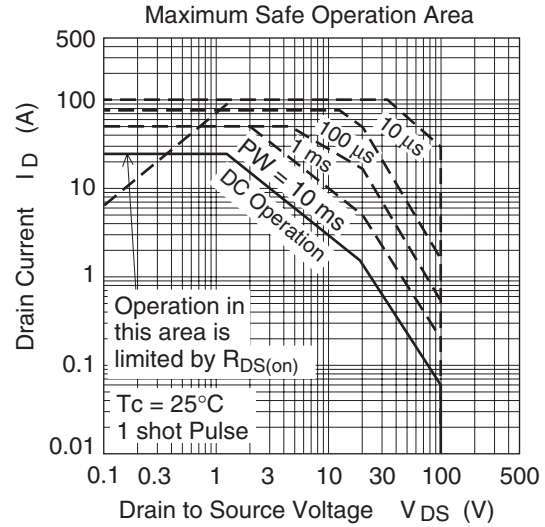
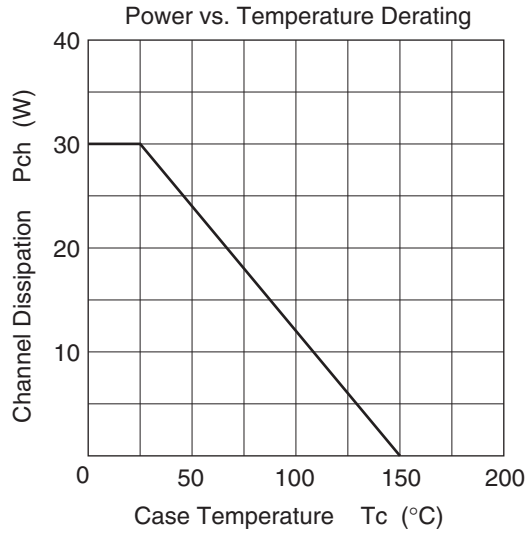
Electrical Characteristics

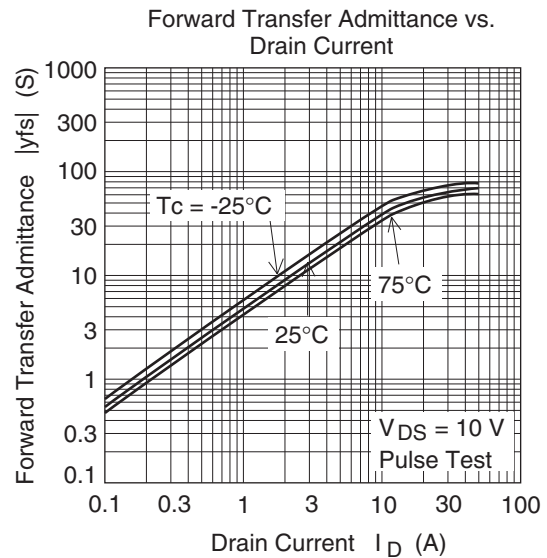
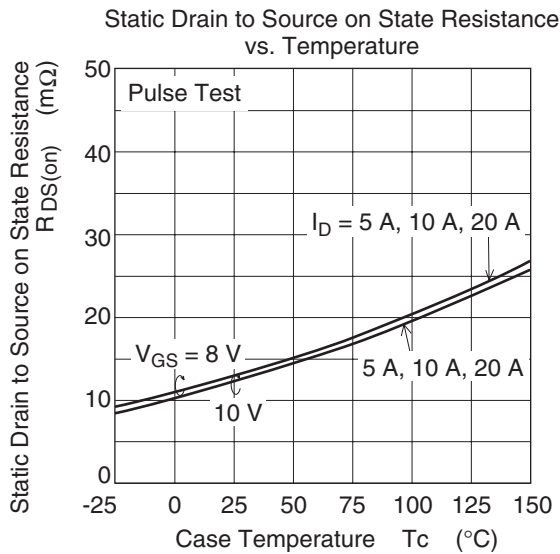
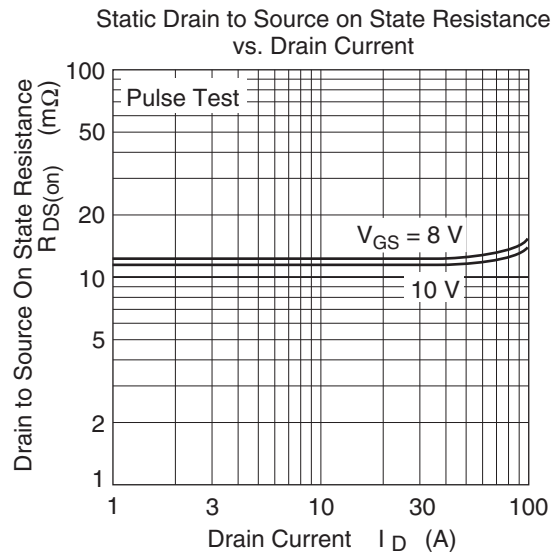
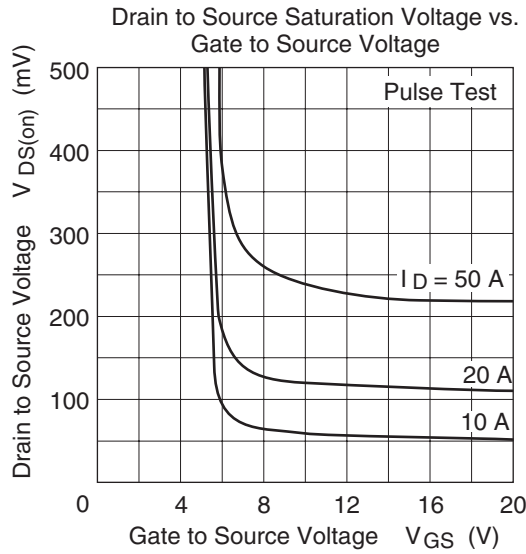
(Ta = 25°C)

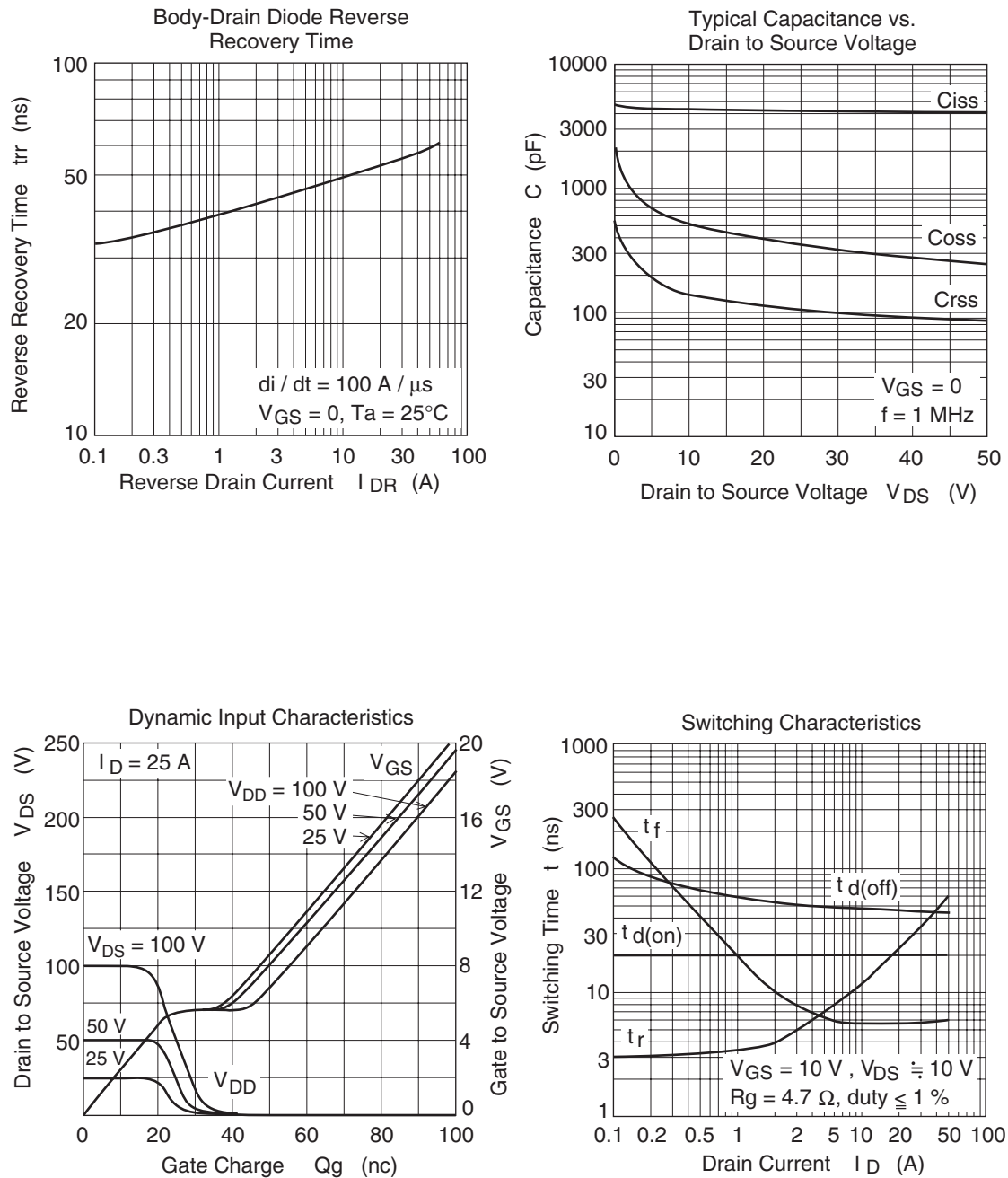
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	4.0	—	6.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 20 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	12	15	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	13	17.5	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 8 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = 12.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4350	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	520	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	150	—	pF	$f = 1 \text{ MHz}$
Gate resistance	R_g	—	0.5	—	Ω	
Total gate charge	Q_g	—	61	—	nc	$V_{DD} = 50 \text{ V}$
Gate to source charge	Q_{gs}	—	23	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	14.5	—	nc	$I_D = 25 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 12.5 \text{ A}$
Rise time	t_r	—	15	—	ns	$V_{DD} \approx 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	37	—	ns	$R_L = 2.4 \text{ }\Omega$
Fall time	t_f	—	5.7	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.82	1.07	V	$I_F = 25 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	55	—	ns	$I_F = 25 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

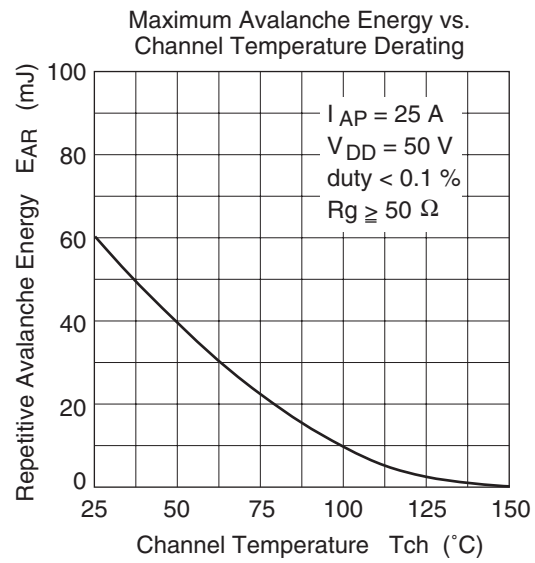
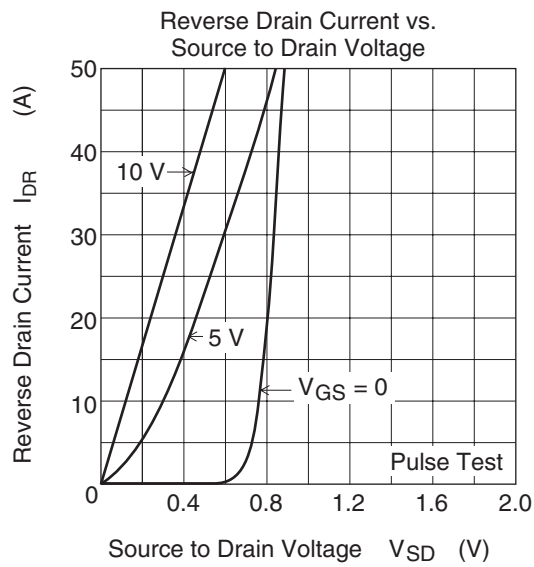
Notes: 4. Pulse test

Main Characteristics

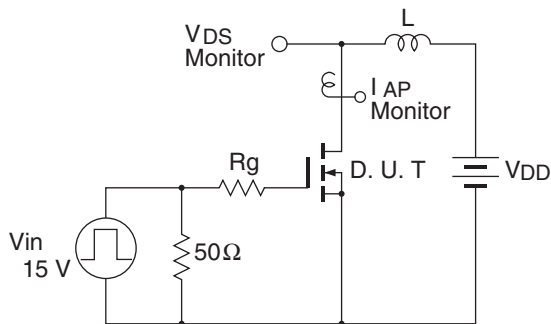






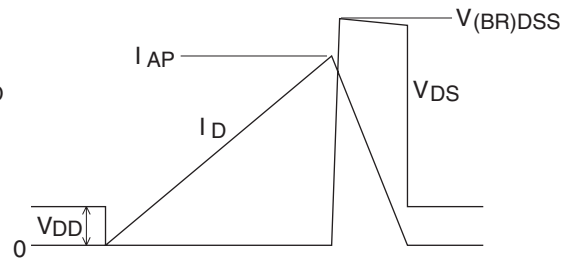


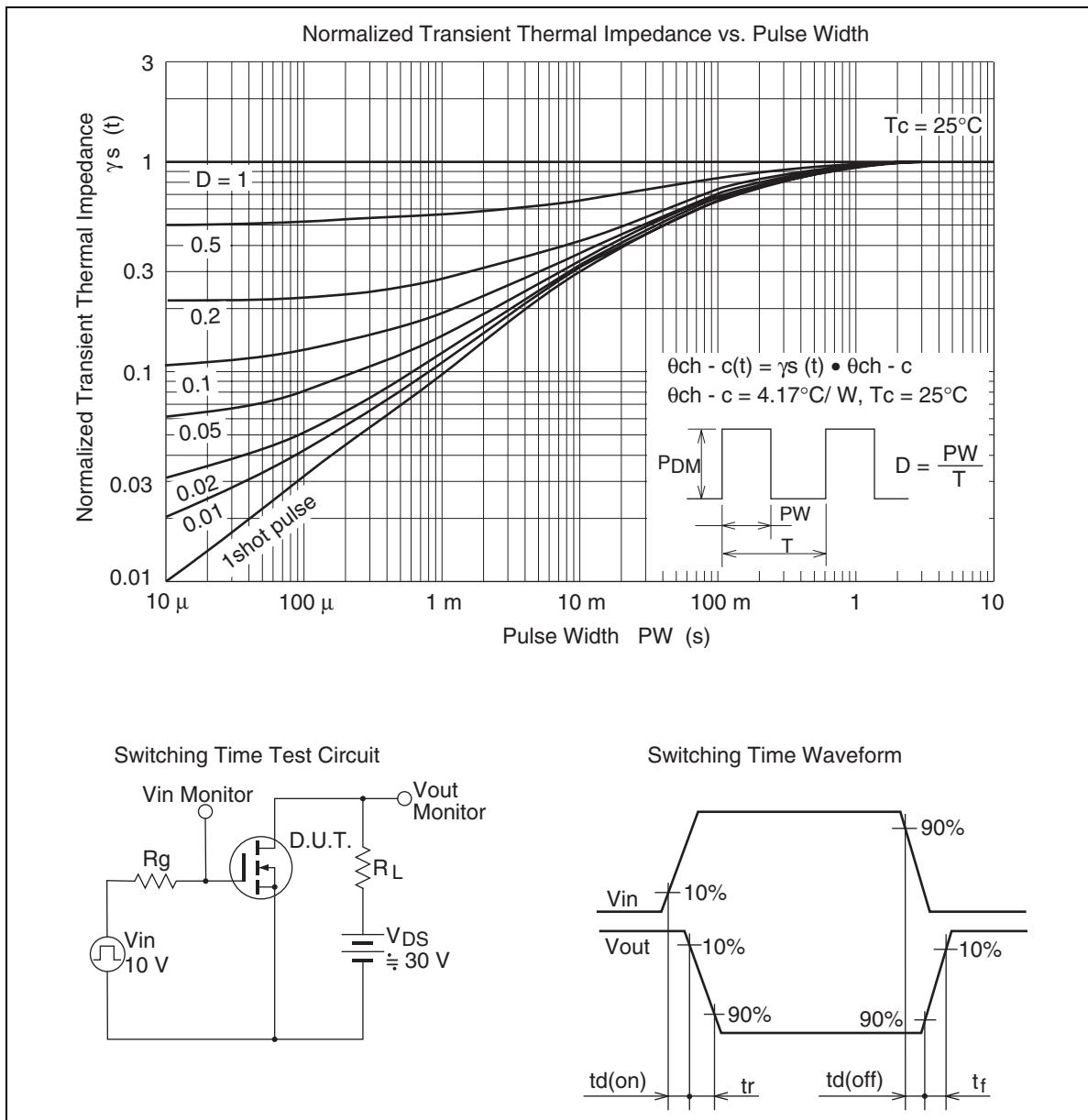
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

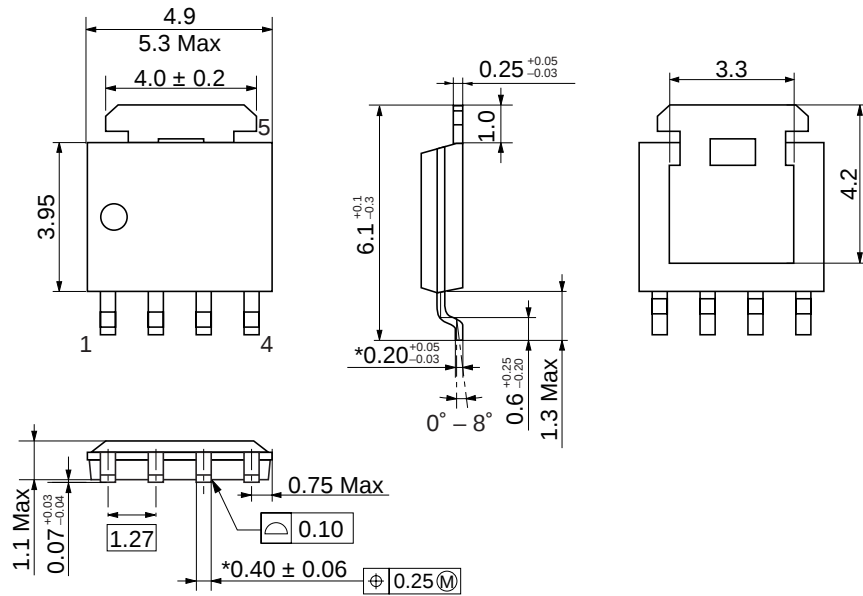
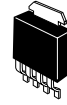




Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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