FAIRCHILD SEMICONDUCTOR®

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FSA805 — USB2.0 High-Speed (480Mbps), UART, and Audio Switch with Negative Signal Capability

Features

- 3:1 Switch Handles:
- Audio Headsets
- UART
- Up to 2 High-Full and Low-Speed USB Data
- Negative-Swing-Capable Audio Channel
- Built-in Termination Resistors for Audio Pop Reduction
- Simple Switch Control Using Two Select Pins

Applications

- Cell Phones, MP3 Players, PDAs

Description

The FSA805 is a 3:1 USB accessory switch that enables USB data, stereo/mono audio, and UART data to share a common connector port. It is designed for high-speed USB 2.0 signaling. The architecture is designed to allow audio signals to swing below ground (to -0.8V) so a common USB and headphone jack can be used for personal media players and portable peripheral devices.

The FSA805 meets both USB Rev. 2.0 and micro-USB specifications.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Eco Status	Package
FSA805UMX	-40 to +85°C	JZ	Green	12-Lead Quad, UMLP, 1.8x1.8mm

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

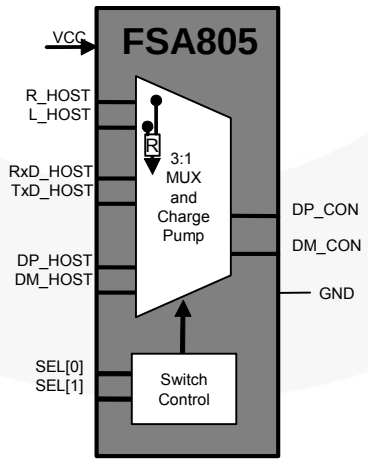


Figure 1. Functional Block Diagram

Application Diagram

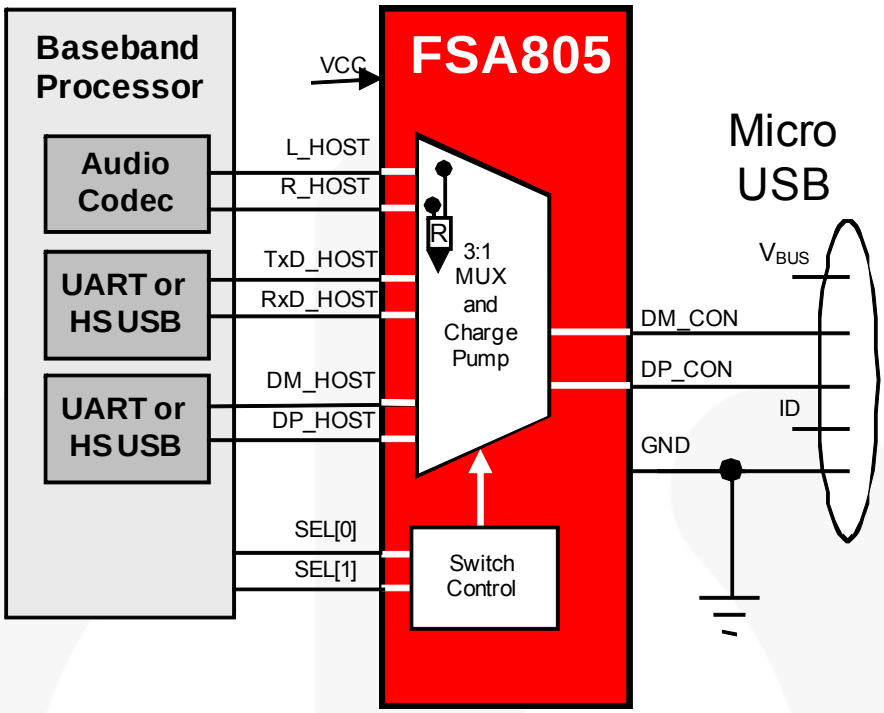


Figure 2. Typical Application

Functional Description

The FSA805 USB2.0 accessory switch is designed to consolidate wired accessories for portable devices, such as cellular telephones and portable audio players. The benefits of consolidation include reduced space requirements from a reduction of connectors and their size. The micro-USB connector, for example, reduces connector height and depth, allowing for slimmer overall designs. Using the USB industry standard and a common connector type for devices such as chargers and headsets, greatly reduces the waste associated with new phone purchases by allowing re-use of the devices.

Using just five wires for all connection types considerably reduces the cost of wired accessories and simplifies their construction. The FSA805 facilitates adopting this methodology because it is designed to redirect the DP/DM pins from the USB connector to one of three ports at the baseband's discretion.

Applications with Multiple USB Controllers

The FSA805 UART port (RxD_HOST, TxD_HOST) can be used as a High-speed USB interface. This allows it to operate in an application with two USB controllers (one full speed, and the other full or high speed).

In this configuration, it is recommended to configure the switches to OPEN before switching to the other (second) USB interface. The OPEN setting duration should be long enough for the accessory to go to a SE0 state, so when the switch is set to the other (second) USB port, the new controller re-enumerates.

Mode Descriptions

The FSA805 has two select pins to control the switching operations, SEL[0], and SEL[1]. Table 1 describes mode operation.

Table 1. Selection Truth Table

SEL[1]	SEL[0]	Switch Action	Description
0	0	OPEN	Open all switch paths (device in low-power mode)(1)
0	1	USB, UART	Closes USB/UART1 path to D+/D-, default condition(2) - DP_CON connected to RxD_HOST - DM_CON connected to TxD_HOST
1	0	USB, UART	Closes USB/UART2 path to D+/D- - DP_CON connected to DP_HOST - DM_CON connected to DM_HOST
1	1	AUDIO	Closes audio path to D+/D- only - DP_CON connected to R_HOST - DM_CON connected to L_HOST

Notes:

1. When the audio switch is in the OPEN position (Table 1, line1), the R and L are terminated to GND with internal termination resistors to discharge any stray capacitance that could cause audio pop.
2. The SELECT pins are CMOS inputs and should not be left in a floating condition. Some applications require the UART path be in the CLOSED position on power-up for initial programming of the device under test. If that condition is desired, the two SELECT pins should be pulled to the correct levels with external resistors that should exceed 100KΩ to reduce the static power consumption. In other applications, adding weak pull-down resistors to GND defaults the device to all paths open (low-power mode).

Pin Configuration

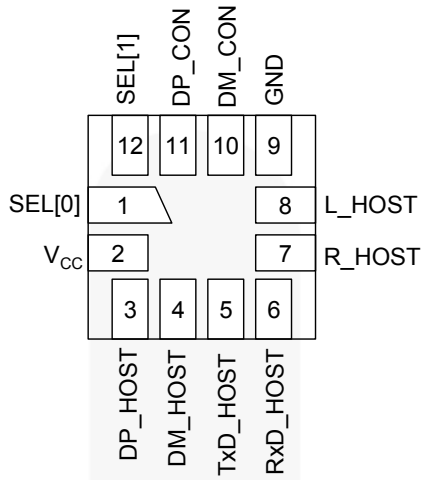


Figure 3. 12-Pin, UMLP Pin Assignments (Top-Through View)

Pin Descriptions

Name	Pin #	Description
USB Interface		
DP_HOST	3	D+ signal, dedicated USB port to be connected to the resident USB transceiver on the phone. Can also be used for UART signaling.
DM_HOST	4	D- signal, dedicated USB port to be connected to the resident USB transceiver on the phone. Can also be used for UART signaling.
Audio Interface		
R_HOST	7	Right audio channel from phone audio-out codec
L_HOST	8	Left audio channel from phone audio-out codec
UART Interface		
TxD_HOST	5	Tx connection from resident UART transceiver on the phone. Can also be used for HS USB signaling.
RxD_HOST	6	Rx connection from resident UART transceiver on the phone. Can also be used for HS USB signaling.
Power Interface		
V_{CC}	2	Input voltage supply pin to be connected to the phone battery output
Connector Interface		
GND	9	Ground
DP_CON	11	Connected to the USB connector D+ pin; depending on the signaling mode, this pin can share D+, R, Rxd, or MIC signals
DM_CON	10	Connected to the USB connector D- pin; depending on the signaling mode, this pin can share D-, L, or Txd signals
Switch Control		
SEL[1:0]	1,12	Switch selection pins; *refer to Table 1 for truth table*

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{CC}	Supply Voltage from Battery / Baseband			-0.5	6.0	V
V_{SW}	Switch I/O Voltage	USB		-1.0	V_{CC} +0.5	V
		Stereo/Mono Audio Path Active		-1.5	V_{CC} +0.5	
		All Other Channels		-0.5	V_{CC} +0.5	
I_{IK}	Input Clamp Diode Current			-50		mA
I_{SW}	Switch I/O Current (Continuous)	USB			50	mA
		Audio			60	
		All Other Channels			50	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)	USB			150	mA
		Audio			150	mA
		All Other Channels			150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System	USB Connector Pins (D+, D-)	Air Gap		13.0	kV
			Contact		8.0	
	JEDEC JESD22-A114, Human Body Model		All Pins		4.5	
	JEDEC JESD22-C101, Charged Device Model		All Pins		1.5	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Battery Supply Voltage		2.7	4.4	V
V_{SW}	Switch I/O Voltage	USB Path Active	0	3.6	V
		Audio Path Active	-0.8	0.8	V
		UART Active	0	4.4	V
T_A	Operating Temperature		-40	+85	ºC

Switch Path DC Electrical Characteristics

All typical values are at T_A=25ºC unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Host Interface Pins (SEL[1:0])							
V_{IH}	Input High Voltage	3.2 to 4.4		1.3			V
V_{IL}	Input Low Voltage	3.2 to 4.4				0.7	V
Switch Off Characteristics							
I_{OFF}	Power Off Leakage Current	0	All Ports Except Audio Path V_{SW}=0V to 4.4V, Figure 9			10	µA
USB Switch On Path							
USB Analog Signal Range		3.2 to 4.4		0		3.6	V
R_{ONUSB}	HS Switch On Resistance(3)	3.2 to 4.4	$V_{D+/D-}$=0V, 0.4V, I_{ON}=8mA, Figure 8		6	9	Ω
Audio R/L Switch On Paths							
Audio Analog Signal Range		3.2 to 4.4		-0.8		0.8	V
R_{ONAUD}	Audio Switch On Resistance(3)	3.2 to 4.4	$V_{L/R}$=-0.8V, 0.8V, I_{ON}=30mA, Figure 8			3	Ω
R_{FLAT}	Audio R_{ON} Flatness(4)	3.2 to 4.4			0.1		Ω
R_{TERM}	Internal Termination Resistors(5)				1		kΩ
UART Switch On Path							
Analog Signal Range		3.2 to 4.4	V_{SW}=0V, 4.4V, I_{ON}=8mA	0		V_{CC}	V
R_{ONUART}	Switch On Resistance(3)	3.2 to 4.4	$V_{TxD/RxD}$=0V, 3.2V, I_{ON}=8mA, Figure 8		25		Ω
Total Switch Current Consumption							
I_{CCSL}	Battery Supply Sleep Mode Average Current	3.2 to 4.4	Static Current During Sleep Mode (SEL[1:0]=0)		10	15	µA
I_{CCWK}	Battery Supply Active Mode Average Current	3.2 to 4.4	Average Pulse Current (~100µs Pulse)		80	110	µA
I_{CCSELT}	Increase in I_{CCSL}/I_{CCWK} Current per Control Voltage and V_{CC}	3.2 to 4.4	V_{SEL} = 2.8V and V_{CC} = 4.4V			8	µA
			V_{SEL} = 1.8V and V_{CC} = 4.4V			10	µA

Notes:

3. On resistance is determined by the voltage drop between the both sides of the switch at the indicated current through the switch.
4. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.
5. Guaranteed by characterization; not production tested.

Switch Path AC Electrical Characteristics[6]

All typical value are for V_{CC} =3.8V at T_A=25ºC unless otherwise specified.

Symbol	Parameter		Conditions	Typical	Unit	Figure
Q	Charge Injection	Audio Mode	1.0nF, V_S=0V, R_S=0Ω	4	pC	Figure 13
		UART Mode		4		
		USB Mode		6		
Xtalk	Active Channel Crosstalk DP_CON to DM_CON	Audio Mode	f=20kHz, R_T=32Ω, C_L=0pF	-95	dB	Figure 12
		UART Mode	f=1MHz, R_T=50Ω, C_L=0pF	-75		
		USB Mode				
	Active Channel Crosstalk MIC	MIC on VBUS to R_HOST, L_HOST	f=20kHz, R_T=32Ω, C_L=0pF	-105		
		MIC on DP_CON to L_HOST (DM_CON)				
O_{IRR}	Off Isolation Rejection Ratio	Audio Path L_HOST to DM_CON, R_HOST to DP_CON	f=20kHz, R_T=32Ω, C_L=0pF	-100	dB	Figure 11
		USB Path DM_HOST to DM_CON, DP_HOST to DP_CON	f=1 MHz, R_T=50Ω, C_L=0pF	-80		
		UART Path TxD_HOST to DM_CON, RxD_HOST to DP_CON		-85		
THD+N	Total Harmonic Distortion + Noise (Audio Path)		20Hz to 20kHz, R_L=16Ω, Input Signal Range 1.6V_{PP}	0.037	%	Figure 16
			20Hz to 20kHz, R_L=32Ω, Input Signal Range 1.6V_{PP}	0.025	%	Figure 16
t_J	Total Jitter (USB Mode)		R_L=50Ω, C_L=50pF, t_r=t_f=500ps (10-90%) at 480Mbps (PRBS=2^{15}–1)	130	ps	
BW	-3db Bandwidth (USB Mode DPHost/DMHost)		R_L=50Ω, C_L=0pF	1150	MHz	Figure 10
			R_L=50Ω, C_L=5pF	550	MHz	Figure 10

Note:

6. Guaranteed by characterization; not production tested.

Capacitance

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = -40 to +85°C			Unit	Figure
				Min.	Typ.	Max.		
C_{IN}	Select Pins Capacitance(7)	0	V_{BIAS}=0.2V		2.0		pF	Figure 14
$C_{ON(D+, D-)}$	D+, D- On Capacitance (HS USB Mode)(7)	3.8	V_{BIAS}=0.2V, f=1MHz		6.5		pF	Figure 15

Note:
7. Guaranteed by characterization; not production tested.

High Speed USB Eye Compliance Results for All FSA805 Signal Paths

The following figures show high-speed USB 2.0 eye diagrams for each path of the FSA805. Full compliance reports are available upon request. Figure 4 shows the eye diagram of the high-speed USB source used for testing of the FSA800 and FSA805 paths.

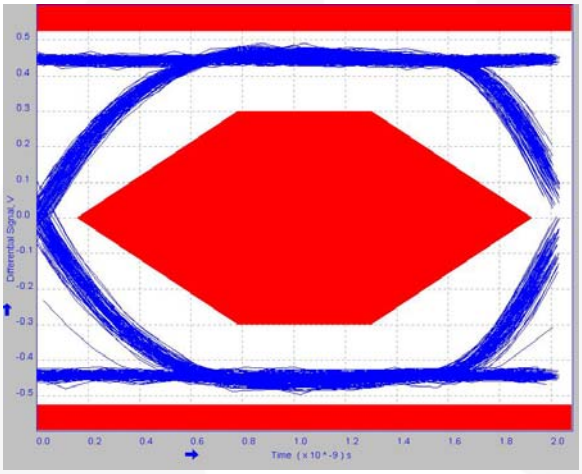


Figure 4. High-Speed Eye Diagram for Source Used for All Testing

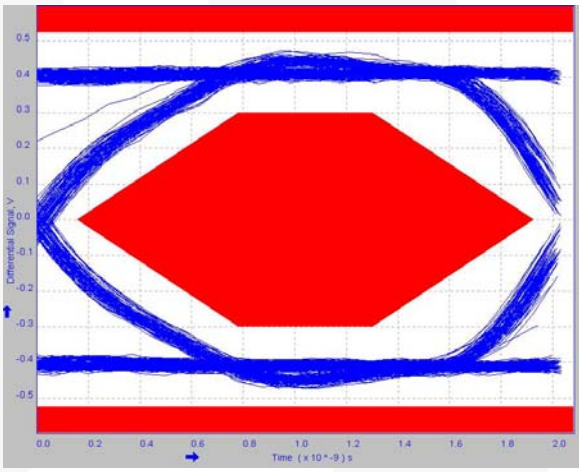


Figure 5. USB (DP_HOST/DM_HOST) Path High-Speed Eye Diagram

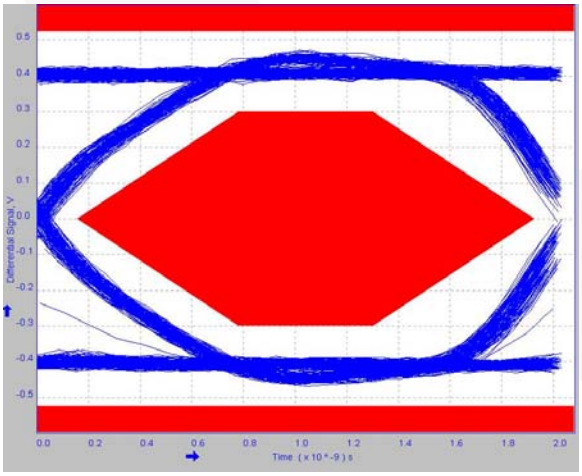


Figure 6. UART (TxD_HOST/RxD_HOST) High-Speed Eye Diagram

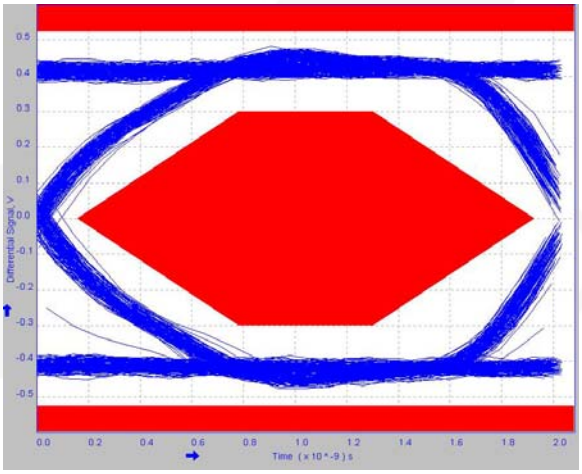


Figure 7. Audio Path High-Speed Eye Diagram

Test Diagrams

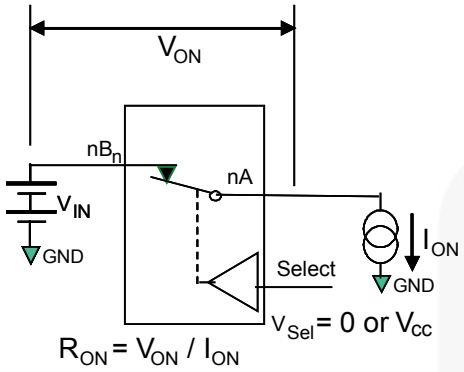
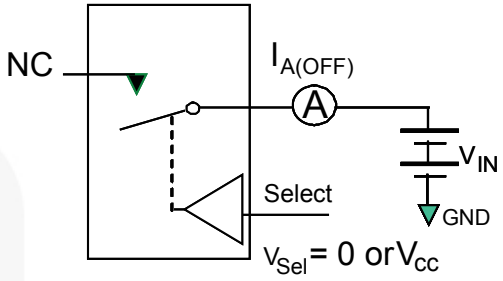
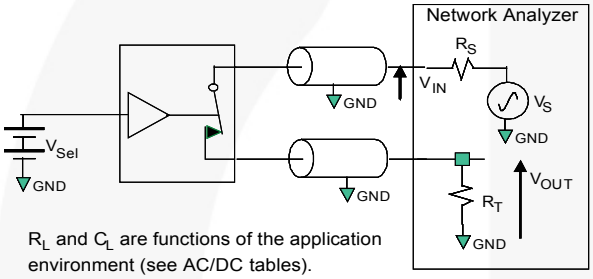


Figure 8. On Resistance



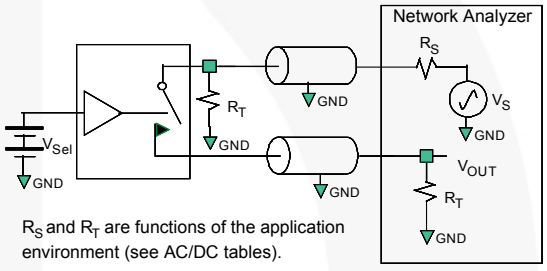
**Each switch port is tested separately.

Figure 9. Off Leakage



R_L and C_L are functions of the application environment (see AC/DC tables).
C_L includes test fixture and stray capacitance.

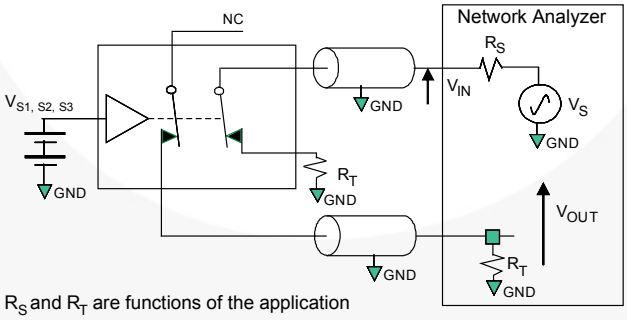
Figure 10. Bandwidth



R_S and R_T are functions of the application environment (see AC/DC tables).

Off-Isolation = 20 Log (V_{OUT} / V_{IN})

Figure 11. Channel Off Isolation



R_S and R_T are functions of the application environment (see AC tables for values).

CROSSTALK = 20 Log (V_{OUT}/ V_{IN})

Figure 12. Adjacent Channel Crosstalk

Test Diagrams (Continued)

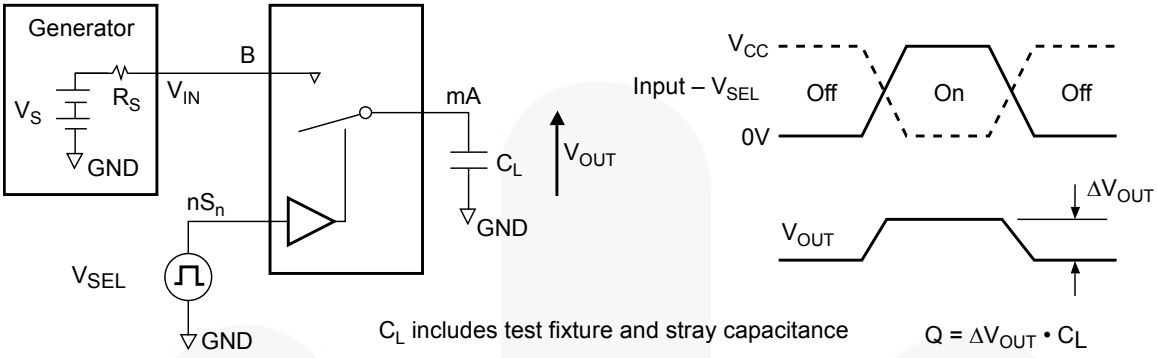


Figure 13. Charge Injection Test

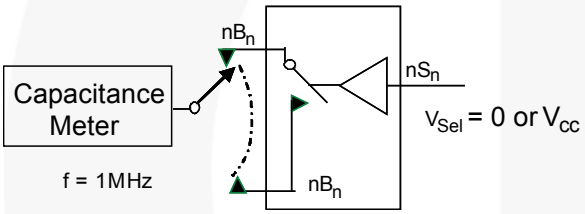


Figure 14. Channel Off Capacitance

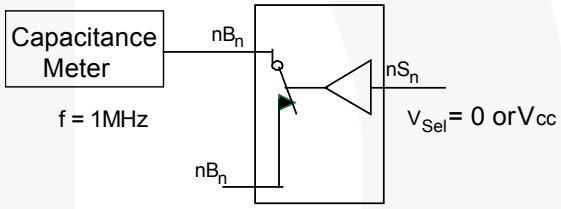


Figure 15. Channel On Capacitance

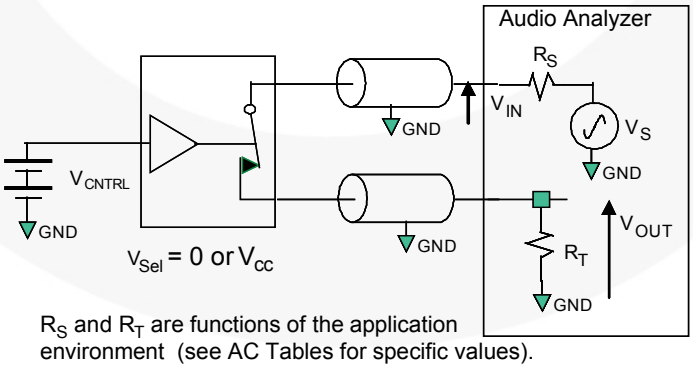
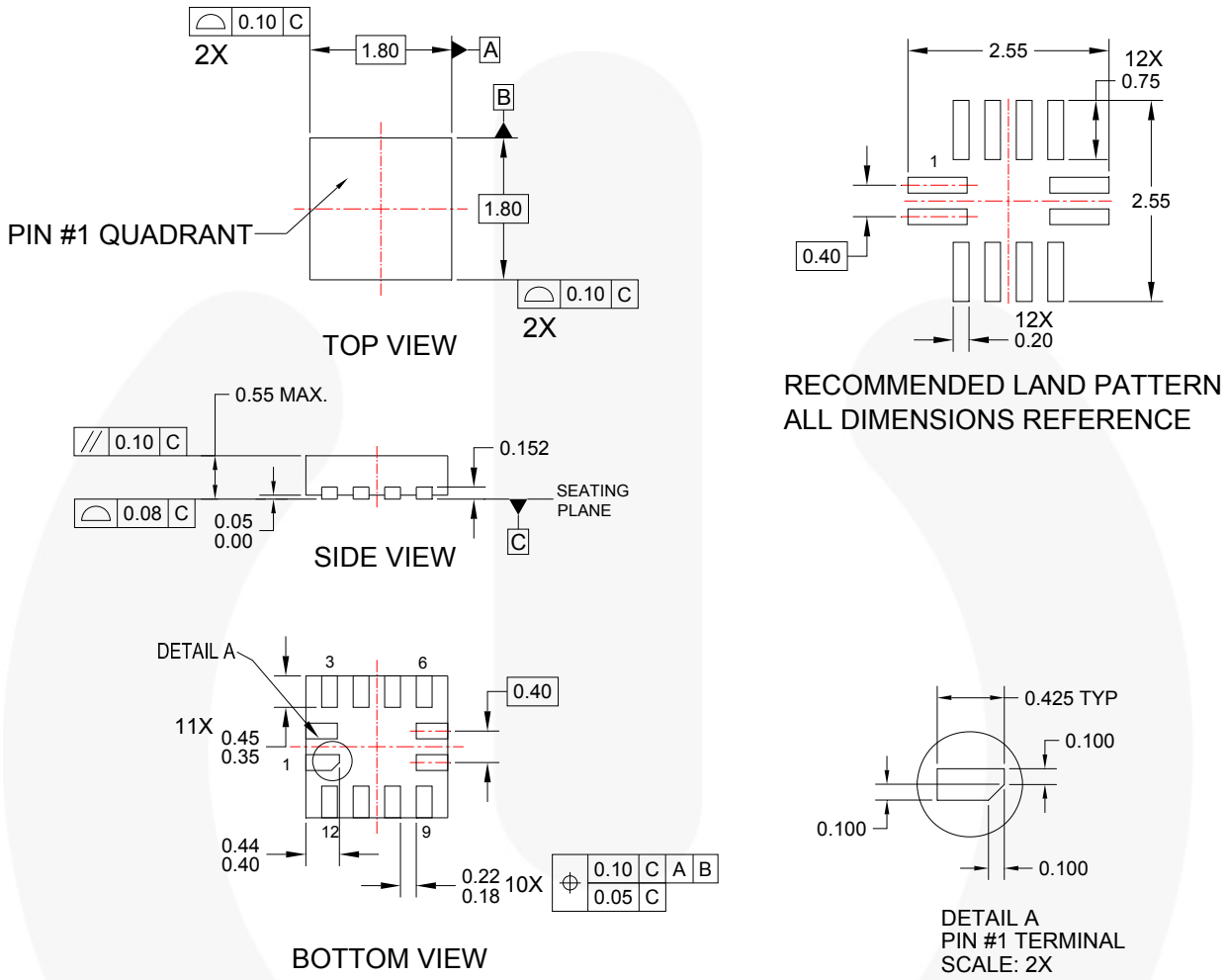


Figure 16. Total Harmonic Distortion

Physical Dimensions



NOTES:

A. DIMENSIONS ARE IN MILLIMETERS.

B. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

C. LANDPATTERN PER IPC LANDPATTERN CALCULATOR V 2009.18.00

D. DRAWING FILENAME: MKT-UMLP12A REVISION2

Figure 17. 12-Lead Quad, UMLP, 1.8x1.8mm

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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