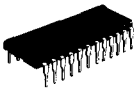
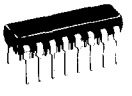
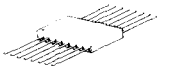
MC10,100/10,200 Series (-30 to +85°C)
MC10,500/10,600 Series (-55 to +125°C)

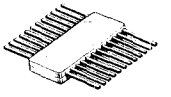
MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

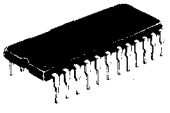
Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.

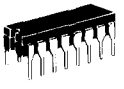

L SUFFIX
CERAMIC PACKAGE
CASE 623

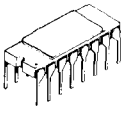

P SUFFIX
PLASTIC PACKAGE
CASE 648


F SUFFIX
CERAMIC PACKAGE
CASE 650


F SUFFIX
CERAMIC PACKAGE
CASE 652


P SUFFIX
PLASTIC PACKAGE
CASE 649


L SUFFIX
CERAMIC PACKAGE
CASE 620


AL SUFFIX
CERAMIC PACKAGE
CASE 690

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

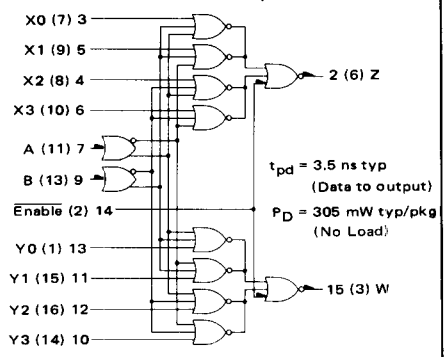
Function	Type① -30 to +85°C	Type① -55 to +125°C	Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
Quad 2-Input NOR Gate With Strobe	MC10100	–	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	–	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	–	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	–	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	–	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	–	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	–	–	–	620
Bus Driver	MC10128	–	12.0	700	620
Quad Bus Receiver	MC10129	–	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	f = 160 MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	–	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	–	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	f = 140 MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	f = 150 MHz	625	620,650

① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*External Load Power not included.

DATA SELECTORS/MULTIPLEXERS (continued)

MC10174 / MC10574
Dual 4 to 1 Multiplexer

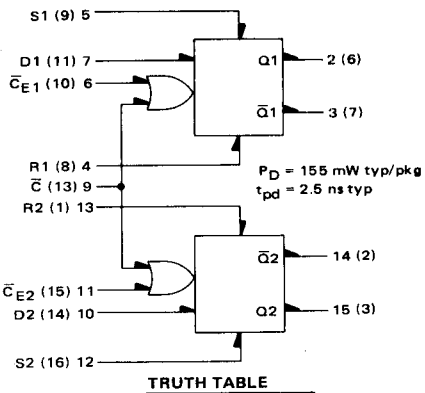


TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

MC10130 / MC10530
Quad Latch



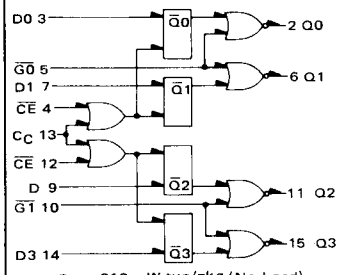
TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care.

LATCHES

MC10133 / MC10533
Quad Latch



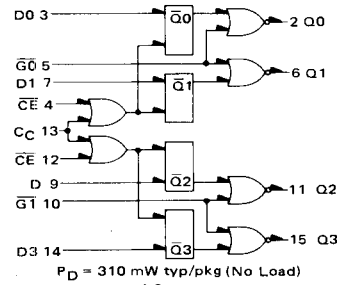
PD = 310 mW typ/pkg (No Load)
tpd = 4.0 ns typ

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
C = $\overline{C}_C$ + CE

MC10153
Quad Latch



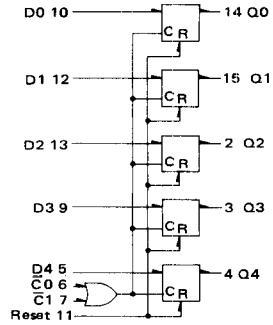
PD = 310 mW typ/pkg (No Load)
tpd = 4.0 ns typ

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
C = $\overline{C}_C$ + CE

MC10175 / MC10575
Quint Latch



PD = 400 mW typ/pkg (No Load)
tpd = 2.5 ns typ

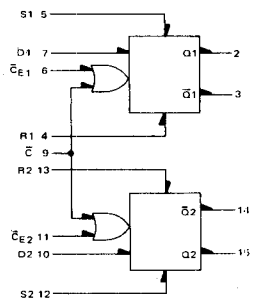
TRUTH TABLE

D	C0	C1	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

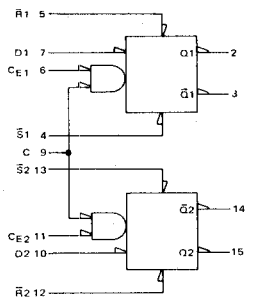
DUAL LATCH

MC10130

POSITIVE LOGIC



NEGATIVE LOGIC



TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
φ	L	H	Q_n
φ	H	L	Q_n
φ	H	H	Q_n

φ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

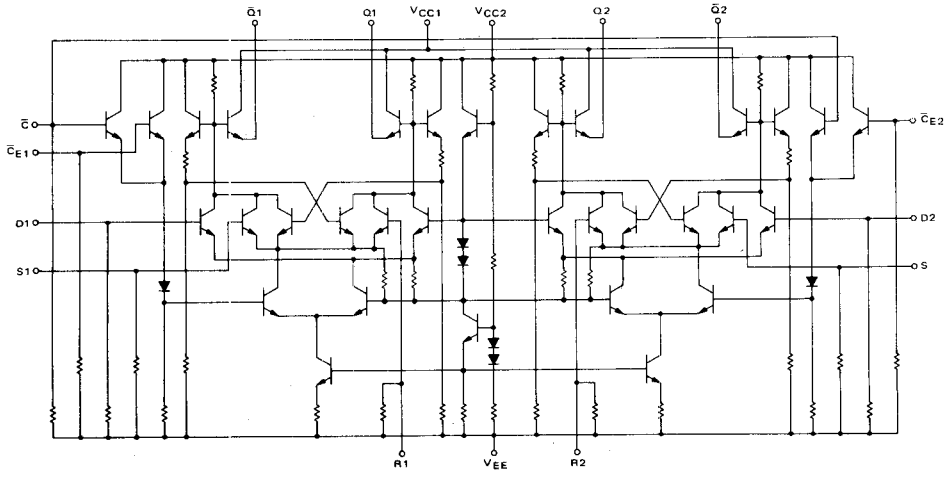
Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

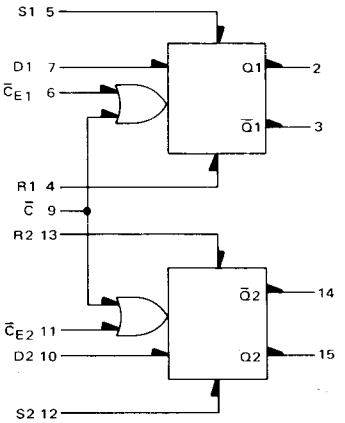
CIRCUIT SCHEMATIC

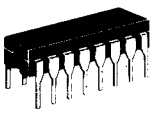


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

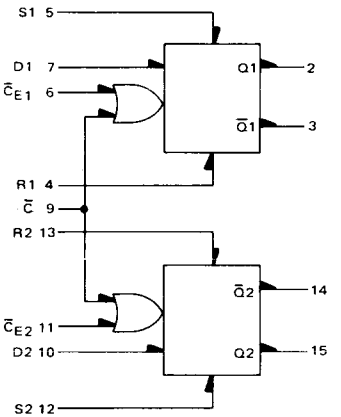
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10130L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	35	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	–	–	–	220	–	–	μAdc	6,11	–	–	–	8	1,16
		9	–	–	–	–	265	–	–		9	–	–	–		
		4,5,9	–	–	–	–	285	–	–		4,5,9	–	–	–		
		7,10,12,13	–	–	–	–	285	–	–		7,10,12,13	9	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910		Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630		-1.595	Vdc	–	9	–	–	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	1.0	3.6	1.0	2.5	3.5	1.0	3.8	ns	–	–	7	2	8	1,16
	t_{5+2+}			3.6		2.7		1.1	3.9		6	–	5			
	t_{4+2-}			3.6		2.7		1.1	3.9		6	–	4			
	t_{6-2+}			4.3		–	4.0	1.0	4.1		–	–	6			
Rise Time (20% to 80%)	t_{2+}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7			
Fall Time (20% to 80%)	t_{2-}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7			
Setup Time	t_{setup}	2	–	–	2.5	–	–	–	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	–	–	1.5	–	–	–	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.



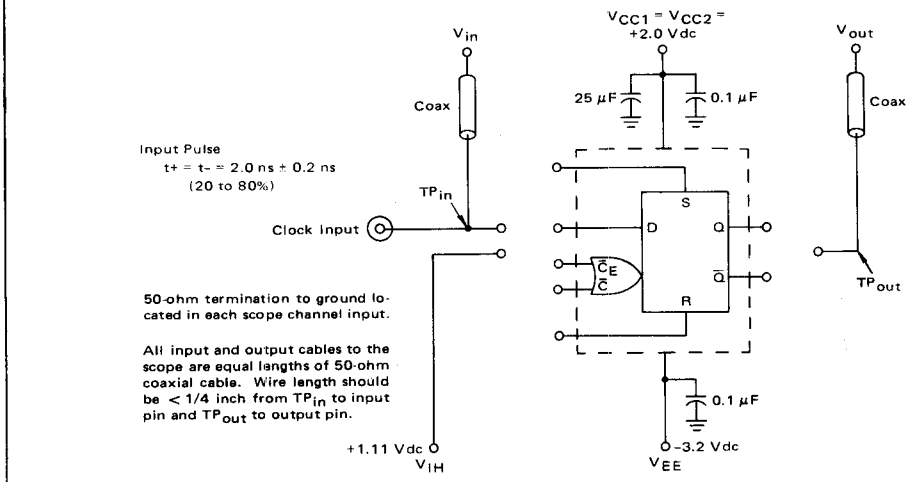
P SUFFIX
PLASTIC PACKAGE
CASE 648

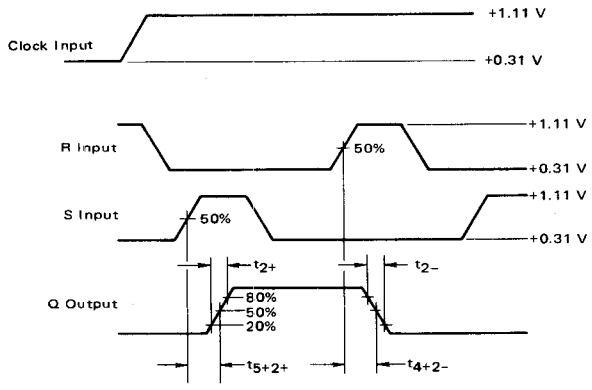
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

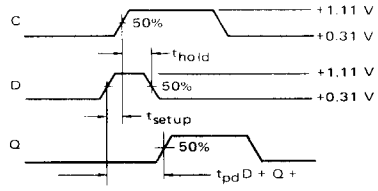
Characteristic	Symbol	Pin Under Test	MC10130P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	30	35	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	–	–	–	220	–	–	μAdc	6,11	–	–	–	8	1,16
		9	–	–	–	–	265	–	–		9	–	–	–		
		4,5,9	–	–	–	–	285	–	–		4,5,9	–	–	–		
		7,10,12,13	–	–	–	–	285	–	–		7,10,12,13	9	–	–		
	I_{inL}	4*	–	–	0.50	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9	–	–	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	–	–	1.0	2.5	3.5	–	–	ns	–	–	7	2	8	1,16
	t_{5+2+}		–	–		2.7		–	–		6	–	5			
	t_{4+2-}		–	–		2.7		–	–		6	–	4			
	t_{6-2+}		–	–		–	4.0	–	–		–	–	6			
Rise Time (20% to 80%)	t_{2+}		–	–	1.1	2.7	3.5	–	–		–	–	7			
Fall Time (20% to 80%)	t_{2-}		–	–	1.1	2.7	3.5	–	–		–	–	7			
Setup Time	t_{setup}	2	–	–	2.5	–	–	–	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	–	–	1.5	–	–	–	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25° C







NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).