PI6LC48H02

PCIe® 4.0/3.0/2.0/1.0 Clock Generator with 2 HCSL Outputs

Features

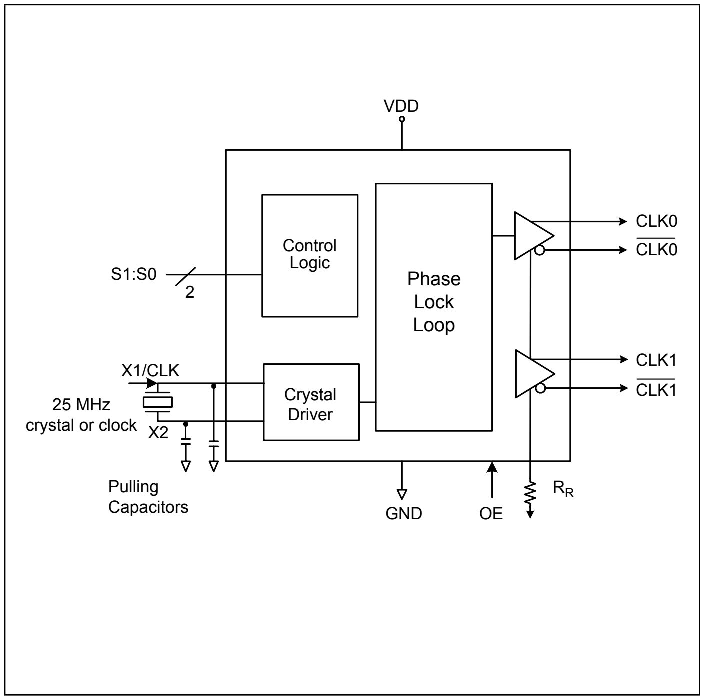
- ➔ PCIe® 4.0/3.0/2.0/1.0 compliant
- ➔ LVDS compatible outputs
- ➔ Supply voltage of 3.3V ±10%
- ➔ 25MHz crystal or clock input frequency
- ➔ HCSL outputs, 0.8V Current mode differential pair
- ➔ Jitter 35ps cycle-to-cycle (typ)
- ➔ RMS phase jitter 12kHz ~ 20MHz @ 100MHz - 0.32ps (typ)
- ➔ RMS phase jitter 12kHz ~ 20MHz @ 125MHz - 0.3ps (typ)
- ➔ Industrial temperature range
- ➔ Packaging: (Pb-free and Green)
  - ▫ 16-pin TSSOP (L16)

Description

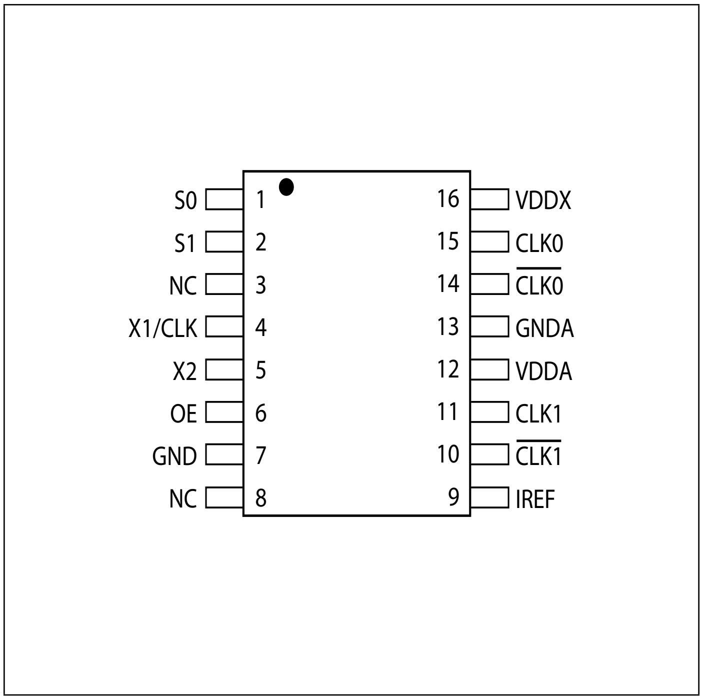
The PI6LC48H02 is a clock generator compliant to PCI Express® 4.0/3.0/2.0/1.0 and Ethernet requirements. The device is used for PC or embedded systems.

The PI6LC48H02 provides two differential (HCSL) or LVDS outputs. Using Diodes' patented Phase Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 25MHz, 100MHz, 125MHz, 200MHz clock frequencies.

Block Diagram



Pin Configuration (16-Pin TSSOP)



Pin Description

Pin #	Pin Name	I/O Type	Description
1	S0	Input	Select pin 0 (Internal pull-up resistor). See Table 1.
2	S1	Input	Select pin 1 (Internal pull-up resistor). See Table 1.
3	NC	-	Do not connect
4	X1/CLK	Input	Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
5	X2	Output	Crystal connection. Leave unconnected for clock input.
6	OE	Input	Output enable. Internal pull-up resistor.
7	GND	Power	Ground
8	NC	-	Do not connect
9	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
10	$\overline{\text{CLK1}}$	Output	HCSL compliment clock output
11	CLK1	Output	HCSL clock output
12	VDDA	Power	Connect to a +3.3V source.
13	GNDA	Power	Output and analog circuit ground.
14	$\overline{\text{CLK0}}$	Output	HCSL compliment clock output
15	CLK0	Output	HCSL clock output
16	VDDX	Power	Connect to a +3.3V source.

Table 1: Output Select Table

S1	S0	CLK(MHz)
0	0	25
0	1	100
1	0	125
1	1	200

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between each V_{DD} pin and the ground plane and placed as close to the V_{DD} pin as possible.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors

C_L = Crystals's load capacitance in pF

Crystal Capacitors (pF) = (C_L - 8) *2

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16-8)*2=16.

Current Source (IREF) Reference Resistor - R_R

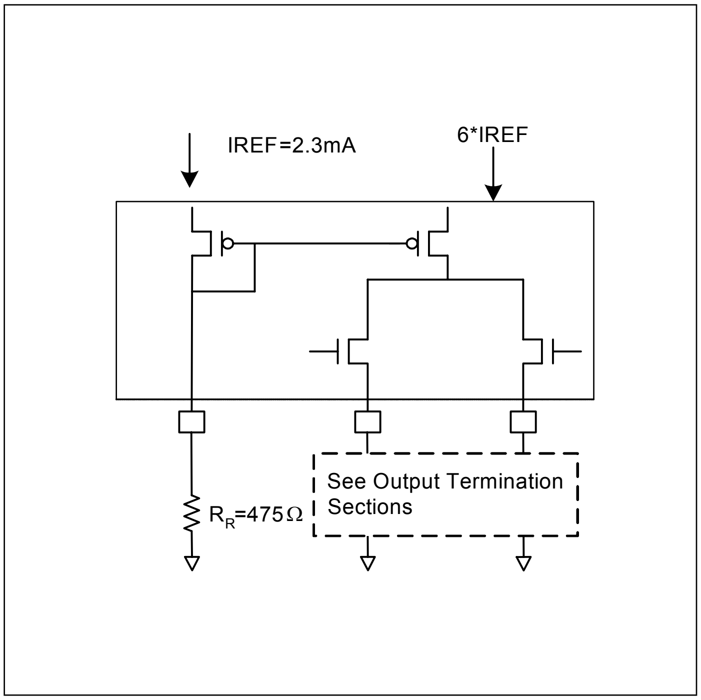
If board target trace impedance is 50Ω,
then R_R = 475Ω providing an IREF of 2.32 mA. The output current (I_{OH}) is 6*IREF.

Output Termination

The PCI Express differential clock outputs of the PI6LC48H02 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6LC48H02 can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

Output Structures



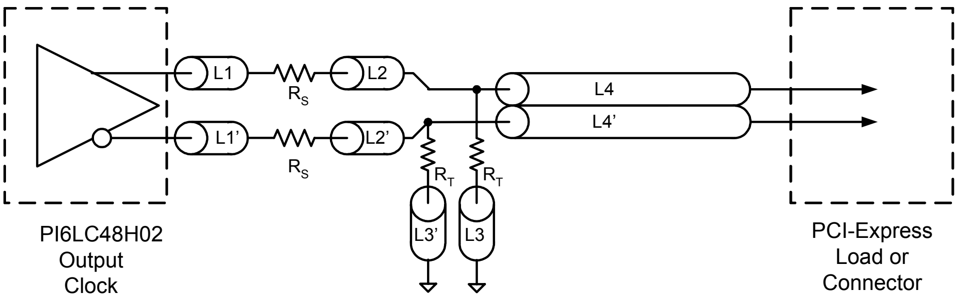
PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω

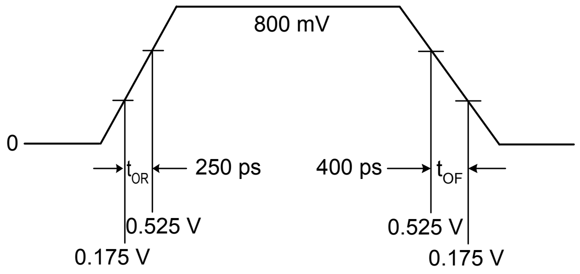
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	0.225 min to 12.6 max	inch

PCI Express Device Routing



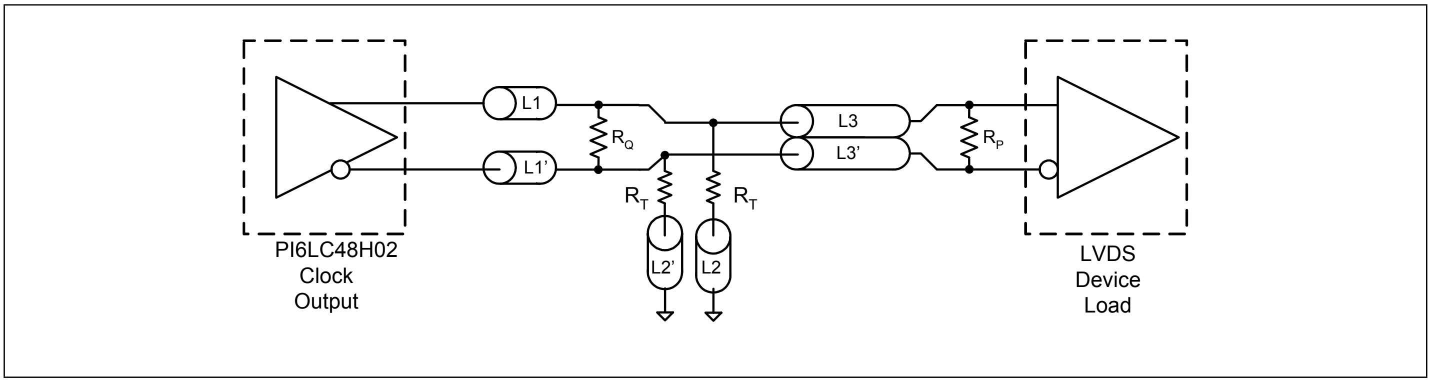
Typical PCI Express (HCSL) Waveform



Application Information

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
RP	100	Ω
RQ	100	Ω
RT	150	Ω
L3 length, route as 100Ω differential trace.		
L3 length, route as 100Ω differential trace.		

LVDS Device Routing



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential	4.6V
All Inputs and Outputs	-0.5V to V_{DD}+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (HBM)	2000 V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Specifications

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Characteristics (V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage[(1)]	OE, S0, S1	2.0		V_{DD} +0.3	V
V_{IL}	Input Low Voltage[(1)]	OE, S0, S1	GND -0.3		0.8	V
I_{IH}	Input High Current	Vin = V_{DD}	-5		5	µA
I_{IL}	Input Low Current	Vin = 0	-20		20	
I_{DD}	Operating Supply Current	R_L = 50Ω, C_L = 2pF			115	mA
I_{DDOE}		OE = LOW			65	mA
C_{IN}	Input Capacitance	@ 55MHz			7	pF
C_{OUT}	Output Capacitance	@ 55MHz			6	pF
L_{PIN}	Pin Inductance				5	nH
R_{OUT}	Output Resistance	CLK Outputs	3.0			kΩ

Notes:

1. Single edge is monotonic when transitioning through region.

HCSL Output AC Characteristics (V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Industry Max.	Unit
F_{IN}	Input Frequency			25			MHz
F_{OUT}	Output Frequency		25		200		MHz
V_{OH}	Output High Voltage (1,2)	100 MHz HCSL output @ V_{DD} = 3.3V	660	800	900		mV
V_{OL}	Output Low Voltage(1,2)		-150	0			mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute	250	350	550		mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges			140		mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			35	60		ps
J_{Phase}	RMS Phase Jitter, (Random)	100MHz 25MHz Xtal input, 12kHz - 20MHz		0.32	0.5		ps
		125MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5		ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output - Low BW		0.4	1.0	3.0	ps
		PCIe 2.0 Test Method @ 100MHz Output - High BW		1.9	2.5	3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.42	1.9	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.05	2.5	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	0.7	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	0.7	1	ps
$J_{RMS4.0}$	PCIe 4.0 RMS Jitter	PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)		0.37	0.45	0.5	ps
t_{OR}	Rise Time(1,2)	From 0.175V to 0.525V	175		700		ps
t_{OF}	Fall Time(1,2)	From 0.525V to 0.175V	175		700		ps
T_{SKEW}	Skew between outputs	At Crossing Point Voltage			50		ps
$T_{DUTY-CYCLE}$	Duty Cycle(1,3)		45		55		%
T_{OE}	Output Enable Time(5)	All outputs			10		µs
T_{OT}	Output Disable Time(5)	All outputs			10		µs
t_{STABLE}	Stabilization Time	From Power-up V_{DD}=3.3V		3.0			ms

Notes:

1. R_L = 50-Ohm with C_L = 2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Thermal Characteristics

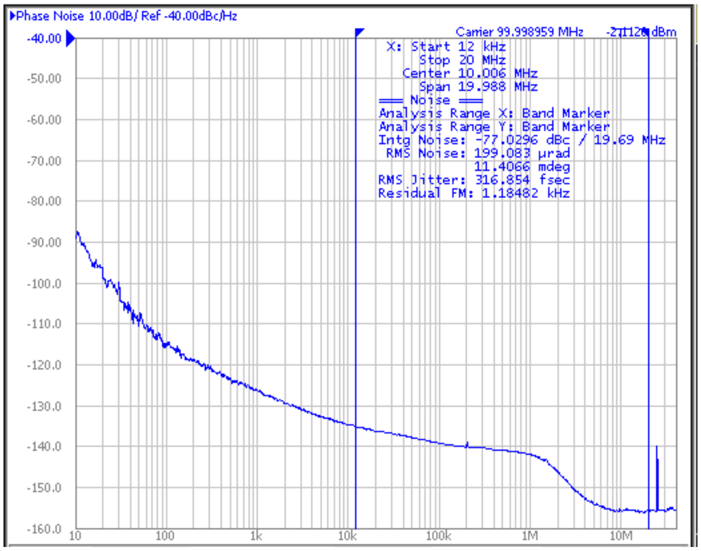
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			90	°C/W
θ_{JC}	Thermal Resistance Junction to Case				24	°C/W

Recomended Crystal Specification

Diodes recommends:
a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
b) FY2500107, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
c) FL2500038, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm

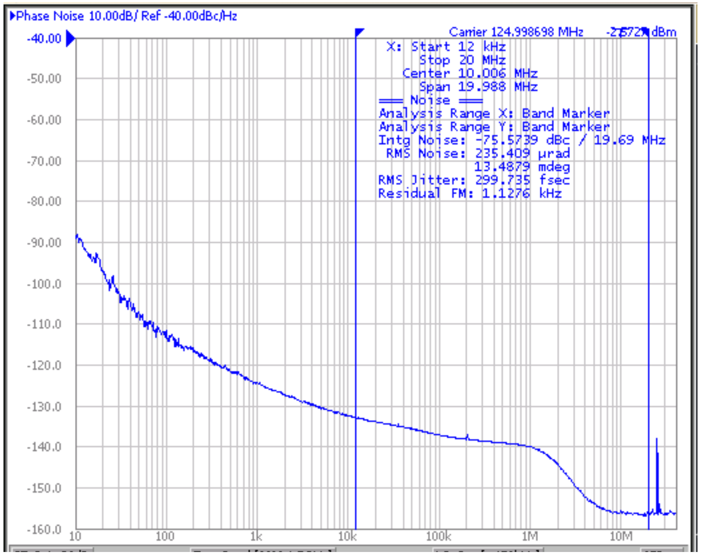
Phase Noise Plot

100MHz



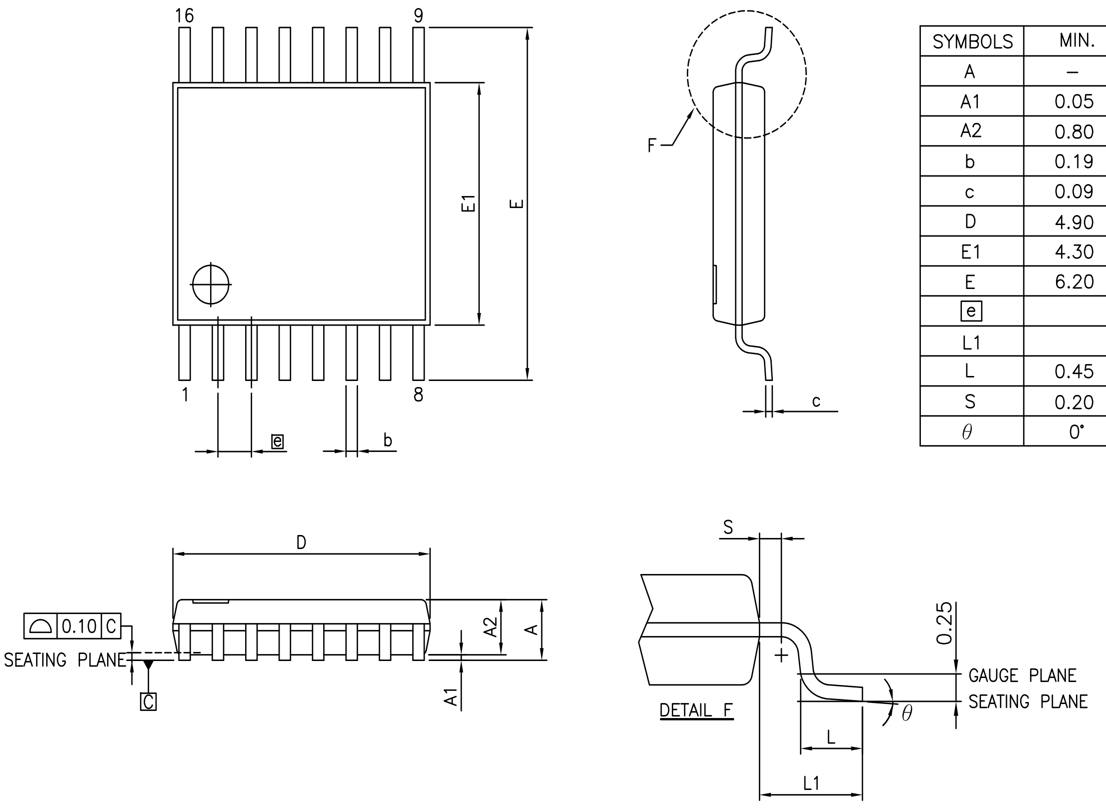
```
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -77.0296 dBc / 19.69 MHz
 RMS Noise: 199.083 µrad
            11.4066 mdeg
RMS Jitter: 316.854 fsec
Residual FM: 1.18482 kHz
```

125MHz



```
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -75.5739 dBc / 19.69 MHz
 RMS Noise: 235.409 µrad
            13.4879 mdeg
RMS Jitter: 299.735 fsec
Residual FM: 1.1276 kHz
```

Packaging Mechanical: 16-Pin TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/24/16

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L16)

DOCUMENT CONTROL #: PD-1310

REVISION: G

16-0061

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6LC48H02LIE	L	16-pin, 173mil Wide (TSSOP)	Industrial
PI6LC48H02LIEX	L	16-pin, 173mil Wide (TSSOP), Tape & Reel	Industrial

Notes:

- **Thermal characteristics can be found on the company web site at** www.Diodes.com/packaging/
- **"E" denotes Pb-free and Green**
- **Adding an "X" at the end of the ordering code denotes tape and reel packaging**

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