

## Features

- High Performance, Low Power AVR<sup>®</sup> 8-Bit Microcontroller
- Advanced RISC Architecture
  - 125 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
- Non-volatile Program and Data Memories
  - 8K/16K/32K Bytes of In-System Self-Programmable Flash
  - 512/512/1024 EEPROM
  - 512/512/1024 Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/ 100,000 EEPROM
  - Data retention: 20 years at 85°C/ 100 years at 25°C<sup>(1)</sup>
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by on-chip Boot Program hardware-activated after reset
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- USB 2.0 Full-speed Device Module with Interrupt on Transfer Completion
  - Complies fully with Universal Serial Bus Specification REV 2.0
  - 48 MHz PLL for Full-speed Bus Operation : data transfer rates at 12 Mbit/s
  - Fully independent 176 bytes USB DPRAM for endpoint memory allocation
  - Endpoint 0 for Control Transfers: from 8 up to 64-bytes
  - 4 Programmable Endpoints:
    - IN or Out Directions
    - Bulk, Interrupt and Isochronous Transfers
    - Programmable maximum packet size from 8 to 64 bytes
    - Programmable single or double buffer
  - Suspend/Resume Interrupts
  - Microcontroller reset on USB Bus Reset without detach
  - USB Bus Disconnection on Microcontroller Request
- Peripheral Features
  - One 8-bit Timer/Counters with Separate Prescaler and Compare Mode (two 8-bit PWM channels)
  - One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Mode (three 8-bit PWM channels)
  - USART with SPI master only mode and hardware flow control (RTS/CTS)
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- On Chip Debug Interface (debugWIRE)
- Special Microcontroller Features
  - Power-On Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 22 Programmable I/O Lines
  - QFN32 (5x5mm) / TQFP32 packages
- Operating Voltages
  - 2.7 - 5.5V
- Operating temperature
  - Industrial (-40°C to +85°C)
- Maximum Frequency
  - 8 MHz at 2.7V - Industrial range
  - 16 MHz at 4.5V - Industrial range

Note: 1. See “Data Retention” on page 6 for details.



**8-bit AVR<sup>®</sup>**  
**Microcontroller**  
**with**  
**8/16/32K Bytes**  
**of ISP Flash**  
**and USB**  
**Controller**

**ATmega8U2**

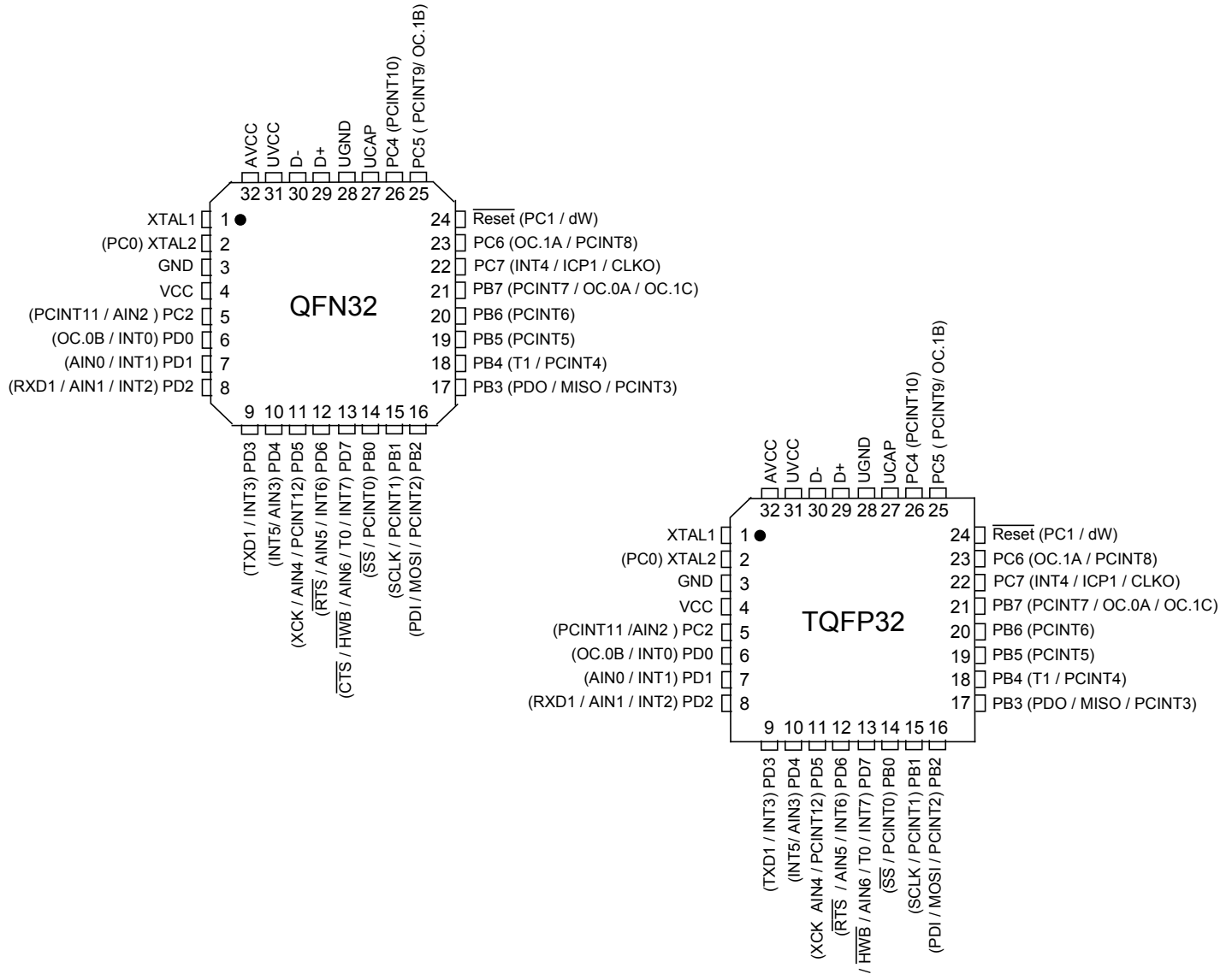
**ATmega16U2**

**ATmega32U2**



## 1. Pin Configurations

Figure 1-1. Pinout



Note: The large center pad underneath the QFN package should be soldered to ground on the board to ensure good mechanical stability.

### 1.1 Disclaimer

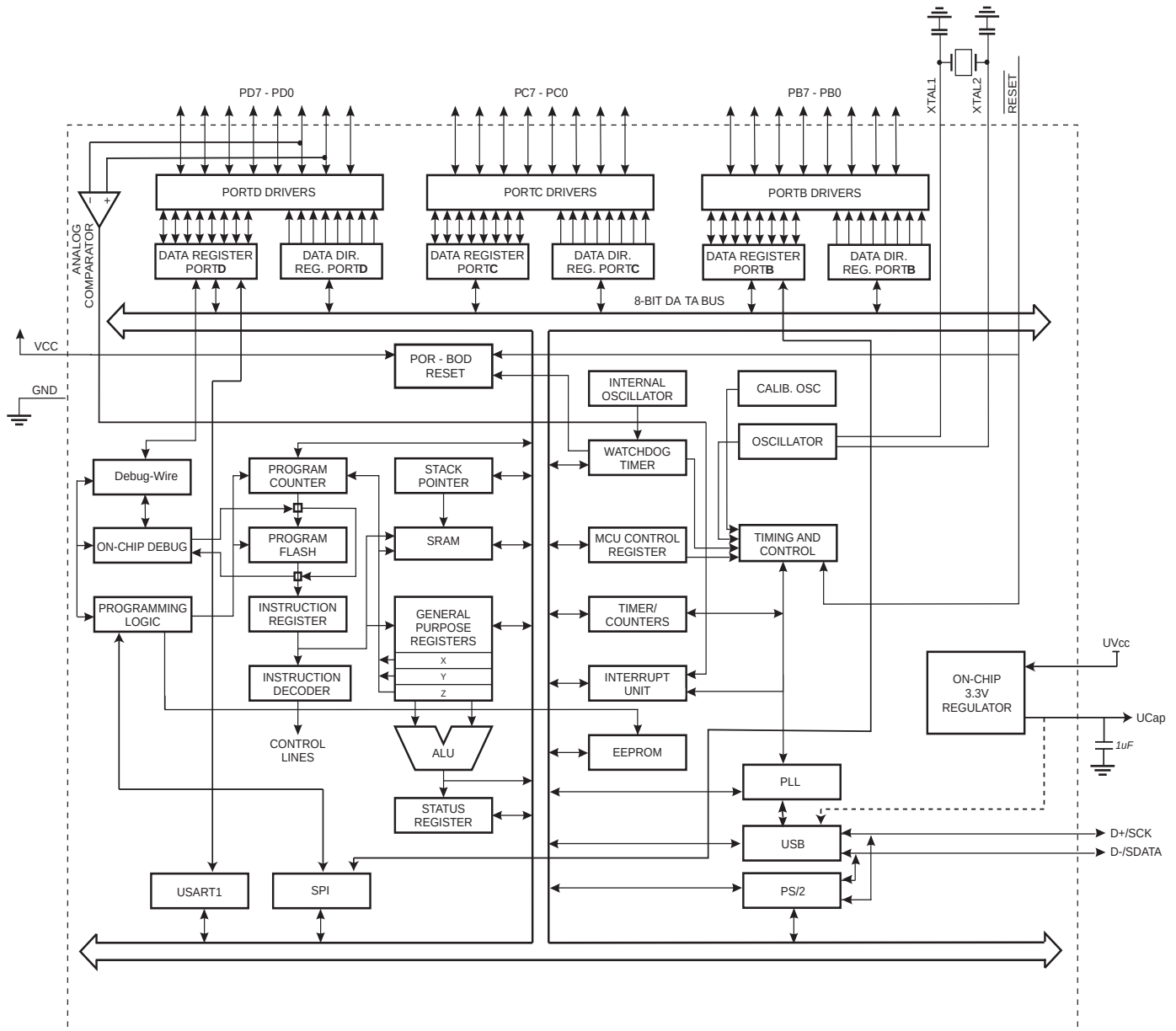
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## 2. Overview

The ATmega8U2/16U2/32U2 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8U2/16U2/32U2 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### 2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting

architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8U2/16U2/32U2 provides the following features: 8K/16K/32K Bytes of In-System Programmable Flash with Read-While-Write capabilities, 512/512/1024 Bytes EEPROM, 512/512/1024 SRAM, 22 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes and PWM, one USART, a programmable Watch-dog Timer with Internal Oscillator, an SPI serial port, debugWIRE interface, also used for accessing the On-chip Debug system and programming and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, the main Oscillator continues to run.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The on-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an on-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8U2/16U2/32U2 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8U2/16U2/32U2 are supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

## 2.2 Pin Descriptions

### 2.2.1 VCC

Digital supply voltage.

### 2.2.2 GND

Ground.

### 2.2.3 AVCC

AVCC is the supply voltage pin (input) for all analog features (Analog Comparator, PLL). It should be externally connected to VCC through a low-pass filter.

### 2.2.4 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega8U2/16U2/32U2 as listed on [page 74](#).

## 2.2.5 Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of various special features of the ATmega8U2/16U2/32U2 as listed on [page 77](#).

## 2.2.6 Port D (PD7..PD0)

Port D serves as analog inputs to the analog comparator.

Port D also serves as an 8-bit bi-directional I/O port, if the analog comparator is not used (concerns PD2/PD1 pins). Port pins can provide internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

## 2.2.7 D-

USB Full Speed Negative Data Upstream Port

## 2.2.8 D+

USB Full Speed Positive Data Upstream Port

## 2.2.9 UGND

USB Ground.

## 2.2.10 UVCC

USB Pads Internal Regulator Input supply voltage.

## 2.2.11 UCAP

USB Pads Internal Regulator Output supply voltage. Should be connected to an external capacitor (1 $\mu$ F).

## 2.2.12 RESET/PC1/dW

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in “[System Control and Reset](#)” on [page 47](#). Shorter pulses are not guaranteed to generate a reset. This pin alternatively serves as debugWire channel or as generic I/O. The configuration depends on the fuses RST-DISBL and DWEN.

## 2.2.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

## 2.2.14 XTAL2/PC0

Output from the inverting Oscillator amplifier if enabled by Fuse. Also serves as a generic I/O.

### **3. Resources**

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

### **4. Code Examples**

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

### **5. Data Retention**

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

## 6. Register Summary

| Address | Name     | Bit 7                              | Bit 6     | Bit 5    | Bit 4    | Bit 3                               | Bit 2    | Bit 1      | Bit 0    | Page     |          |          |
|---------|----------|------------------------------------|-----------|----------|----------|-------------------------------------|----------|------------|----------|----------|----------|----------|
| (0xFF)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xFE)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xFD)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xFC)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xFB)  | UPOE     | UPWE1                              | UPWE0     | UPDRV1   | UPDRV0   | SCKI                                | DATAI    | DPI        | DMI      | page 195 |          |          |
| (0xFA)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF9)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF8)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF7)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF6)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF5)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF4)  | UEINT    | -                                  | -         | -        | EPINT4:0 |                                     |          |            |          |          | page 222 |          |
| (0xF3)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xF2)  | UEBCLX   | BYCT7:0                            |           |          |          |                                     |          |            |          |          | page 221 |          |
| (0xF1)  | UEDATX   | DAT7:0                             |           |          |          |                                     |          |            |          |          | page 221 |          |
| (0xF0)  | UEIENX   | FLERRE                             | NAKINE    | -        | NAKOUTE  | RXSTPE                              | RXOUTE   | STALLEDE   | TXINE    | page 220 |          |          |
| (0xEF)  | UESTA1X  | -                                  | -         | -        | -        | -                                   | CTRLDIR  | CURRBK1:0  |          | page 218 |          |          |
| (0xEE)  | UESTA0X  | CFGOK                              | OVERFI    | UNDERFI  | -        | DTSEQ1:0                            |          | NBUSYBK1:0 |          | page 217 |          |          |
| (0xED)  | UECFG1X  | -                                  | EPSIZE2:0 |          |          | EPBK1:0                             |          | ALLOC      | -        | page 216 |          |          |
| (0xEC)  | UECFG0X  | EPTYPE1:0                          |           | -        | -        | -                                   | -        | -          | EPDIR    | page 215 |          |          |
| (0xEB)  | UECONX   | -                                  | -         | STALLRQ  | STALLRQC | RSTDT                               | -        | -          | EPEN     | page 214 |          |          |
| (0xEA)  | UERST    | -                                  | -         | -        | EPRST4:0 |                                     |          |            |          |          | page 214 |          |
| (0xE9)  | UENUM    | -                                  | -         | -        | -        | -                                   | EPNUM2:0 |            |          | page 214 |          |          |
| (0xE8)  | UEINTX   | FIFOCON                            | NAKINI    | RWAL     | NAKOUTI  | RXSTPI                              | RXOUTI   | STALLEDI   | TXINI    | page 219 |          |          |
| (0xE7)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xE6)  | UDMFN    | -                                  | -         | -        | FNCERR   | -                                   | -        | -          | -        | page 213 |          |          |
| (0xE5)  | UDFNUMH  | -                                  | -         | -        | -        | -                                   | FNUM10:8 |            |          | page 213 |          |          |
| (0xE4)  | UDFNUML  | FNUM7:0                            |           |          |          |                                     |          |            |          |          | page 213 |          |
| (0xE3)  | UDADDR   | ADDEN                              | UADD6:0   |          |          |                                     |          |            |          |          |          | page 212 |
| (0xE2)  | UDIEN    | -                                  | UPRSME    | EORSME   | WAKEUPE  | EORSTE                              | SOFE     | -          | SUSPE    | page 211 |          |          |
| (0xE1)  | UDINT    | -                                  | UPRSMI    | EORSMI   | WAKEUPI  | EORSTI                              | SOFI     | -          | SUSPI    | page 210 |          |          |
| (0xE0)  | UDCON    | -                                  | -         | -        | RPUTX    | -                                   | RSTCPU   | RMWKUP     | DETACH   | page 209 |          |          |
| (0xDF)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xDE)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xDD)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xDC)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xDB)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xDA)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD9)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD8)  | USBCON   | USBE                               | -         | FRZCLK   | -        | -                                   | -        | -          | -        | page 195 |          |          |
| (0xD7)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD6)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD5)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD4)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD3)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xD2)  | CLKSTA   | -                                  | -         | -        | -        | -                                   | -        | RCON       | EXTON    | page 38  |          |          |
| (0xD1)  | CLKSEL1  | RCCKSEL3                           | RCCKSEL2  | RCCKSEL1 | RCCKSEL0 | EXCKSEL3                            | EXCKSEL2 | EXCKSEL1   | EXCKSEL0 | page 38  |          |          |
| (0xD0)  | CLKSEL0  | RCSUT1                             | RCSUT0    | EXSUT1   | EXSUT0   | RCE                                 | EXTE     | -          | CLKS     | page 37  |          |          |
| (0xCF)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xCE)  | UDR1     | USART1 I/O Data Register           |           |          |          |                                     |          |            |          |          | page 167 |          |
| (0xCD)  | UBRR1H   | -                                  | -         | -        | -        | USART1 Baud Rate Register High Byte |          |            |          |          | page 171 |          |
| (0xCC)  | UBRR1L   | USART1 Baud Rate Register Low Byte |           |          |          |                                     |          |            |          |          | page 171 |          |
| (0xCB)  | UCSR1D   | -                                  | -         | -        | -        | -                                   | -        | CTSEN      | RTSEN    | page 171 |          |          |
| (0xCA)  | UCSR1C   | UMSEL11                            | UMSEL10   | UPM11    | UPM10    | USBS1                               | UCSZ11   | UCSZ10     | UCPOL1   | page 169 |          |          |
| (0xC9)  | UCSR1B   | RXCIE1                             | TXCIE1    | UDRIE1   | RXEN1    | TXEN1                               | UCSZ12   | RXB81      | TXB81    | page 168 |          |          |
| (0xC8)  | UCSR1A   | RXC1                               | TXC1      | UDRE1    | FE1      | DOR1                                | PE1      | U2X1       | MPCM1    | page 167 |          |          |
| (0xC7)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC6)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC5)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC4)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC3)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC2)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC1)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xC0)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |
| (0xBF)  | Reserved | -                                  | -         | -        | -        | -                                   | -        | -          | -        |          |          |          |

| Address | Name     | Bit 7                                                | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1 | Bit 0 | Page                     |
|---------|----------|------------------------------------------------------|--------|--------|--------|--------|--------|-------|-------|--------------------------|
| (0xBE)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xBD)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xBC)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xBB)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xBA)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB9)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB8)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB7)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB6)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB5)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB4)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB3)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB2)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB1)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xB0)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xAF)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xAE)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xAD)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xAC)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xAB)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xAA)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA9)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA8)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA7)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA6)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA5)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA4)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA3)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA2)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA1)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0xA0)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x9F)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x9E)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x9D)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x9C)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x9B)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x9A)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x99)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x98)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x97)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x96)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x95)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x94)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x93)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x92)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x91)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x90)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x8F)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x8E)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x8D)  | OCR1CH   | Timer/Counter1 - Output Compare Register C High Byte |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x8C)  | OCR1CL   | Timer/Counter1 - Output Compare Register C Low Byte  |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x8B)  | OCR1BH   | Timer/Counter1 - Output Compare Register B High Byte |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x8A)  | OCR1BL   | Timer/Counter1 - Output Compare Register B Low Byte  |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x89)  | OCR1AH   | Timer/Counter1 - Output Compare Register A High Byte |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x88)  | OCR1AL   | Timer/Counter1 - Output Compare Register A Low Byte  |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x87)  | ICR1H    | Timer/Counter1 - Input Capture Register High Byte    |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x86)  | ICR1L    | Timer/Counter1 - Input Capture Register Low Byte     |        |        |        |        |        |       |       | <a href="#">page 135</a> |
| (0x85)  | TCNT1H   | Timer/Counter1 - Counter Register High Byte          |        |        |        |        |        |       |       | <a href="#">page 134</a> |
| (0x84)  | TCNT1L   | Timer/Counter1 - Counter Register Low Byte           |        |        |        |        |        |       |       | <a href="#">page 134</a> |
| (0x83)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x82)  | TCCR1C   | FOC1A                                                | FOC1B  | FOC1C  | -      | -      | -      | -     | -     | <a href="#">page 134</a> |
| (0x81)  | TCCR1B   | ICNC1                                                | ICES1  | -      | WGM13  | WGM12  | CS12   | CS11  | CS10  | <a href="#">page 133</a> |
| (0x80)  | TCCR1A   | COM1A1                                               | COM1A0 | COM1B1 | COM1B0 | COM1C1 | COM1C0 | WGM11 | WGM10 | <a href="#">page 129</a> |
| (0x7F)  | DIDR1    | -                                                    | AIN6D  | AIN5D  | AIN4D  | AIN3D  | AIN2D  | AIN1D | AIN0D | <a href="#">page 225</a> |
| (0x7E)  | Reserved | -                                                    | -      | -      | -      | -      | -      | -     | -     |                          |
| (0x7D)  | ACMUX    | -                                                    | -      | -      | -      | -      | CMUX2  | CMUX1 | CMUX0 | <a href="#">page 225</a> |



| Address     | Name     | Bit 7                                    | Bit 6  | Bit 5    | Bit 4   | Bit 3                             | Bit 2   | Bit 1  | Bit 0    | Page                        |
|-------------|----------|------------------------------------------|--------|----------|---------|-----------------------------------|---------|--------|----------|-----------------------------|
| (0x7C)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x7B)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x7A)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x79)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x78)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x77)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x76)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x75)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x74)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x73)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x72)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x71)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x70)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x6F)      | TIMSK1   | -                                        | -      | ICIE1    | -       | OCIE1C                            | OCIE1B  | OCIE1A | TOIE1    | <a href="#">page 135</a>    |
| (0x6E)      | TIMSK0   | -                                        | -      | -        | -       | -                                 | OCIE0B  | OCIE0A | TOIE0    | <a href="#">page 106</a>    |
| (0x6D)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x6C)      | PCMSK1   | -                                        | -      | -        | PCINT12 | PCINT11                           | PCINT10 | PCINT9 | PCINT8   | <a href="#">page 87</a>     |
| (0x6B)      | PCMSK0   | PCINT7                                   | PCINT6 | PCINT5   | PCINT4  | PCINT3                            | PCINT2  | PCINT1 | PCINT0   | <a href="#">page 87</a>     |
| (0x6A)      | EICRB    | ISC71                                    | ISC70  | ISC61    | ISC60   | ISC51                             | ISC50   | ISC41  | ISC40    | <a href="#">page 85</a>     |
| (0x69)      | EICRA    | ISC31                                    | ISC30  | ISC21    | ISC20   | ISC11                             | ISC10   | ISC01  | ISC00    | <a href="#">page 84</a>     |
| (0x68)      | PCICR    | -                                        | -      | -        | -       | -                                 | -       | PCIE1  | PCIE0    | <a href="#">page 86</a>     |
| (0x67)      | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| (0x66)      | OSCCAL   | Oscillator Calibration Register          |        |          |         |                                   |         |        |          | <a href="#">page 38</a>     |
| (0x65)      | PRR1     | PRUSB                                    | -      | -        | -       | -                                 | -       | -      | PRUSART1 | <a href="#">page 46</a>     |
| (0x64)      | PRR0     | -                                        | -      | PRTIM0   | -       | PRTIM1                            | PRSPI   | -      | -        | <a href="#">page 46</a>     |
| (0x63)      | REGCR    | -                                        | -      | -        | -       | -                                 | -       | -      | REGDIS   | <a href="#">page 196</a>    |
| (0x62)      | WDTCKD   | -                                        | -      | WDEWIFCM | WCLKD2  | WDEWIF                            | WDEWIE  | WCLKD1 | WCLKD0   | <a href="#">page 57</a>     |
| (0x61)      | CLKPR    | CLKPCE                                   | -      | -        | -       | CLKPS3                            | CLKPS2  | CLKPS1 | CLKPS0   | <a href="#">page 39</a>     |
| (0x60)      | WDTCSR   | WDIF                                     | WDIE   | WDP3     | WDCE    | WDE                               | WDP2    | WDP1   | WDP0     | <a href="#">page 56</a>     |
| 0x3F (0x5F) | SREG     | I                                        | T      | H        | S       | V                                 | N       | Z      | C        | <a href="#">page 9</a>      |
| 0x3E (0x5E) | SPH      | SP15                                     | SP14   | SP13     | SP12    | SP11                              | SP10    | SP9    | SP8      | <a href="#">page 12</a>     |
| 0x3D (0x5D) | SPL      | SP7                                      | SP6    | SP5      | SP4     | SP3                               | SP2     | SP1    | SP0      | <a href="#">page 12</a>     |
| 0x3C (0x5C) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x3B (0x5B) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x3A (0x5A) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x39 (0x59) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x38 (0x58) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x37 (0x57) | SPMCSR   | SPMIE                                    | RWWSB  | SIGRD    | RWWSRE  | BLBSET                            | PGWRT   | PGERS  | SPMEN    | <a href="#">page 242</a>    |
| 0x36 (0x56) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x35 (0x55) | MCUCR    | -                                        | -      | -        | -       | -                                 | -       | IVSEL  | IVCE     | <a href="#">page 65, 82</a> |
| 0x34 (0x54) | MCUSR    | -                                        | -      | USBRF    | -       | WDRF                              | BORF    | EXTRF  | PORF     | <a href="#">page 55</a>     |
| 0x33 (0x53) | SMCR     | -                                        | -      | -        | -       | SM2                               | SM1     | SM0    | SE       | <a href="#">page 45</a>     |
| 0x32 (0x52) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x31 (0x51) | DWDR     | debugWIRE Data Register                  |        |          |         |                                   |         |        |          | <a href="#">page 245</a>    |
| 0x30 (0x50) | ACSR     | ACD                                      | ACBG   | ACO      | ACI     | ACIE                              | ACIC    | ACIS1  | ACIS0    | <a href="#">page 224</a>    |
| 0x2F (0x4F) | Reserved | -                                        | -      | -        | -       | -                                 | -       | -      | -        |                             |
| 0x2E (0x4E) | SPDR     | SPI Data Register                        |        |          |         |                                   |         |        |          | <a href="#">page 147</a>    |
| 0x2D (0x4D) | SPSR     | SPIF                                     | WCOL   | -        | -       | -                                 | -       | -      | SPI2X    | <a href="#">page 146</a>    |
| 0x2C (0x4C) | SPCR     | SPIE                                     | SPE    | DORD     | MSTR    | CPOL                              | CPHA    | SPR1   | SPR0     | <a href="#">page 145</a>    |
| 0x2B (0x4B) | GPOR2    | General Purpose I/O Register 2           |        |          |         |                                   |         |        |          | <a href="#">page 24</a>     |
| 0x2A (0x4A) | GPOR1    | General Purpose I/O Register 1           |        |          |         |                                   |         |        |          | <a href="#">page 24</a>     |
| 0x29 (0x49) | PLLCSR   | -                                        | -      | -        | PLL2    | PLL1                              | PLL0    | PLLE   | PLOCK    | <a href="#">page 40</a>     |
| 0x28 (0x48) | OCR0B    | Timer/Counter0 Output Compare Register B |        |          |         |                                   |         |        |          | <a href="#">page 106</a>    |
| 0x27 (0x47) | OCR0A    | Timer/Counter0 Output Compare Register A |        |          |         |                                   |         |        |          | <a href="#">page 106</a>    |
| 0x26 (0x46) | TCNT0    | Timer/Counter0 (8 Bit)                   |        |          |         |                                   |         |        |          | <a href="#">page 106</a>    |
| 0x25 (0x45) | TCCR0B   | FOC0A                                    | FOC0B  | -        | -       | WGM02                             | CS02    | CS01   | CS00     | <a href="#">page 105</a>    |
| 0x24 (0x44) | TCCR0A   | COM0A1                                   | COM0A0 | COM0B1   | COM0B0  | -                                 | -       | WGM01  | WGM00    | <a href="#">page 105</a>    |
| 0x23 (0x43) | GTCCR    | TSM                                      | -      | -        | -       | -                                 | -       | PSRASY | PSRSYNC  | <a href="#">page 89</a>     |
| 0x22 (0x42) | EEARH    | -                                        | -      | -        | -       | EEPROM Address Register High Byte |         |        |          | <a href="#">page 20</a>     |
| 0x21 (0x41) | EEARL    | EEPROM Address Register Low Byte         |        |          |         |                                   |         |        |          | <a href="#">page 20</a>     |
| 0x20 (0x40) | EEDR     | EEPROM Data Register                     |        |          |         |                                   |         |        |          | <a href="#">page 20</a>     |
| 0x1F (0x3F) | EECR     | -                                        | -      | EEP1     | EEP0    | EERIE                             | EEMPE   | EEPE   | EERE     | <a href="#">page 21</a>     |
| 0x1E (0x3E) | GPOR0    | General Purpose I/O Register 0           |        |          |         |                                   |         |        |          | <a href="#">page 25</a>     |
| 0x1D (0x3D) | EIMSK    | INT7                                     | INT6   | INT5     | INT4    | INT3                              | INT2    | INT1   | INT0     | <a href="#">page 86</a>     |
| 0x1C (0x3C) | EIFR     | INTF7                                    | INTF6  | INTF5    | INTF4   | INTF3                             | INTF2   | INTF1  | INTF0    | <a href="#">page 86</a>     |
| 0x1B (0x3B) | PCIFR    | -                                        | -      | -        | -       | -                                 | -       | PCIF1  | PCIF0    | <a href="#">page 86</a>     |

| Address     | Name     | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Page                     |
|-------------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------------------------|
| 0x1A (0x3A) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x19 (0x39) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x18 (0x38) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x17 (0x37) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x16 (0x36) | TIFR1    | -      | -      | ICF1   | -      | OCF1C  | OCF1B  | OCF1A  | TOV1   | <a href="#">page 136</a> |
| 0x15 (0x35) | TIFR0    | -      | -      | -      | -      | -      | OCF0B  | OCF0A  | TOV0   | <a href="#">page 107</a> |
| 0x14 (0x34) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x13 (0x33) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x12 (0x32) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x11 (0x31) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x10 (0x30) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x0F (0x2F) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x0E (0x2E) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x0D (0x2D) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x0C (0x2C) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x0B (0x2B) | PORTD    | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | <a href="#">page 83</a>  |
| 0x0A (0x2A) | DDRD     | DDD7   | DDD6   | DDD5   | DDD4   | DDD3   | DDD2   | DDD1   | DDD0   | <a href="#">page 83</a>  |
| 0x09 (0x29) | PIND     | PIND7  | PIND6  | PIND5  | PIND4  | PIND3  | PIND2  | PIND1  | PIND0  | <a href="#">page 83</a>  |
| 0x08 (0x28) | PORTC    | PORTC7 | PORTC6 | PORTC5 | PORTC4 | -      | PORTC2 | PORTC1 | PORTC0 | <a href="#">page 82</a>  |
| 0x07 (0x27) | DDRC     | DDC7   | DDC6   | DDC5   | DDC4   | -      | DDC2   | DDC1   | DDC0   | <a href="#">page 82</a>  |
| 0x06 (0x26) | PINC     | PINC7  | PINC6  | PINC5  | PINC4  | -      | PINC2  | PINC1  | PINC0  | <a href="#">page 82</a>  |
| 0x05 (0x25) | PORTB    | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | <a href="#">page 82</a>  |
| 0x04 (0x24) | DDRB     | DDB7   | DDB6   | DDB5   | DDB4   | DDB3   | DDB2   | DDB1   | DDB0   | <a href="#">page 82</a>  |
| 0x03 (0x23) | PINB     | PINB7  | PINB6  | PINB5  | PINB4  | PINB3  | PINB2  | PINB1  | PINB0  | <a href="#">page 82</a>  |
| 0x02 (0x22) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x01 (0x21) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |
| 0x00 (0x20) | Reserved | -      | -      | -      | -      | -      | -      | -      | -      |                          |

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Moreover reserved bits are not guaranteed to be read as "0". Reserved I/O memory addresses should never be written.
  2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
  4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses. The ATmega8U2/16U2/32U2 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 - \$1FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

## 7. Instruction Set Summary

| Mnemonics                         | Operands | Description                            | Operation                                             | Flags      | #Clocks |
|-----------------------------------|----------|----------------------------------------|-------------------------------------------------------|------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS |          |                                        |                                                       |            |         |
| ADD                               | Rd, Rr   | Add two Registers                      | $Rd \leftarrow Rd + Rr$                               | Z,C,N,V,H  | 1       |
| ADC                               | Rd, Rr   | Add with Carry two Registers           | $Rd \leftarrow Rd + Rr + C$                           | Z,C,N,V,H  | 1       |
| ADIW                              | RdI,K    | Add Immediate to Word                  | $Rdh:Rdl \leftarrow Rdh:Rdl + K$                      | Z,C,N,V,S  | 2       |
| SUB                               | Rd, Rr   | Subtract two Registers                 | $Rd \leftarrow Rd - Rr$                               | Z,C,N,V,H  | 1       |
| SUBI                              | Rd, K    | Subtract Constant from Register        | $Rd \leftarrow Rd - K$                                | Z,C,N,V,H  | 1       |
| SBC                               | Rd, Rr   | Subtract with Carry two Registers      | $Rd \leftarrow Rd - Rr - C$                           | Z,C,N,V,H  | 1       |
| SBCI                              | Rd, K    | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$                            | Z,C,N,V,H  | 1       |
| SBIW                              | RdI,K    | Subtract Immediate from Word           | $Rdh:Rdl \leftarrow Rdh:Rdl - K$                      | Z,C,N,V,S  | 2       |
| AND                               | Rd, Rr   | Logical AND Registers                  | $Rd \leftarrow Rd \bullet Rr$                         | Z,N,V      | 1       |
| ANDI                              | Rd, K    | Logical AND Register and Constant      | $Rd \leftarrow Rd \bullet K$                          | Z,N,V      | 1       |
| OR                                | Rd, Rr   | Logical OR Registers                   | $Rd \leftarrow Rd \vee Rr$                            | Z,N,V      | 1       |
| ORI                               | Rd, K    | Logical OR Register and Constant       | $Rd \leftarrow Rd \vee K$                             | Z,N,V      | 1       |
| EOR                               | Rd, Rr   | Exclusive OR Registers                 | $Rd \leftarrow Rd \oplus Rr$                          | Z,N,V      | 1       |
| COM                               | Rd       | One's Complement                       | $Rd \leftarrow 0xFF - Rd$                             | Z,C,N,V    | 1       |
| NEG                               | Rd       | Two's Complement                       | $Rd \leftarrow 0x00 - Rd$                             | Z,C,N,V,H  | 1       |
| SBR                               | Rd,K     | Set Bit(s) in Register                 | $Rd \leftarrow Rd \vee K$                             | Z,N,V      | 1       |
| CBR                               | Rd,K     | Clear Bit(s) in Register               | $Rd \leftarrow Rd \bullet (0xFF - K)$                 | Z,N,V      | 1       |
| INC                               | Rd       | Increment                              | $Rd \leftarrow Rd + 1$                                | Z,N,V      | 1       |
| DEC                               | Rd       | Decrement                              | $Rd \leftarrow Rd - 1$                                | Z,N,V      | 1       |
| TST                               | Rd       | Test for Zero or Minus                 | $Rd \leftarrow Rd \bullet Rd$                         | Z,N,V      | 1       |
| CLR                               | Rd       | Clear Register                         | $Rd \leftarrow Rd \oplus Rd$                          | Z,N,V      | 1       |
| SER                               | Rd       | Set Register                           | $Rd \leftarrow 0xFF$                                  | None       | 1       |
| BRANCH INSTRUCTIONS               |          |                                        |                                                       |            |         |
| RJMP                              | k        | Relative Jump                          | $PC \leftarrow PC + k + 1$                            | None       | 2       |
| IJMP                              |          | Indirect Jump to (Z)                   | $PC \leftarrow Z$                                     | None       | 2       |
| JMP                               | k        | Direct Jump                            | $PC \leftarrow k$                                     | None       | 3       |
| RCALL                             | k        | Relative Subroutine Call               | $PC \leftarrow PC + k + 1$                            | None       | 4       |
| ICALL                             |          | Indirect Call to (Z)                   | $PC \leftarrow Z$                                     | None       | 4       |
| CALL                              | k        | Direct Subroutine Call                 | $PC \leftarrow k$                                     | None       | 5       |
| RET                               |          | Subroutine Return                      | $PC \leftarrow STACK$                                 | None       | 5       |
| RETI                              |          | Interrupt Return                       | $PC \leftarrow STACK$                                 | I          | 5       |
| CPSE                              | Rd,Rr    | Compare, Skip if Equal                 | if (Rd = Rr) $PC \leftarrow PC + 2$ or 3              | None       | 1/2/3   |
| CP                                | Rd,Rr    | Compare                                | $Rd - Rr$                                             | Z, N,V,C,H | 1       |
| CPC                               | Rd,Rr    | Compare with Carry                     | $Rd - Rr - C$                                         | Z, N,V,C,H | 1       |
| CPI                               | Rd,K     | Compare Register with Immediate        | $Rd - K$                                              | Z, N,V,C,H | 1       |
| SBRC                              | Rr, b    | Skip if Bit in Register Cleared        | if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3              | None       | 1/2/3   |
| SBRs                              | Rr, b    | Skip if Bit in Register is Set         | if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3              | None       | 1/2/3   |
| SBIC                              | P, b     | Skip if Bit in I/O Register Cleared    | if (P(b)=0) $PC \leftarrow PC + 2$ or 3               | None       | 1/2/3   |
| SBIS                              | P, b     | Skip if Bit in I/O Register is Set     | if (P(b)=1) $PC \leftarrow PC + 2$ or 3               | None       | 1/2/3   |
| BRBS                              | s, k     | Branch if Status Flag Set              | if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$      | None       | 1/2     |
| BRBC                              | s, k     | Branch if Status Flag Cleared          | if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$      | None       | 1/2     |
| BREQ                              | k        | Branch if Equal                        | if (Z = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRNE                              | k        | Branch if Not Equal                    | if (Z = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRCS                              | k        | Branch if Carry Set                    | if (C = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRCC                              | k        | Branch if Carry Cleared                | if (C = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRSH                              | k        | Branch if Same or Higher               | if (C = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRLO                              | k        | Branch if Lower                        | if (C = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRMI                              | k        | Branch if Minus                        | if (N = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRPL                              | k        | Branch if Plus                         | if (N = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRGE                              | k        | Branch if Greater or Equal, Signed     | if (N $\oplus$ V = 0) then $PC \leftarrow PC + k + 1$ | None       | 1/2     |
| BRLT                              | k        | Branch if Less Than Zero, Signed       | if (N $\oplus$ V = 1) then $PC \leftarrow PC + k + 1$ | None       | 1/2     |
| BRHS                              | k        | Branch if Half Carry Flag Set          | if (H = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRHC                              | k        | Branch if Half Carry Flag Cleared      | if (H = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRTS                              | k        | Branch if T Flag Set                   | if (T = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRTC                              | k        | Branch if T Flag Cleared               | if (T = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRVS                              | k        | Branch if Overflow Flag is Set         | if (V = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRVC                              | k        | Branch if Overflow Flag is Cleared     | if (V = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRIE                              | k        | Branch if Interrupt Enabled            | if (I = 1) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BRID                              | k        | Branch if Interrupt Disabled           | if (I = 0) then $PC \leftarrow PC + k + 1$            | None       | 1/2     |
| BIT AND BIT-TEST INSTRUCTIONS     |          |                                        |                                                       |            |         |
| SBI                               | P,b      | Set Bit in I/O Register                | $I/O(P,b) \leftarrow 1$                               | None       | 2       |
| CBI                               | P,b      | Clear Bit in I/O Register              | $I/O(P,b) \leftarrow 0$                               | None       | 2       |
| LSL                               | Rd       | Logical Shift Left                     | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$        | Z,C,N,V    | 1       |
| LSR                               | Rd       | Logical Shift Right                    | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$        | Z,C,N,V    | 1       |

| Mnemonics                  | Operands | Description                      | Operation                                                              | Flags      | #Clocks |
|----------------------------|----------|----------------------------------|------------------------------------------------------------------------|------------|---------|
| ROL                        | Rd       | Rotate Left Through Carry        | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$     | Z, C, N, V | 1       |
| ROR                        | Rd       | Rotate Right Through Carry       | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$     | Z, C, N, V | 1       |
| ASR                        | Rd       | Arithmetic Shift Right           | $Rd(n) \leftarrow Rd(n+1), n=0..6$                                     | Z, C, N, V | 1       |
| SWAP                       | Rd       | Swap Nibbles                     | $Rd(3..0) \leftrightarrow Rd(7..4), Rd(7..4) \leftrightarrow Rd(3..0)$ | None       | 1       |
| BSET                       | s        | Flag Set                         | $SREG(s) \leftarrow 1$                                                 | SREG(s)    | 1       |
| BCLR                       | s        | Flag Clear                       | $SREG(s) \leftarrow 0$                                                 | SREG(s)    | 1       |
| BST                        | Rr, b    | Bit Store from Register to T     | $T \leftarrow Rr(b)$                                                   | T          | 1       |
| BLD                        | Rd, b    | Bit load from T to Register      | $Rd(b) \leftarrow T$                                                   | None       | 1       |
| SEC                        |          | Set Carry                        | $C \leftarrow 1$                                                       | C          | 1       |
| CLC                        |          | Clear Carry                      | $C \leftarrow 0$                                                       | C          | 1       |
| SEN                        |          | Set Negative Flag                | $N \leftarrow 1$                                                       | N          | 1       |
| CLN                        |          | Clear Negative Flag              | $N \leftarrow 0$                                                       | N          | 1       |
| SEZ                        |          | Set Zero Flag                    | $Z \leftarrow 1$                                                       | Z          | 1       |
| CLZ                        |          | Clear Zero Flag                  | $Z \leftarrow 0$                                                       | Z          | 1       |
| SEI                        |          | Global Interrupt Enable          | $I \leftarrow 1$                                                       | I          | 1       |
| CLI                        |          | Global Interrupt Disable         | $I \leftarrow 0$                                                       | I          | 1       |
| SES                        |          | Set Signed Test Flag             | $S \leftarrow 1$                                                       | S          | 1       |
| CLS                        |          | Clear Signed Test Flag           | $S \leftarrow 0$                                                       | S          | 1       |
| SEV                        |          | Set Twos Complement Overflow     | $V \leftarrow 1$                                                       | V          | 1       |
| CLV                        |          | Clear Twos Complement Overflow   | $V \leftarrow 0$                                                       | V          | 1       |
| SET                        |          | Set T in SREG                    | $T \leftarrow 1$                                                       | T          | 1       |
| CLT                        |          | Clear T in SREG                  | $T \leftarrow 0$                                                       | T          | 1       |
| SEH                        |          | Set Half Carry Flag in SREG      | $H \leftarrow 1$                                                       | H          | 1       |
| CLH                        |          | Clear Half Carry Flag in SREG    | $H \leftarrow 0$                                                       | H          | 1       |
| DATA TRANSFER INSTRUCTIONS |          |                                  |                                                                        |            |         |
| MOV                        | Rd, Rr   | Move Between Registers           | $Rd \leftarrow Rr$                                                     | None       | 1       |
| MOVW                       | Rd, Rr   | Copy Register Word               | $Rd+1:Rd \leftarrow Rr+1:Rr$                                           | None       | 1       |
| LDI                        | Rd, K    | Load Immediate                   | $Rd \leftarrow K$                                                      | None       | 1       |
| LD                         | Rd, X    | Load Indirect                    | $Rd \leftarrow (X)$                                                    | None       | 2       |
| LD                         | Rd, X+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (X), X \leftarrow X + 1$                                | None       | 2       |
| LD                         | Rd, -X   | Load Indirect and Pre-Dec.       | $X \leftarrow X - 1, Rd \leftarrow (X)$                                | None       | 2       |
| LD                         | Rd, Y    | Load Indirect                    | $Rd \leftarrow (Y)$                                                    | None       | 2       |
| LD                         | Rd, Y+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (Y), Y \leftarrow Y + 1$                                | None       | 2       |
| LD                         | Rd, -Y   | Load Indirect and Pre-Dec.       | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$                                | None       | 2       |
| LDD                        | Rd, Y+q  | Load Indirect with Displacement  | $Rd \leftarrow (Y + q)$                                                | None       | 2       |
| LD                         | Rd, Z    | Load Indirect                    | $Rd \leftarrow (Z)$                                                    | None       | 2       |
| LD                         | Rd, Z+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (Z), Z \leftarrow Z + 1$                                | None       | 2       |
| LD                         | Rd, -Z   | Load Indirect and Pre-Dec.       | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$                                | None       | 2       |
| LDD                        | Rd, Z+q  | Load Indirect with Displacement  | $Rd \leftarrow (Z + q)$                                                | None       | 2       |
| LDS                        | Rd, k    | Load Direct from SRAM            | $Rd \leftarrow (k)$                                                    | None       | 2       |
| ST                         | X, Rr    | Store Indirect                   | $(X) \leftarrow Rr$                                                    | None       | 2       |
| ST                         | X+, Rr   | Store Indirect and Post-Inc.     | $(X) \leftarrow Rr, X \leftarrow X + 1$                                | None       | 2       |
| ST                         | -X, Rr   | Store Indirect and Pre-Dec.      | $X \leftarrow X - 1, (X) \leftarrow Rr$                                | None       | 2       |
| ST                         | Y, Rr    | Store Indirect                   | $(Y) \leftarrow Rr$                                                    | None       | 2       |
| ST                         | Y+, Rr   | Store Indirect and Post-Inc.     | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$                                | None       | 2       |
| ST                         | -Y, Rr   | Store Indirect and Pre-Dec.      | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$                                | None       | 2       |
| STD                        | Y+q, Rr  | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$                                                | None       | 2       |
| ST                         | Z, Rr    | Store Indirect                   | $(Z) \leftarrow Rr$                                                    | None       | 2       |
| ST                         | Z+, Rr   | Store Indirect and Post-Inc.     | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$                                | None       | 2       |
| ST                         | -Z, Rr   | Store Indirect and Pre-Dec.      | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$                                | None       | 2       |
| STD                        | Z+q, Rr  | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$                                                | None       | 2       |
| STS                        | k, Rr    | Store Direct to SRAM             | $(k) \leftarrow Rr$                                                    | None       | 2       |
| LPM                        |          | Load Program Memory              | $R0 \leftarrow (Z)$                                                    | None       | 3       |
| LPM                        | Rd, Z    | Load Program Memory              | $Rd \leftarrow (Z)$                                                    | None       | 3       |
| LPM                        | Rd, Z+   | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$                                | None       | 3       |
| SPM                        |          | Store Program Memory             | $(Z) \leftarrow R1:R0$                                                 | None       | -       |
| IN                         | Rd, P    | In Port                          | $Rd \leftarrow P$                                                      | None       | 1       |
| OUT                        | P, Rr    | Out Port                         | $P \leftarrow Rr$                                                      | None       | 1       |
| PUSH                       | Rr       | Push Register on Stack           | $STACK \leftarrow Rr$                                                  | None       | 2       |
| POP                        | Rd       | Pop Register from Stack          | $Rd \leftarrow STACK$                                                  | None       | 2       |
| MCU CONTROL INSTRUCTIONS   |          |                                  |                                                                        |            |         |
| NOP                        |          | No Operation                     |                                                                        | None       | 1       |
| SLEEP                      |          | Sleep                            | (see specific descr. for Sleep function)                               | None       | 1       |
| WDR                        |          | Watchdog Reset                   | (see specific descr. for WDR/timer)                                    | None       | 1       |
| BREAK                      |          | Break                            | For On-chip Debug Only                                                 | None       | N/A     |

## 8. Ordering Information

### 8.1 ATmega8U2

| Speed  | Power Supply | Ordering Code | Package | Operational Range |
|--------|--------------|---------------|---------|-------------------|
| 16 MHz | 2.7 - 5.5V   | ATmega8U2-AU  | 32A     | -40°C to +85°C    |
|        |              | ATmega8U2-MU  | 32M1-A  |                   |

| Package Type |                                                                      |
|--------------|----------------------------------------------------------------------|
| <b>32A</b>   | 32-lead, 7 x7 x 1.2 mm, lead pitch 0.8 mm Thin Quad Flat Package     |
| <b>32M1</b>  | 32-pad, 5 x 5 x 1 mm body, pad pitch 0.50 mm Quad Flat No lead (QFN) |

## 8.2 ATmega16U2

| Speed  | Power Supply | Ordering Code | Package | Operational Range |
|--------|--------------|---------------|---------|-------------------|
| 16 MHz | 2.7 - 5.5V   | ATmega16U2-AU | 32A     | -40°C to +85°C    |
|        |              | ATmega16U2-MU | 32M1-A  |                   |

| Package Type |                                                                      |
|--------------|----------------------------------------------------------------------|
| <b>32A</b>   | 32-lead, 7 x7 x 1.2 mm, lead pitch 0.8 mm Thin Quad Flat Package     |
| <b>32M1</b>  | 32-pad, 5 x 5 x 1 mm body, pad pitch 0.50 mm Quad Flat No lead (QFN) |

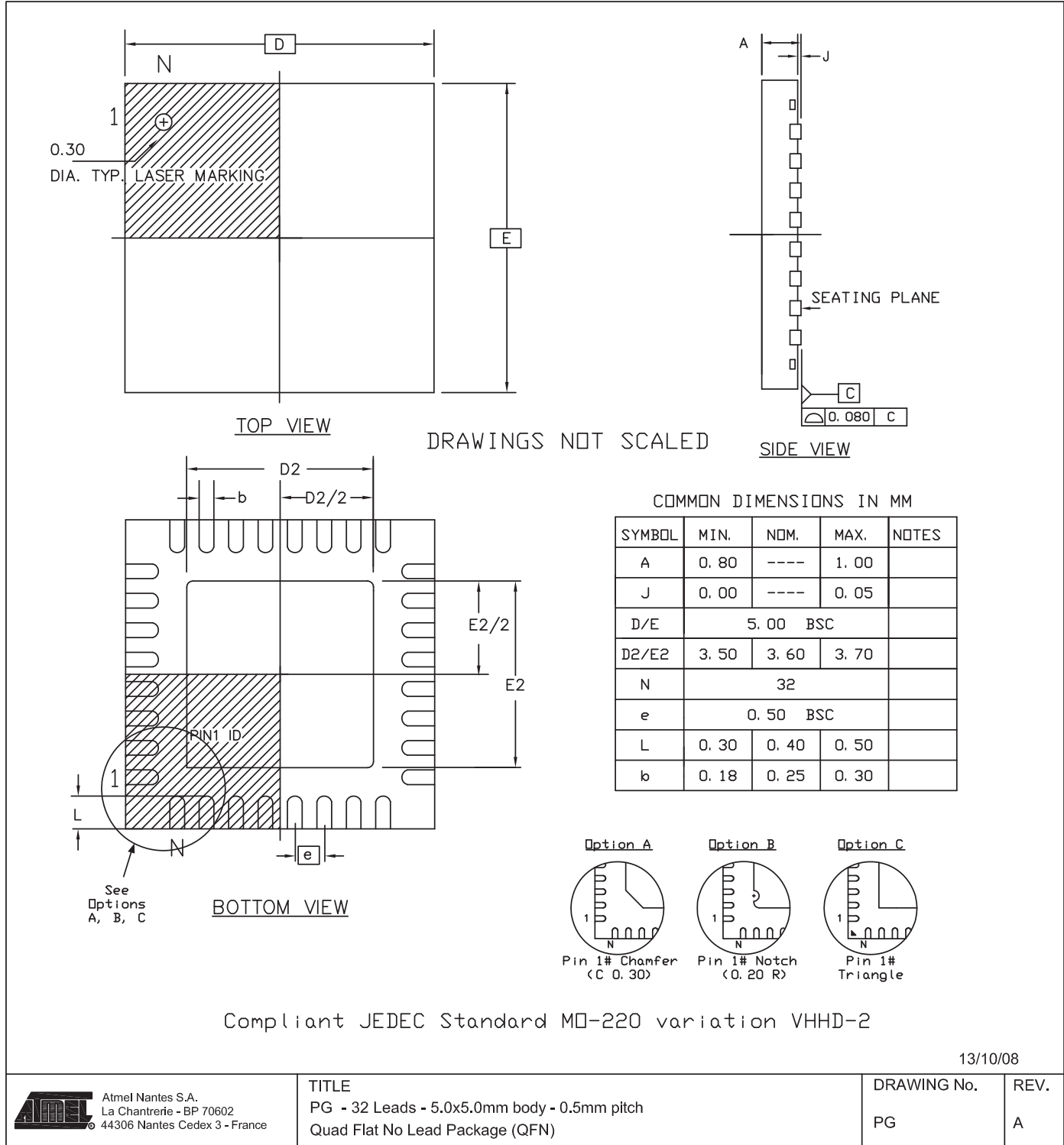
## 8.3 ATmega32U2

| Speed  | Power Supply | Ordering Code | Package | Operational Range |
|--------|--------------|---------------|---------|-------------------|
| 16 MHz | 2.7 - 5.5V   | ATmega32U2-AU | 32A     | -40°C to +85°C    |
|        |              | ATmega32U2-MU | 32M1-A  |                   |

| Package Type |                                                                      |
|--------------|----------------------------------------------------------------------|
| <b>32A</b>   | 32-lead, 7 x7 x 1.2 mm, lead pitch 0.8 mm Thin Quad Flat Package     |
| <b>32M1</b>  | 32-pad, 5 x 5 x 1 mm body, pad pitch 0.50 mm Quad Flat No lead (QFN) |

## 9. Packaging Information

### 9.1 QFN32







## **10. Errata**

### **10.1 Errata ATmega8U2**

The revision letter in this section refers to the revision of the ATmega8U2 device.

#### **10.1.1 rev. A and rev B**

- **Full Swing oscillator**

##### **1. Full Swing oscillator**

The maximum frequency for the Full Swing Crystal Oscillator is 8MHz. For Crystal frequencies > 8MHz the Full Swing Crystal Oscillator is not guaranteed to operate correctly.

##### **Problem fix/Workaround**

If a Crystal with frequency > 8MHz is used, the Low Power Crystal Oscillator option should be used instead. See table 8-1 for an overview of the Device Clocking Options. Note that the Low Power Crystal Oscillator will not provide full rail-to-rail swing on the XTAL2 pin. If system clock output is needed to drive other clock inputs while running from the Low Power Crystal Oscillator, the system clock can be output on PORTC7 by programming the CKOUT fuse.

### **10.2 Errata ATmega16U2**

The revision letter in this section refers to the revision of the ATmega16U2 device.

#### **10.2.1 rev. A and rev B**

- **Full Swing oscillator**

##### **1. Full Swing oscillator**

The maximum frequency for the Full Swing Crystal Oscillator is 8MHz. For Crystal frequencies > 8MHz the Full Swing Crystal Oscillator is not guaranteed to operate correctly.

##### **Problem fix/Workaround**

If a Crystal with frequency > 8MHz is used, the Low Power Crystal Oscillator option should be used instead. See table 8-1 for an overview of the Device Clocking Options. Note that the Low Power Crystal Oscillator will not provide full rail-to-rail swing on the XTAL2 pin. If system clock output is needed to drive other clock inputs while running from the Low Power Crystal Oscillator, the system clock can be output on PORTC7 by programming the CKOUT fuse.

### **10.3 Errata ATmega32U2**

The revision letter in this section refers to the revision of the ATmega32U2 device.

#### **10.3.1 rev. C**

No Known Errata

### 10.3.2 rev. A and rev B

- **Full Swing oscillator**

#### 1. Full Swing oscillator

The maximum frequency for the Full Swing Crystal Oscillator is 8MHz. For Crystal frequencies > 8MHz the Full Swing Crystal Oscillator is not guaranteed to operate correctly.

##### **Problem fix/Workaround**

If a Crystal with frequency > 8MHz is used, the Low Power Crystal Oscillator option should be used instead. See table 8-1 for an overview of the Device Clocking Options. Note that the Low Power Crystal Oscillator will not provide full rail-to-rail swing on the XTAL2 pin. If system clock output is needed to drive other clock inputs while running from the Low Power Crystal Oscillator, the system clock can be output on PORTC7 by programming the CKOUT fuse.

## 11. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

### 11.1 Rev.7799E – 09/12

1. Renamed package name in [Figure 1-1 on page 2](#) from VQFP32 to TQFP32.
2. Corrected typos.

### 11.2 Rev. 7799D – 11/10

1. Updated the footnote on page 2. Removed the VQFP from the footnote
2. Updated [Section 20-4 "Typical Bus powered application with 3.3V I/O" on page 187](#).
3. Updated [Figure 20-6 on page 188](#). By connecting UVCC to 3V power-supply.
4. Updated [Table 21-2 on page 215](#). 10: Bulk Type, and 01: Isochronous Type
5. Added UVCC limits in Electrical Characteristics
6. Updated ["Electrical Characteristics" on page 264](#). Added USB D+ Internal Pull-up (streaming mode)
7. Updated ["Register Summary" on page 7](#). Added DIDR1 (adress: 0x7F)
8. Removed Figure 27-26: USB Regulator Consumption with load 75Ω vs. Vcc

### 11.3 Rev. 7799C – 12/09

1. Updated ["Features" on page 1](#).
2. Added description of ["AVCC" on page 4](#).
3. Updated [Figure 7-2 on page 18](#).
4. Updated [Figure 20-3 on page 186](#) and [Figure 20-4 on page 187](#).
5. Updated ["Fuse Bits" on page 247](#).
6. Updated ["DC Characteristics" on page 264](#).
7. Updated [Table 26-3 on page 267](#), by removing Vrst.
8. Updated [Table 26-4 on page 268](#).
9. Updated ["Typical Characteristics" on page 273](#).
10. Added new ["Errata" on page 18](#).

### 11.4 Rev. 7799B – 06/09

1. Updated ["Typical Characteristics" on page 273](#).

## 11.5 Rev. 7799A – 03/09

1. Initial revision.

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