

OptiMOS[®] 2 Power-Transistor

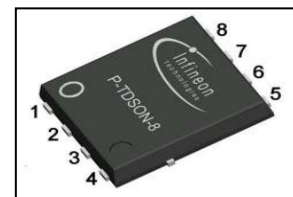
Features

- Fast switching MOSFET for SMPS
- Optimized technology for notebook DC/DC converters
- Qualified according to JEDEC¹ for target applications
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- Avalanche rated
- dv/dt rated

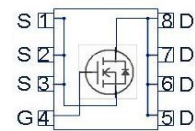
Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	2.2	m Ω
I_D	50	A

P-TDSON-8



Type	Package	Ordering Code	Marking
BSC022N03S	P-TDSON-8	Q67042-S4218	22N03S



Maximum ratings, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ }^{\circ}\text{C}$	50	A
		$T_C=100\text{ }^{\circ}\text{C}$	50	
		$T_A=25\text{ }^{\circ}\text{C}$, $R_{thJA}=45\text{ K/W}^{(2)}$	28	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ }^{\circ}\text{C}^{(3)}$	200	
Avalanche energy, single pulse	E_{AS}	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$	800	mJ
Reverse diode dv/dt	dv/dt	$I_D=50\text{ A}$, $V_{DS}=24\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ }^{\circ}\text{C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ }^{\circ}\text{C}$	104	W
		$T_A=25\text{ }^{\circ}\text{C}$, $R_{thJA}=45\text{ K/W}^{(2)}$	2.8	
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.2	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ²⁾	-	-	45	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=100\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=50\text{ A}$	-	2.6	3.3	m Ω
		$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	1.8	2.2	
Gate resistance	R_G		0.3	0.6	1.2	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=50\text{ A}$	70	140	-	S

¹⁾ J-STD20 and JESD22

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	5630	7490	pF
Output capacitance	C_{oss}		-	2000	2660	
Reverse transfer capacitance	C_{rss}		-	251	376	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=2.7\ \Omega$	-	9.7	14	ns
Rise time	t_r		-	9	13	
Turn-off delay time	$t_{d(off)}$		-	42	62	
Fall time	t_f		-	7	11	

Gate Charge Characteristics⁴⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=25\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	16	21	nC
Gate charge at threshold	$Q_{g(th)}$		-	9	12	
Gate to drain charge	Q_{gd}		-	11	16	
Switching charge	Q_{sw}		-	17	25	
Gate charge total	Q_g		-	43	58	
Gate plateau voltage	$V_{plateau}$		-	2.8	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	38	51	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	48	63	

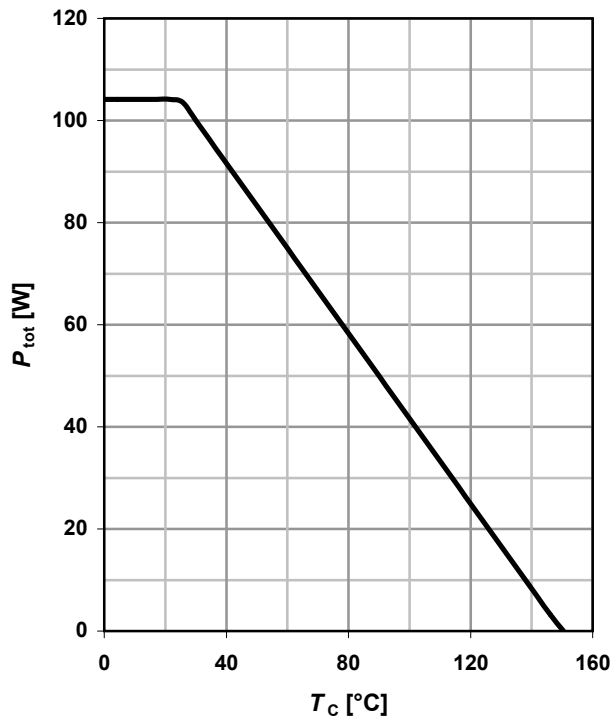
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.81	1	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	20	nC

⁴⁾ See figure 16 for gate charge parameter definition

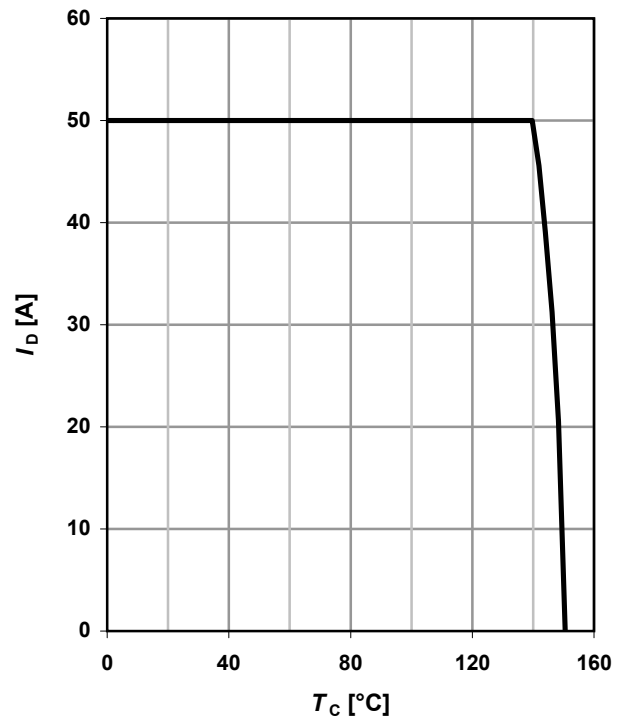
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

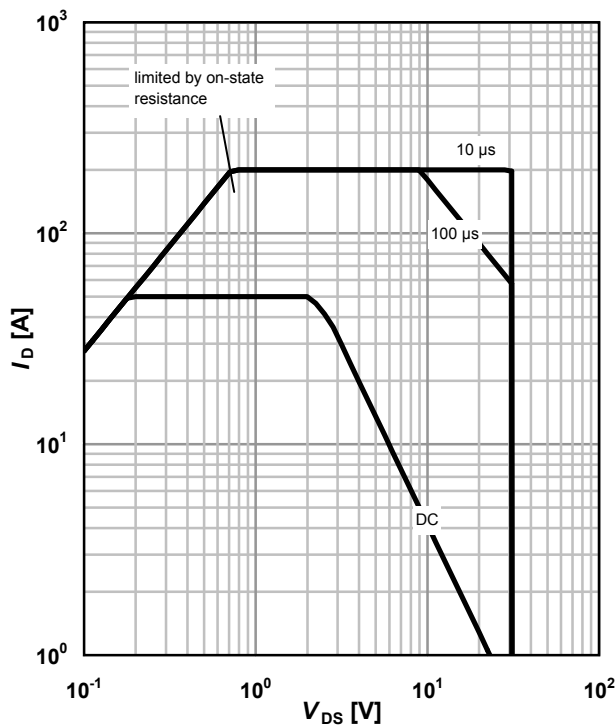
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

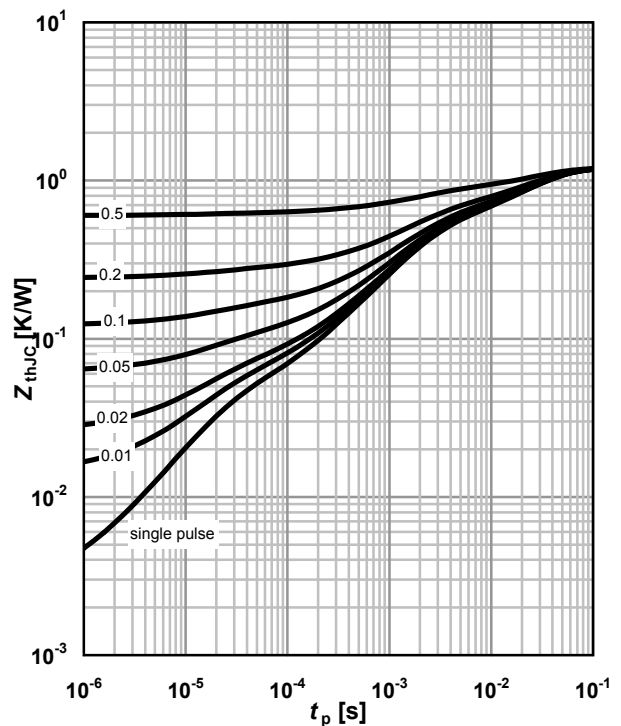
parameter: t_p



4 Max. transient thermal impedance

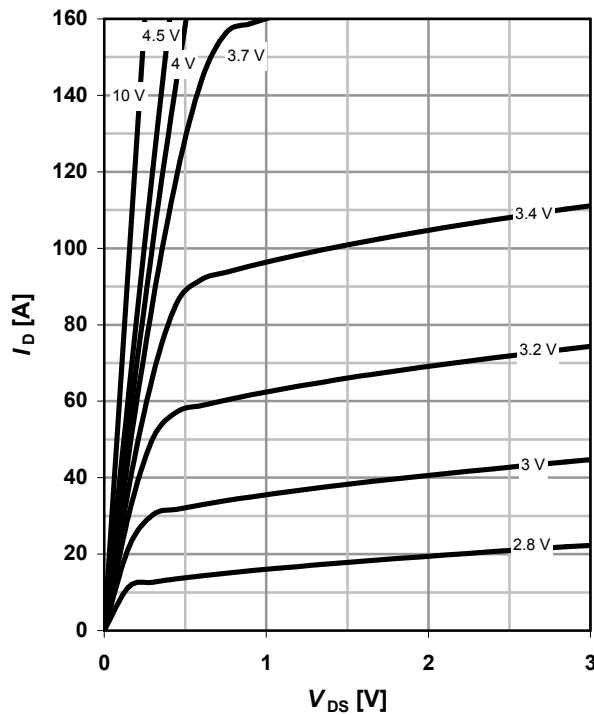
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p / T$



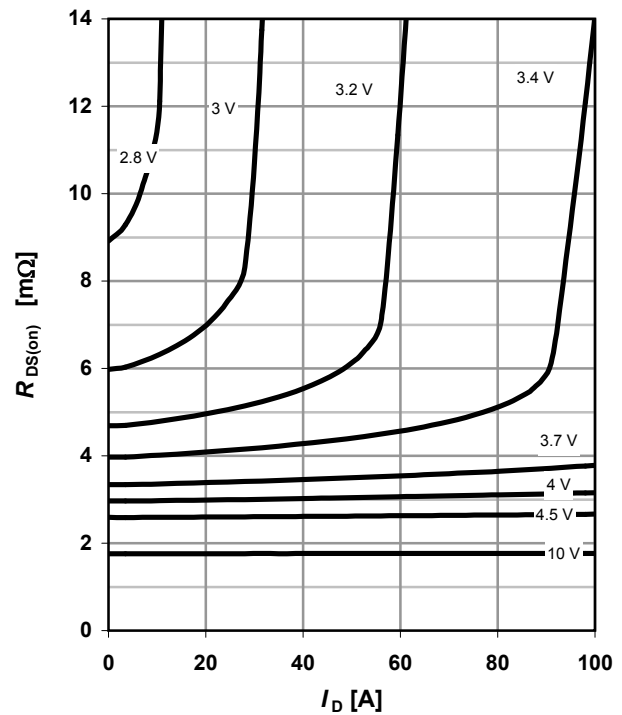
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


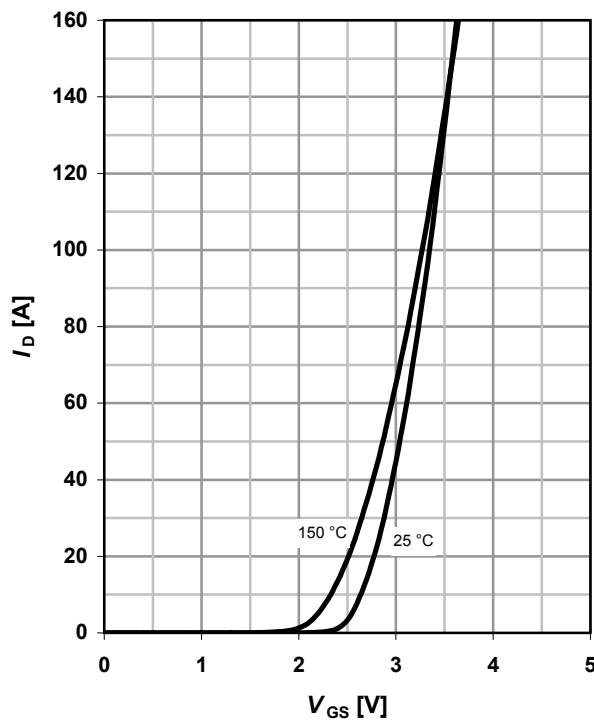
6 Typ. drain-source on resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

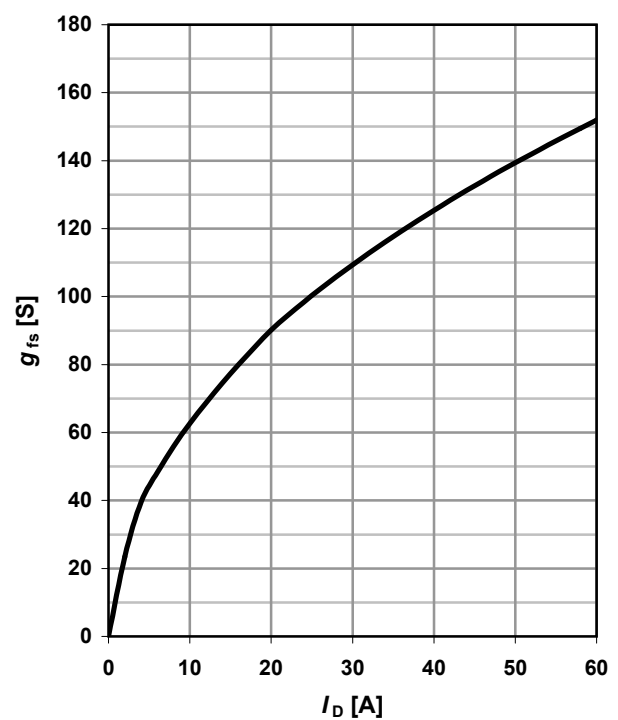
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

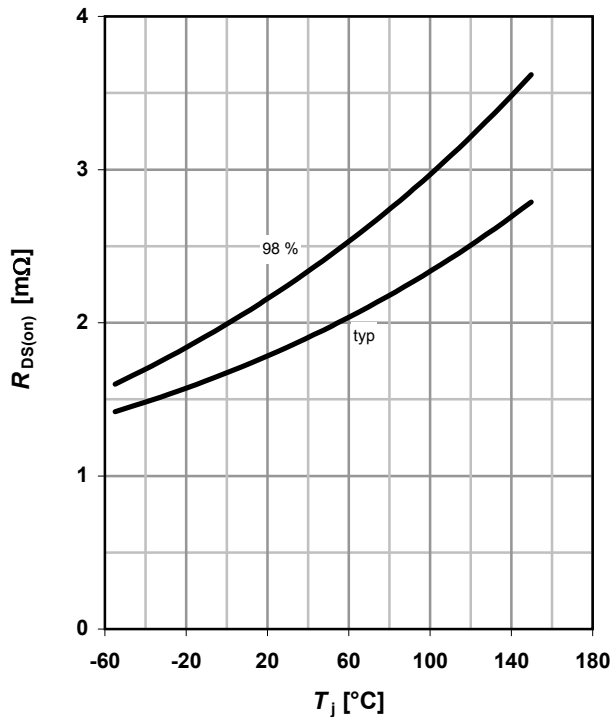
parameter: T_j


8 Typ. forward transconductance

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$


9 Drain-source on-state resistance

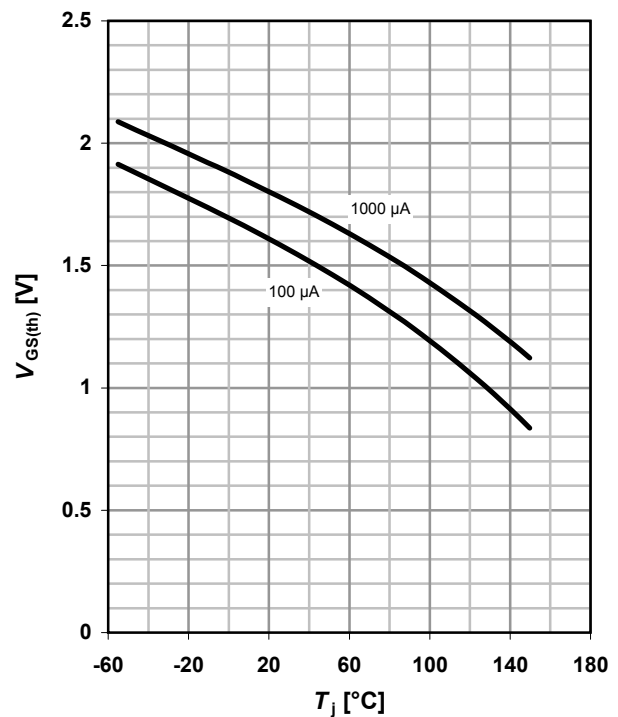
$R_{DS(on)} = f(T_j)$; $I_D = 50 \text{ A}$; $V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

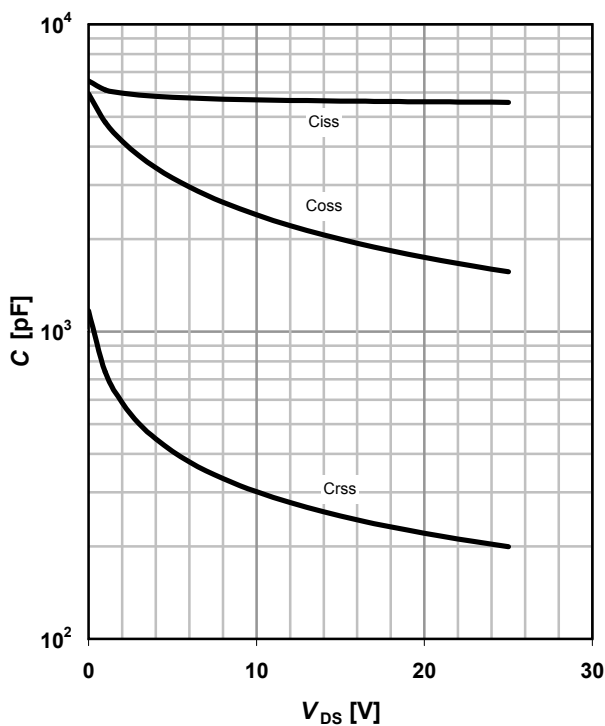
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

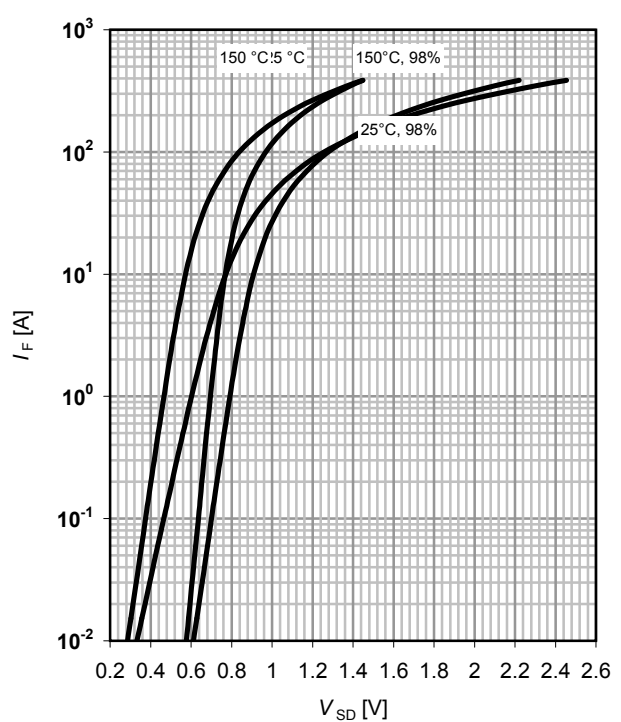
$C = f(V_{DS})$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

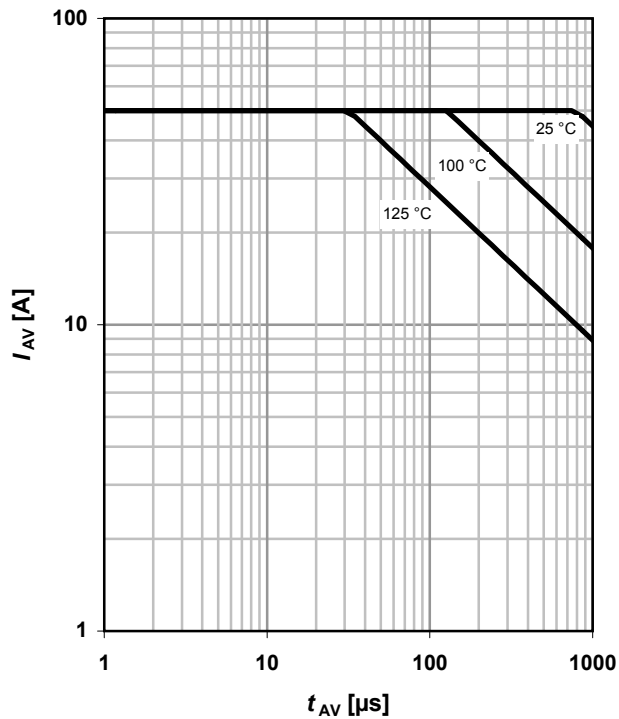
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

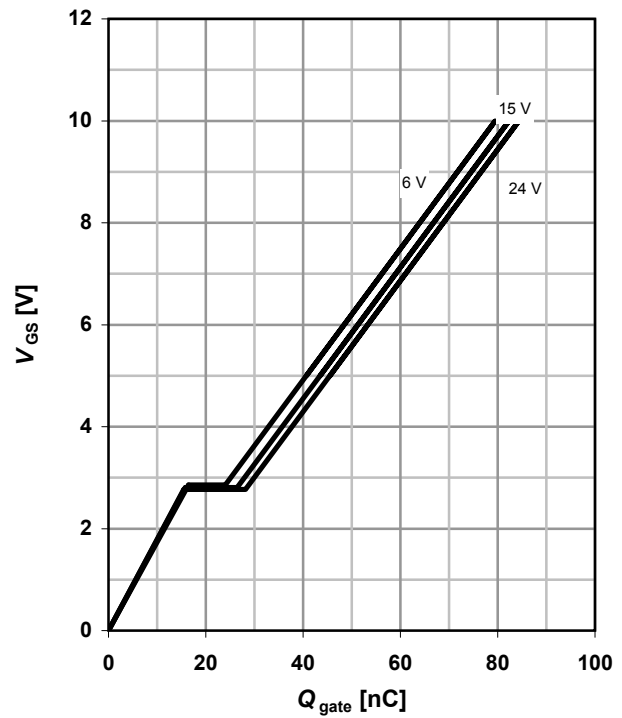
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

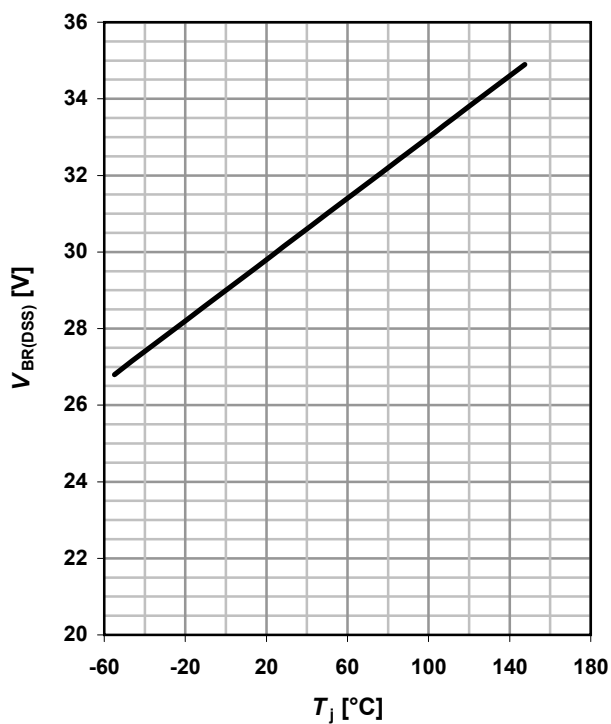
$$V_{GS}=f(Q_{\text{gate}}); I_D=25\ \text{A pulsed}$$

parameter: V_{DD}

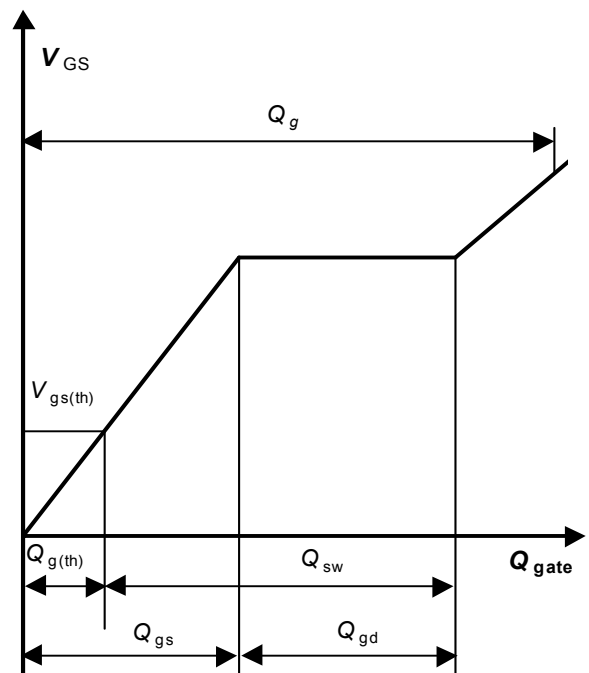


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$

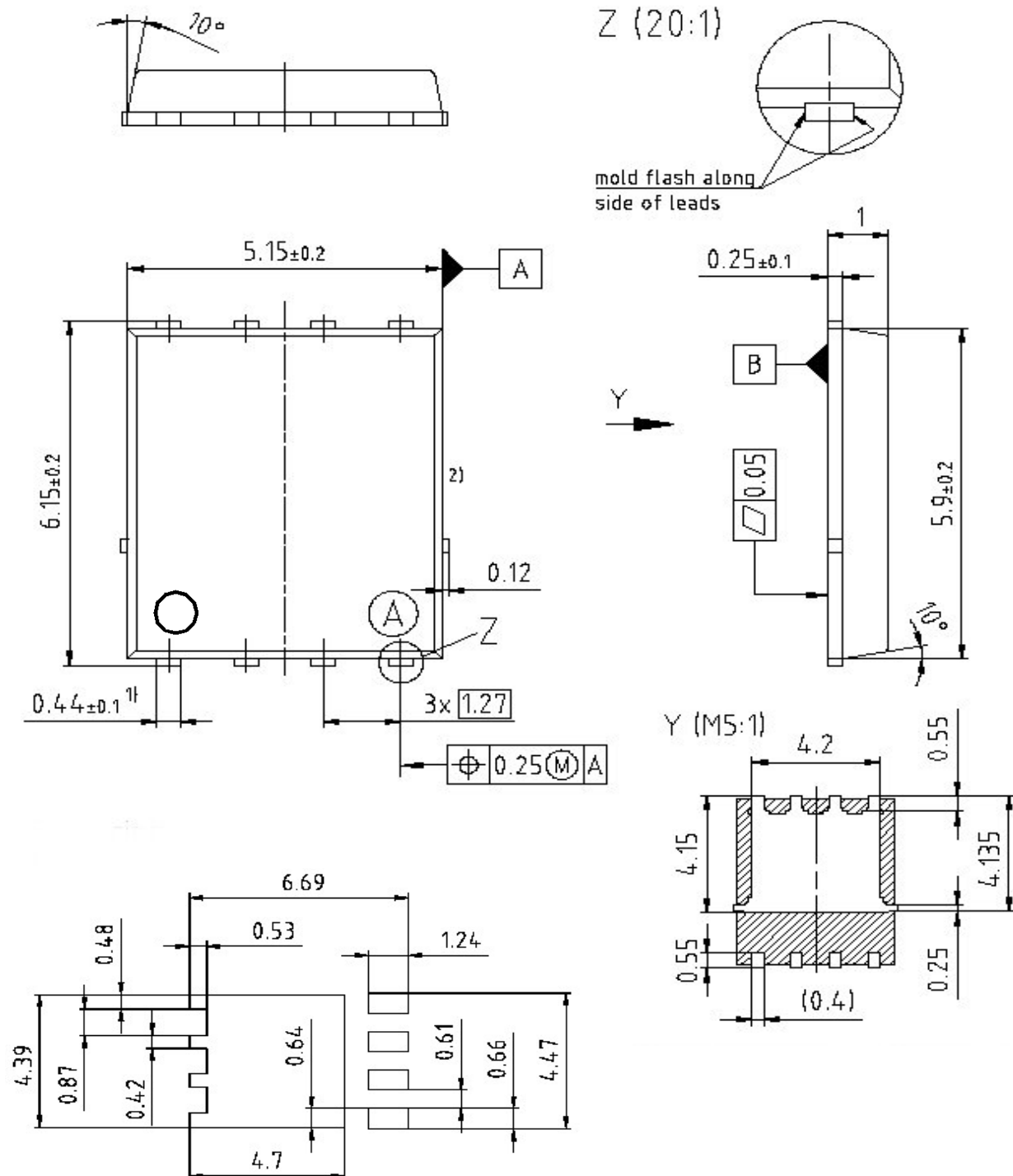


16 Gate charge waveforms



Package Outline

P-TDSON-8: Outline



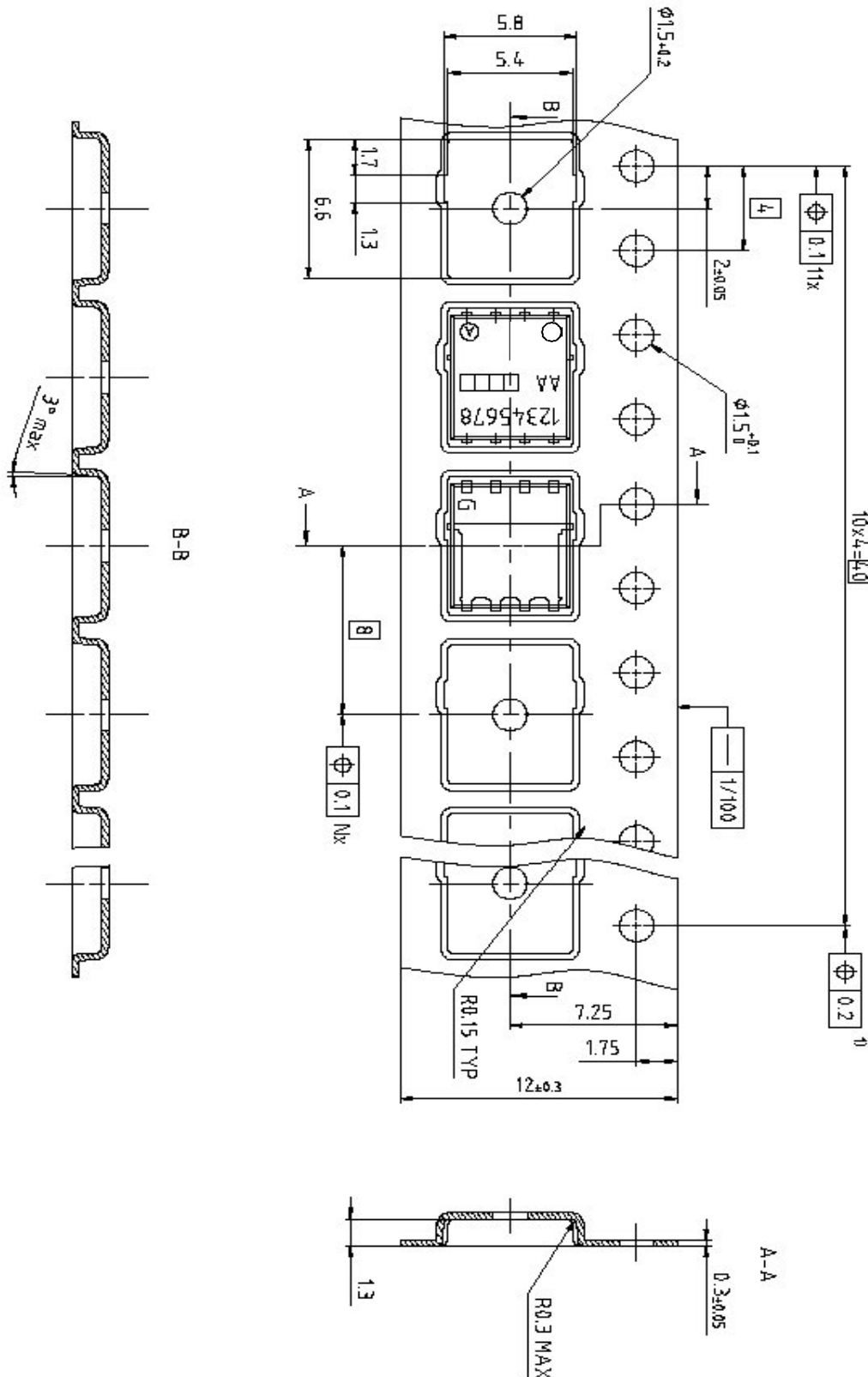
Drawing according to ISO 8015; general tolerances $\pm 0.1 / 1^\circ 30'$

Footprint

Dimensions in mm

Package Outline

P-TDSON-8: Tape



Dimensions in mm

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