FemtoClock® Multi-Rate 3.3V, 2.5V LVPECL Frequency Synthesizer

ICS843034

DATA SHEET

General Description

The ICS843034 is a general purpose, low phase noise LVPECL synthesizer which can generate frequencies for a wide variety of applications. The ICS843034 has a 4:1 input Multiplexer from which the following inputs can be selected: one differential input, one single-ended input, or two crystal oscillators, thus making the device ideal for frequency translation or frequency generation. Each differential LVPECL output pair has an output divider which can be independently set so that two different frequencies can be generated. Additionally, each LVPECL output pair has a dedicated power supply pin so the outputs can run at 3.3V or 2.5V. The ICS843034 also supplies a buffered copy of the reference clock or crystal frequency on the single-ended REF_CLK output pin which can be enabled or disabled (disabled by default). The output frequency can be programmed using either a serial or parallel programming interface.

The phase jitter of the ICS843034 is less than 1ps rms, making it suitable for use in Fibre Channel, SONET, and Ethernet applications.

Example applications include systems which must support both FEC and non FEC rates. In 10Gb Fibre Channel, for example, you can use a 25.5MHz crystal to generate a 159.375MHz reference clock, and then switch to a 20.544MHz crystal to generate 164.355MHz for 66/64 FEC. Other applications could include supporting both Ethernet frequencies and SONET frequencies in an application. When Ethernet frequencies are needed, a 25MHz crystal can be used and when SONET frequencies are needed, the input MUX can be switched to select a 38.88MHz crystal.

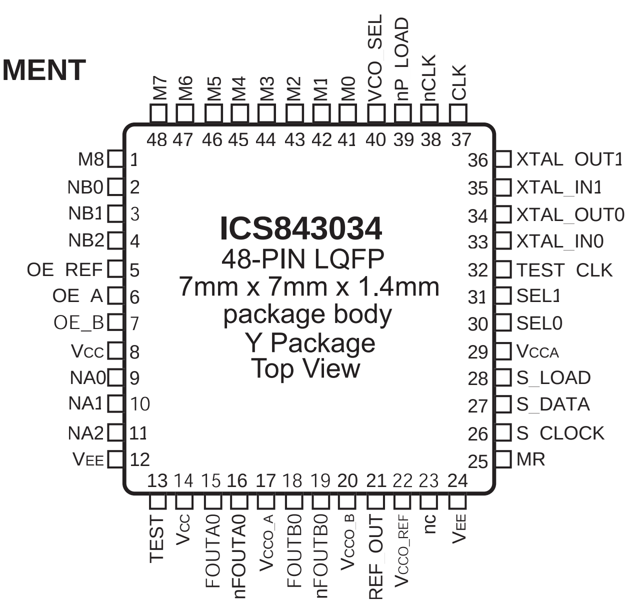
Features

- Dual differential 3.3V LVPECL outputs which can be set independently for either 3.3V or 2.5V
- 4:1 Input Mux:
  - One differential input
  - One single-ended input
  - Two crystal oscillator interfaces
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- TEST_CLK accepts LVCMOS or LVTTL input levels
- Output frequency range: 35MHz to 625MHz
- Crystal input frequency range: 12MHz to 40MHz
- VCO range: 560MHz to 625MHz
- Parallel or serial interface for programming feedback divider and output dividers
- RMS phase jitter at 333.33MHz, using a 22.222MHz crystal (12kHz to 20MHz): 0.91ps (typical)
- Supply voltage modes:

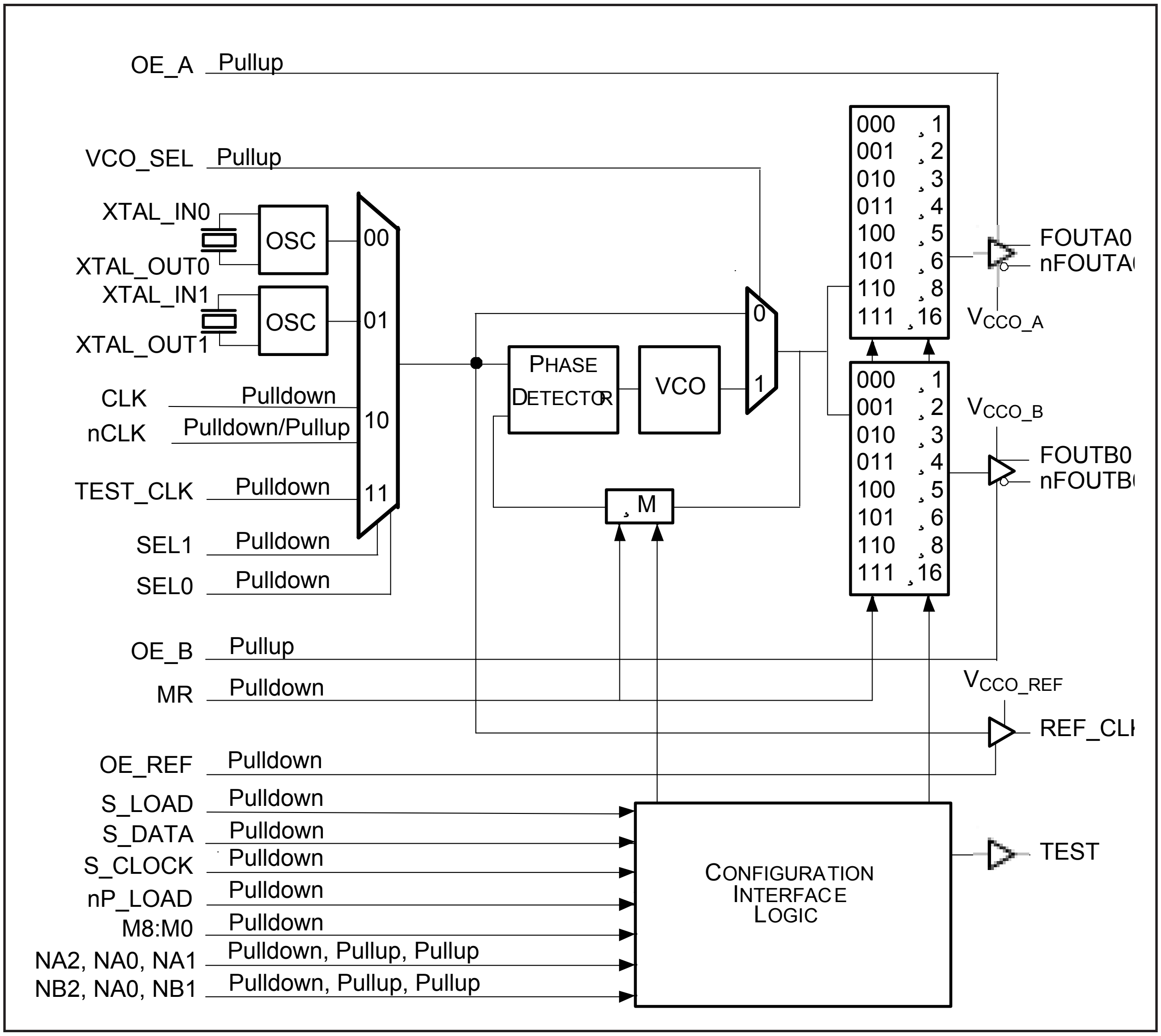
  LVPECL outputs (core/outputs):
  3.3V/3.3V
  3.3V/2.5V

  REF_CLK output (core/outputs):
  3.3V/3.3V
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request with E-pad option.
- Available in lead-free (RoHS 6) packages

Pin Assignment



BLOCK DIAGRAM



Functional Description

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS843034 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 560MHz to 625MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The ICS843034 supports either serial or parallel programming modes to program the M feedback divider and N output divider. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on the M, NA, and NB inputs are passed directly to the M divider and both N output dividers. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M and N dividers remain loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and Nx bits can be hardwired to set the M divider and Nx output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: $f_{VCO} = f_{xtal} \times M$

The M value and the required values of M0 through M8 are shown in Table 3B to program the VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as 23 ≤ M ≤ 30. The frequency out is defined as follows: $FOUT = \frac{f_{VCO}}{N} = \frac{f_{xtal} \times M}{N}$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and Nx output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and Nx output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and Nx output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and Nx bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Output
1	0	Output of M divider
1	1	Same frequencey as FOUTA0

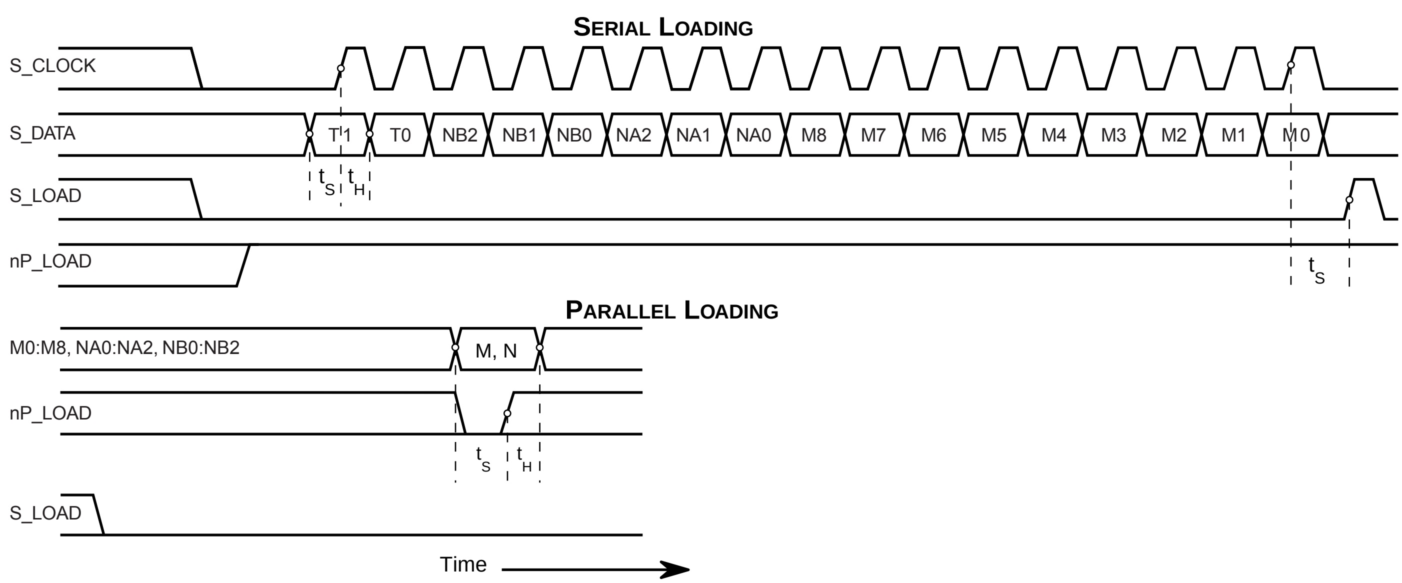


Figure 1. Parallel & Serial Load Operations

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 41, 42, 43, 44, 45, 47, 48	M8, M0, M1, M2, M3, M4, M6, M7	Input	Pulldown	M divider input. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
2, 3	NB0, NB1	Input	Pullup	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
4	NB2	Input	Pulldown	
5	OE_REF	Input	Pulldown	Output enable. Controls enabling and disabling of REF_CLK output. LVCMOS/LVTTL interface levels. REF_CLK is enable when OE_REF is HIGH. REF_CLK is Hi-Z when OE_REF is LOW. OE_REF defaults to LOW.
6	OE_A	Input	Pullup	Output enable. Controls enabling and disabling of FOUTA0, nFOUTA0 outputs. LVCMOS/LVTTL interface levels.
7	OE_B	Input	Pullup	Output enable. Controls enabling and disabling of FOUTB0, nFOUTB0 outputs. LVCMOS/LVTTL interface levels.
8, 14	V_{CC}	Power		Core supply pins.
9, 10	NA0, NA1	Input	Pullup	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
11	NA2	Input	Pulldown	
12, 24	V_{EE}	Power		Negative supply pins.
13	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.
15, 16	FOUTA0, nFOUTA0	Output		Differential output for the synthesizer. LVPECL interface levels.
17	V_{CCO_A}	Power		Output supply pin for FOUTA0, nFOUTA0.
18, 19	FOUTB0, nFOUTB0	Output		Differential output for the synthesizer. LVPECL interface levels.
20	V_{CCO_B}	Power		Output supply pin for FOUTB0, nFOUTB0.
21	REF_CLK	Output		Reference clock output. LVCMOS/LVTTL interface levels.
22	V_{CCO_REF}	Power		Output supply pin for REF_CLK.
23	nc	Unused		No connect.
25	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, forces the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS/LVTTL interface levels.
26	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
27	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
28	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
29	V_{CCA}	Power		Analog supply pin.
30, 31	SEL0, SEL1	Input	Pulldown	Clock select inputs. LVCMOS/LVTTL interface levels.
32	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS/LVTTL interface levels.
33, 34	XTAL_IN0, XTAL_OUT0	Input		Crystal oscillator interface. XTAL_IN0 is the input, XTAL_OUT0 is the output.
35, 36	XTAL_IN1, XTAL_OUT1	Input		Crystal oscillator interface. XTAL_IN1 is the input, XTAL_OUT1 is the output.

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Table 1. Pin Descriptions, continued

Number	Name	Type		Description
37	CLK	Input	Pulldown	Non-inverting differential clock input.
38	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input.V_{CC}/2 default when left floating.
39	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at NA2:NA0 and NB2:NB0 is loaded into the N output dividers. LVCMOS/LVTTL interface levels.
40	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.
46	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	REF_CLK	V_{CCO_REF} = 3.3V	5	7	12	Ω

Table 3A. Parallel and Serial Mode Function Table

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
575	23	0	0	0	0	1	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•
700	28	0	0	0	0	1	1	1	0	0
•	•	•	•	•	•	•	•	•	•	•
750	30	0	0	0	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST_CLK input frequency of 25MHz.

Table 3C. Programmable Output Divider Function Table

Inputs			N Divider Value	Output Frequency (MHz)	
*NX2	*NX1	*NX0		Minimum	Maximum
0	0	0	1	560	625
0	0	1	2	280	375
0	1	0	3	186.66	250
0	1	1	4 (default)	140	187.5
1	0	0	5	112	150
1	0	1	6	93.33	125
1	1	0	8	70	93.75
1	1	1	16	35	46.875

*NOTE: X denotes Bank A or Bank B

TABLE 3D. OE_REF

OE_REF	REF_CLK
0	Hi Z (default)
1	Enabled

TABLE 3E. OE_A, OE_B

OE_A OE_B	FOUTA0, nFOUTA0 FOUTB0, nFOUTB0
0	Disabled (Hi Z)
1	Enabled (default)

TABLE 3F. SEL0, SEL1

SEL0	SEL1	INPUT
0	0	XTAL_IN0, XTAL_OUT0 (default)
0	1	CLK, nCLK
1	0	XTAL_IN1, XTAL_OUT1
1	1	TEST_CLK

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	65.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.18	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{CCO_REF}	Output Supply	REF_CLK	3.135	3.3	3.465	V
I_{EE}	Power Supply Current				188	mA
I_{CCA}	Analog Supply Current				18	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = V_{CCO_REF} = 3.3V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, SEL[1:0], OE_REF, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, Nx2, M1:M4, M6:M8	V_{CC} = V_{IN} = 3.465V			150	µA
		Nx0, Nx1, M5, OE_A, OE_B, VCO_SEL	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	TEST_CLK, MR, SEL[1:0], OE_REF, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, Nx2, M1:M4, M6:M8	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		Nx0, Nx1, M5, OE_A, OE_B, VCO_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1	V_{CCO_REF} = 3.3V±5%	2.6			V
		REF_CLK		V_{CCO_REF} - 0.3V			V
V_{OL}	Output Low Voltage	TEST; NOTE 1	V_{CCO_REF} = 3.3V±5%			0.5	V
		REF_CLK				0.4	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK	V_{IN} = V_{CC} = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
		CLK	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 3.3V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.5		1.1	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_A,}$ V_{CCO_B} - 2V.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.1	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_A,}$ V_{CCO_B} - 2V.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL_IN0/XTAL_OUT0, XTAL_IN1/XTAL_OUT1		12		40	MHz
		CLK/nCLK, TEST_CLK		12		40	MHz
		S_CLOCK				50	MHz
t_R/t_F	Input Rise/Fall Time	TEST_CLK	20% to 80%			5	ns
		S_LOAD, S_DATA, S_CLOCK	20% to 80%		6		ns
		nP_LOAD	20% to 80%			50	ns

NOTE: For the input crystal, CLK, CLK and TEST_CLK frequency range, the M value must be set for the VCO to operate within the 560MHz to 625MHz range. Using the minimum input frequency of 12MHz, valid values of M are 47 ≤ M ≤ 52. Using the maximum frequency of 40MHz, valid values of M are 14 ≤ M ≤ 15. For N = 1, M divider value must result in a VCO frequency ≤ 625MHz.

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 7A. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			35		625	MHz
*t*jit(Ø)	Phase Jitter, RMS (Random); NOTE 1, 2		F_{OUT} = 333.33MHz, XTAL = 22.222 MHz Integration Range: 12kHz - 20MHz		0.91		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4, 6					175	ps
*t*sk(o)	Output Skew; NOTE 2, 4, 5		Measured @ the same Output Frequency			120	ps
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%	200		700	ps
		REF_CLK					
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		N Divider Values ≠ 1	45		55	%
			N Divider Values = 1	40		60	%
t_{LOCK}	PLL Lock Time					100	ms

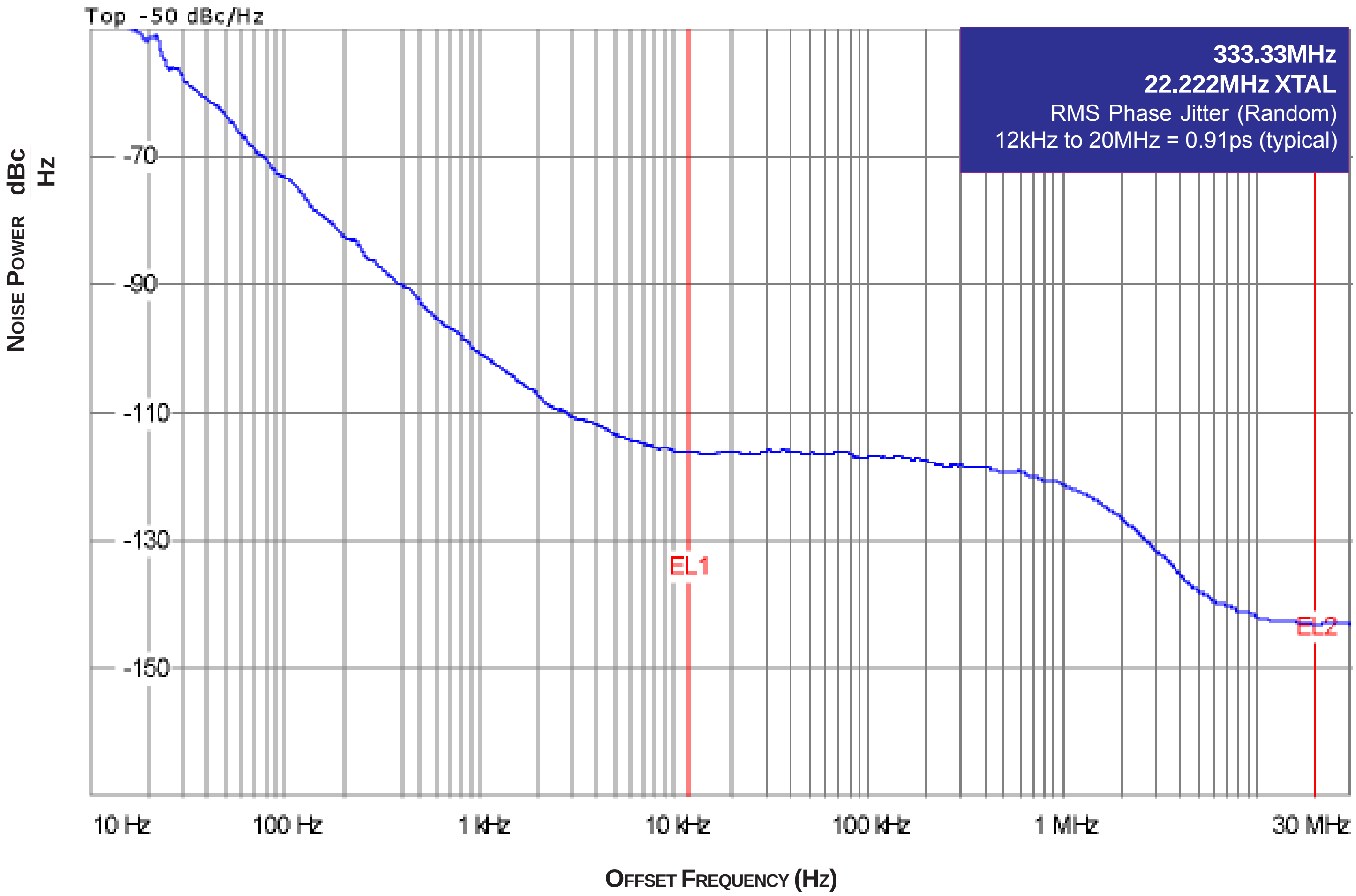
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Characterized with REF_CLK output disabled.
NOTE 3: Jitter performance using XTAL inputs.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 6: Characterized using worst device configuration.

Table 7B. AC Characteristics, V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 2.5V±5%, TA = 0°C to 70°C

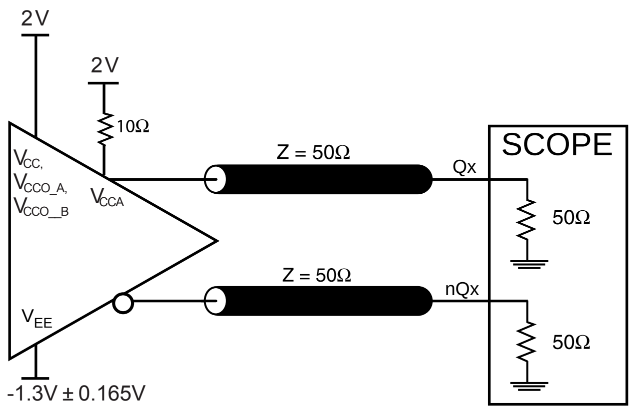
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			35		625	MHz
*t*jit(Ø)	Phase Jitter, RMS (Random); NOTE 1, 2		22.222MHz crystal, 333.33MHz, Integration Range: 12kHz - 20MHz		0.91		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4, 6					175	ps
*t*sk(o)	Output Skew; NOTE 2, 4, 5		Measured @ the same Output Frequency			120	ps
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%	200		700	ps
		REF_CLK					
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		N Divider Values ≠ 1	45		55	%
			N Divider Values = 1	40		60	%
t_{LOCK}	PLL Lock Time					100	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Characterized with REF_CLK output disabled.
NOTE 3: Jitter performance using XTAL inputs.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 6: Characterized using worst device configuration.

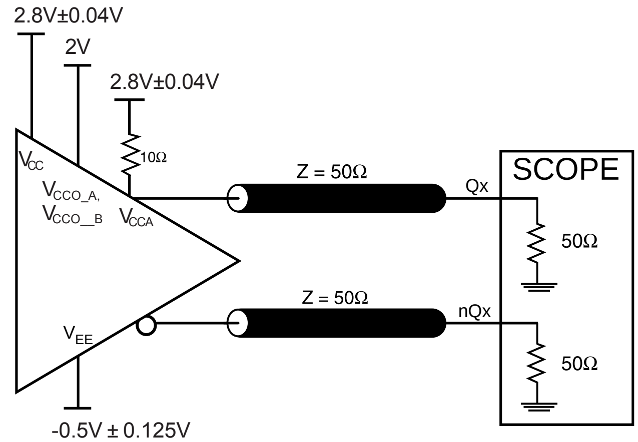
Typical Phase Noise at 333.33MHz



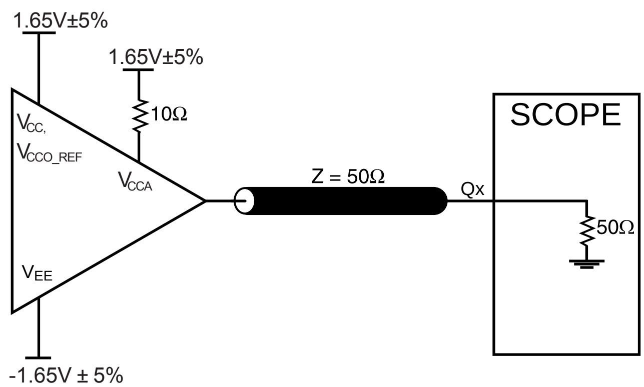
Parameter Measurement Information



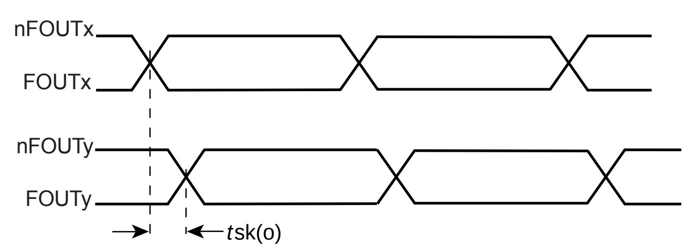
3.3V Core/3.3V Output Load AC Test Circuit FOUTA0/nFOUTA0, FOUTB0/nFOUTB0



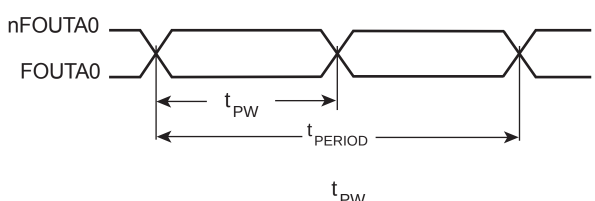
3.3V Core/2.5V Output Load AC Test Circuit FOUTA0/nFOUTA0, FOUTB0/nFOUTB0



3.3VCore/3.3V REF_CLK Output Load AC Test Circuit

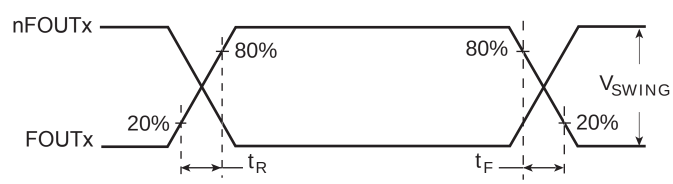


Output Skew

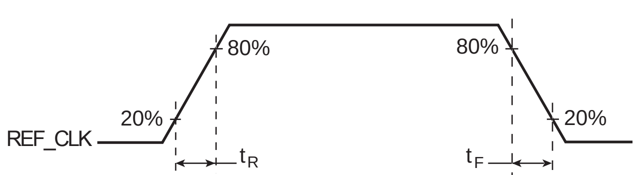


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Output Pulse Width/Period



LVPECL Output Rise/Fall Time



LVCMOS Output Rise/Fall Time

Application Information

Wiring the Differential Input Level Application

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage VREF = VCC/2 is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the VREF in the center of the input voltage swing. For example, if the input clock swing is 2.5V and VCC = 3.3V, R1 and R2 value should be adjusted to set VREF at 1.25V. The values below are for when both the single ended swing and VCC are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50W applications, R3 and R4 can be 100W. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however VIL cannot be less than -0.3V and VIH cannot be more than VCC + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

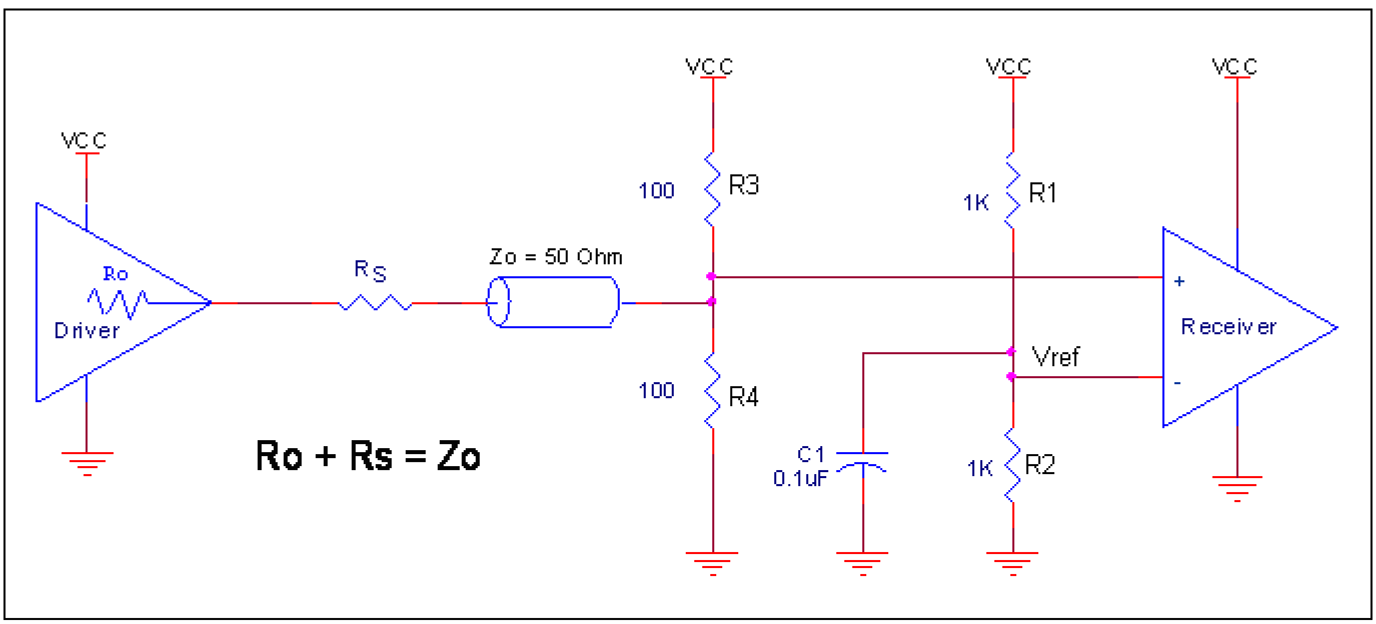


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

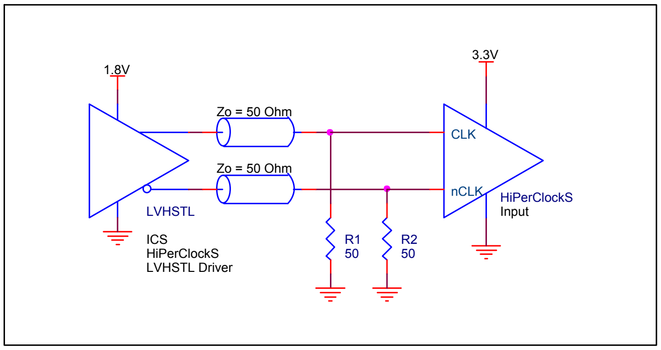


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

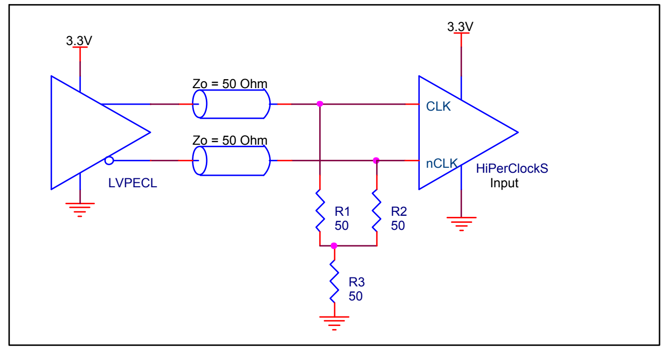


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

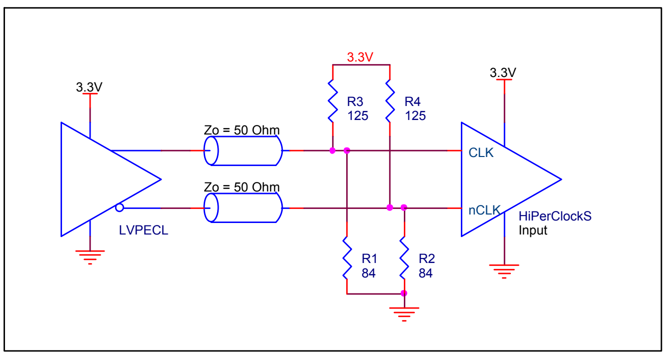


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

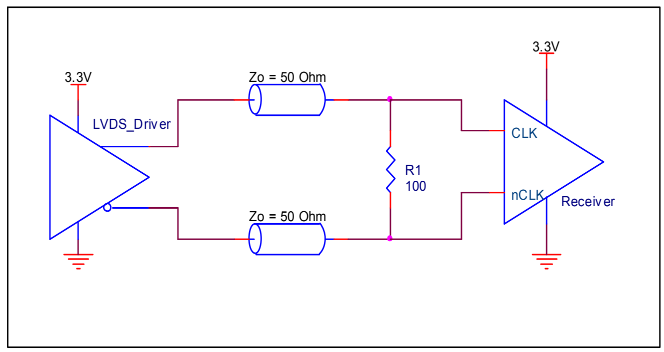


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

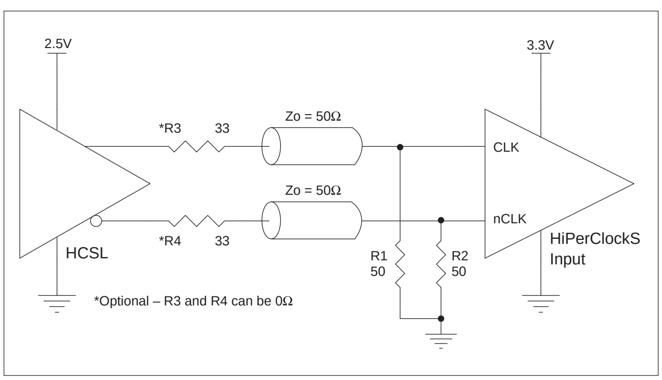


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Overdriving The XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3A shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50W applications, R1 and R2 can be 100W. This can also be accomplished by removing R1 and changing R2 to 50W. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 3B shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

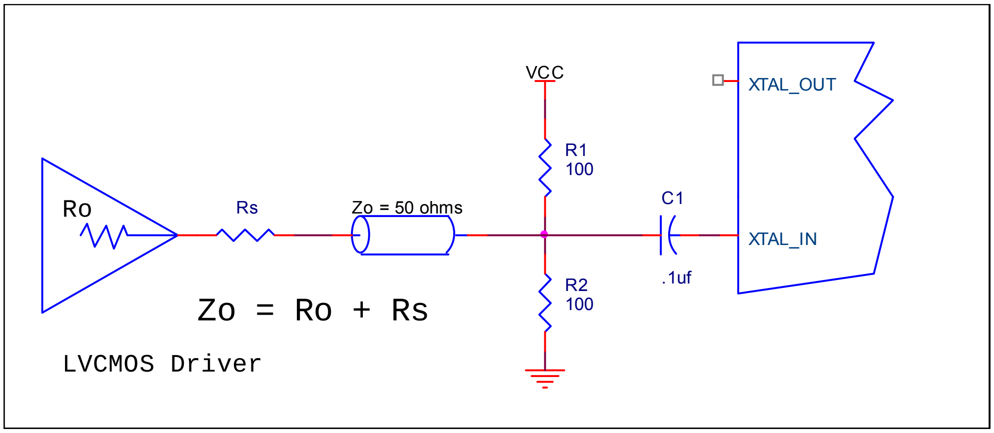


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

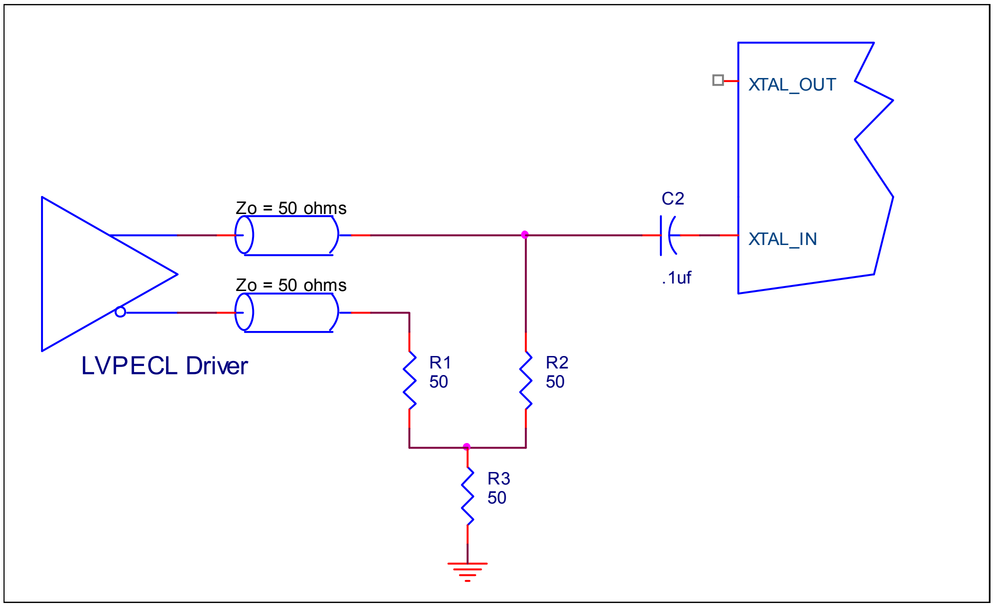


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_INx and XTAL_OUTx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins

All select pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

The unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

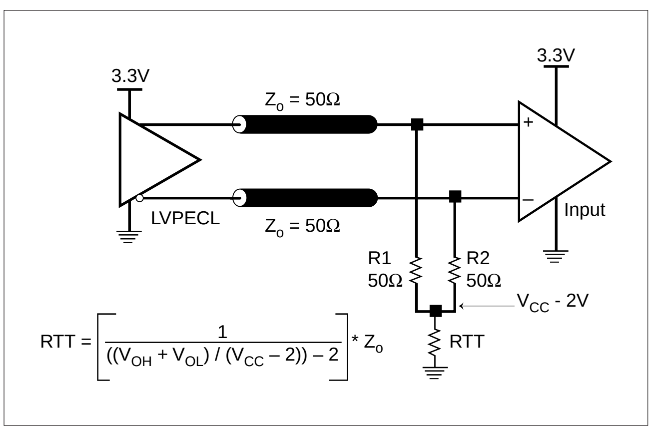


Figure 4A. LVPECL Output Termination

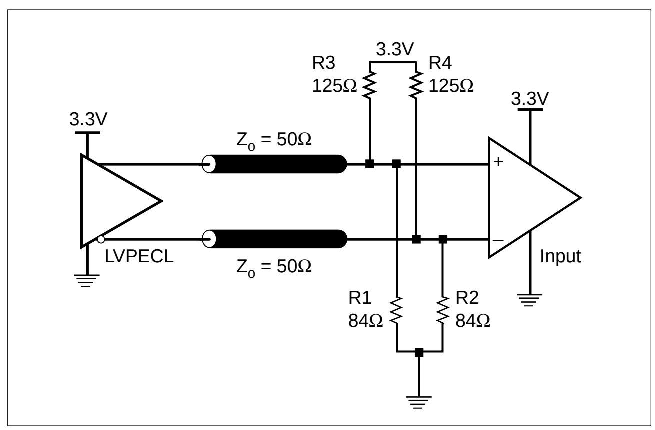


Figure 4B. LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} - 2V. For V_{CCO} = 2.5V, the V_{CCO} - 2V is very close to ground level. The R3 in *Figure 5B* can be eliminated and the termination is shown in *Figure 5C.*

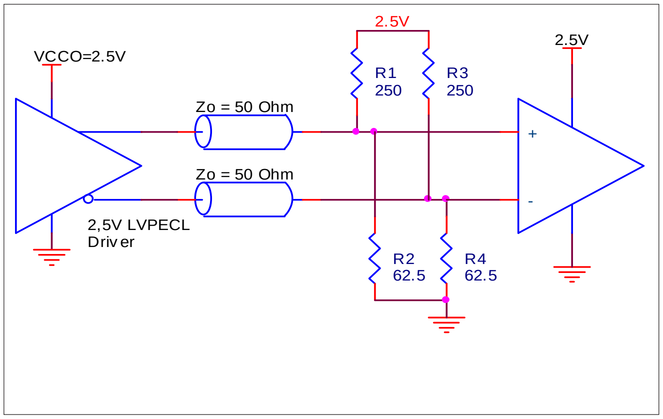


Figure 5A. 2.5V LVPECL Driver Termination Example

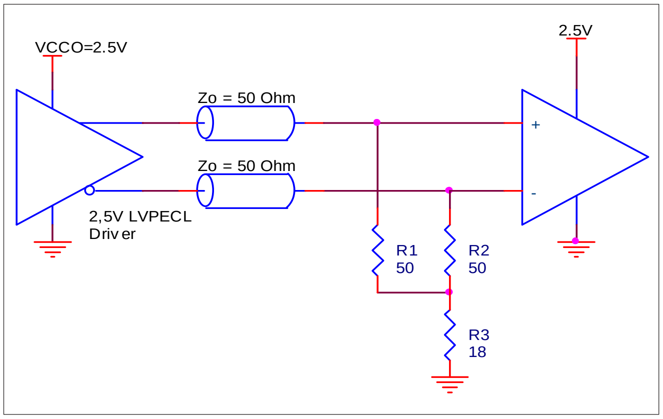


Figure 5B. 2.5V LVPECL Driver Termination Example

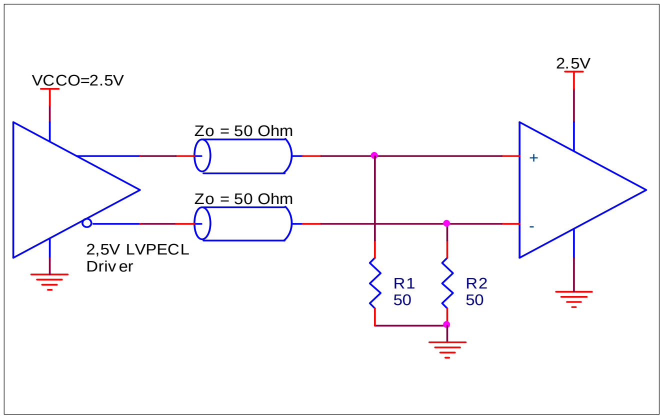


Figure 5C. 2.5V LVPECL Termination Example

Application Schematic Example

Figure 6 shows an example of ICS843034 application schematic. In this example, the device is operated $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_REF} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 18pF and C2 = 22pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843034 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

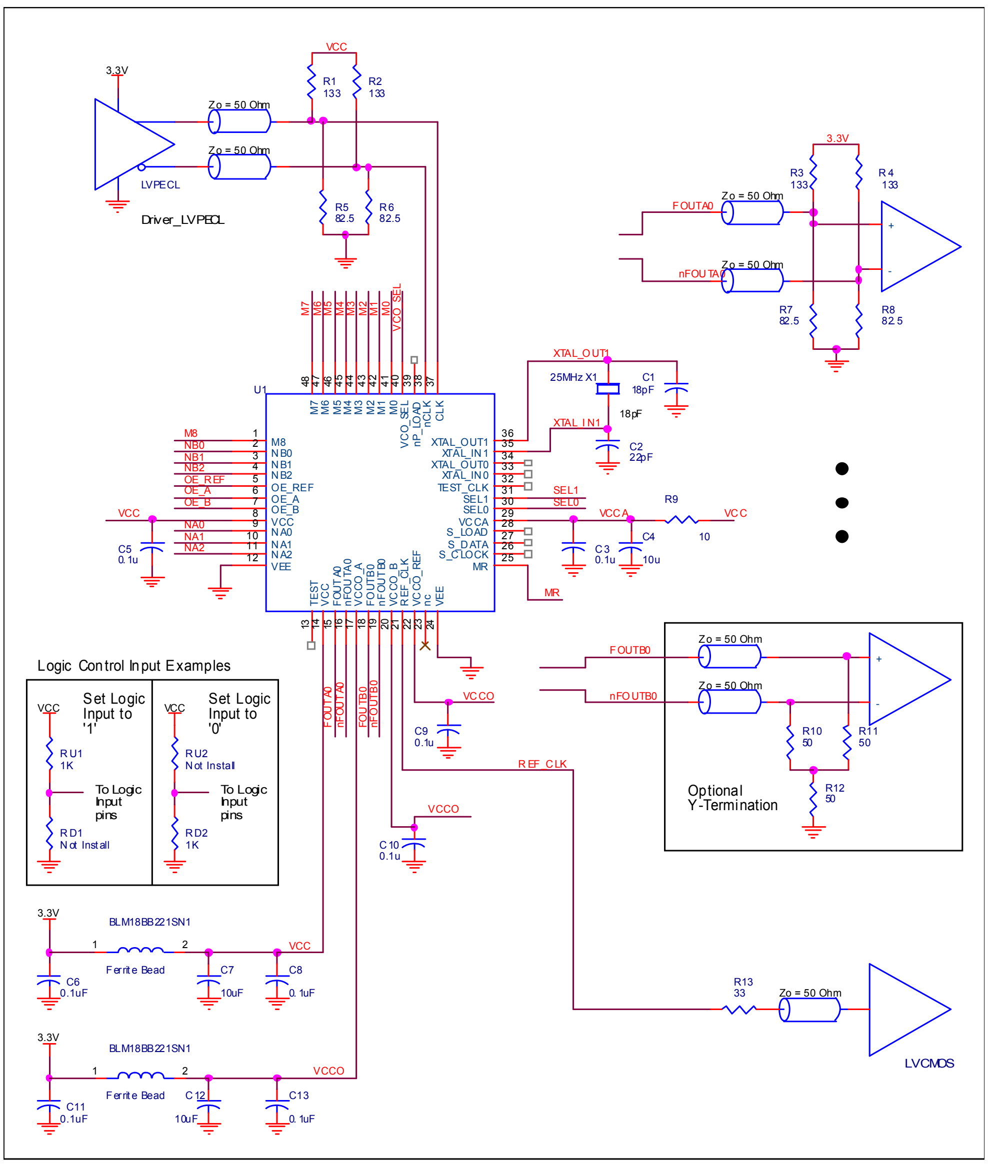


Figure 6. ICS843034 Application Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843034. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843034 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 188mA = **651.42mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 32.6mW = **65.2mW**
- Power (R_{OUT}) = $R_{OUT} * I_{OUT}^2$ = 12Ω* (49.2 mA)^2 = **29.05mW**

Total Power Dissipation

- Total Power
  = Power (core) +Power (outputs) +Power (R_{OUT})
  = 651.42mW + 65.2mW + 29.05mW
  = **745.67mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.746W * 65.7°C/W = 119.0°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 10.*

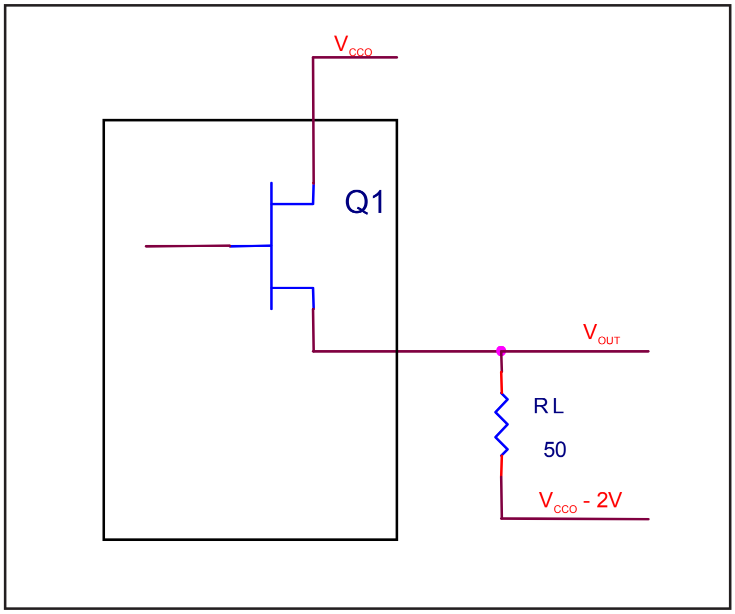


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.6V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V = \mathbf{12.8mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.6mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for 48 Lead LQFP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

Transistor Count

The transistor count for ICS843034 is: 11,748

Package Outline - Y Suffix for 48 Lead LQFP

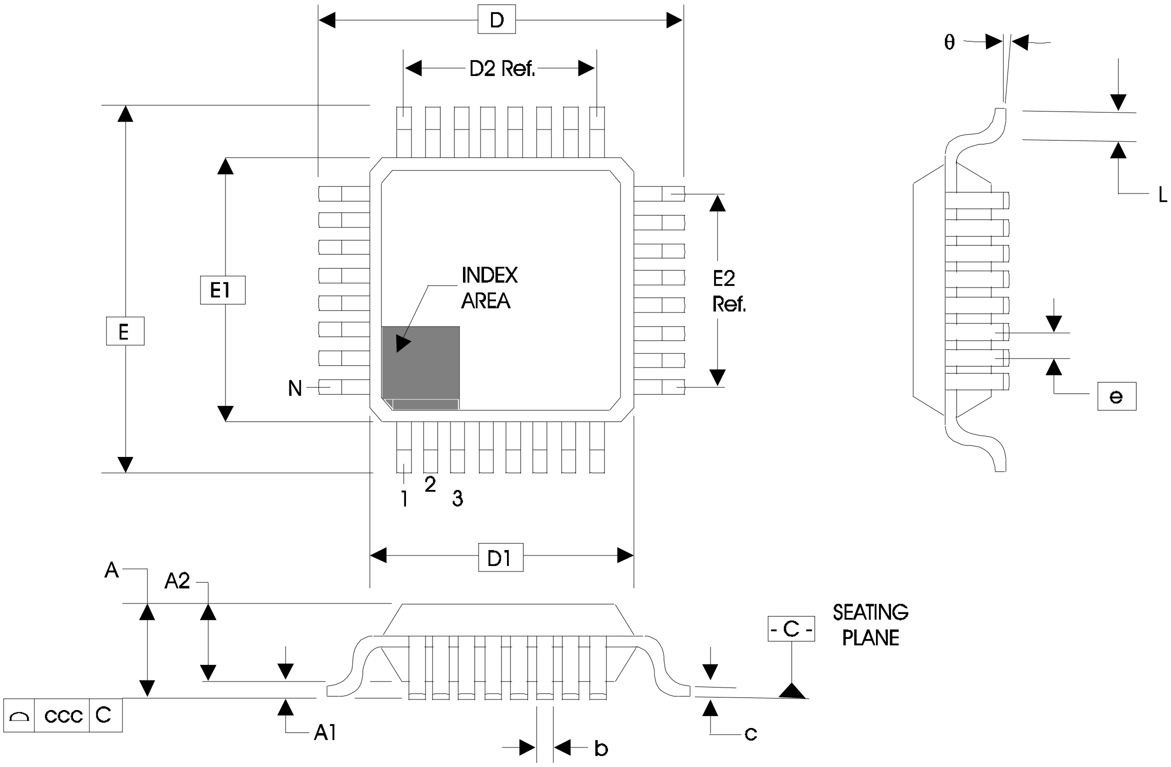


Table 10. Package Dimensions

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843034CYLF	ICS843034CYL	48 Lead "Lead-Free" LQFP	tray	0°C to 70°C
843034CYLFT	ICS843034CYL	48 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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