IXDI514 / IXDN514

14 Ampere Low-Side Ultrafast MOSFET Drivers

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected over entire Operating Range
- High Peak Output Current: 14A Peak
- Wide Operating Range: 4.5V to 30V
- -55°C to +125°C Extended Operating Temperature
- High Capacitive Load Drive Capability: 15nF in <30ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current
- Two Drivers in Single Chip

Applications

- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Power Charge Pumps

General Description

The IXDI514 and IXDN514 are high speed high current gate drivers specifically designed to drive the largest IXYS MOSFETs & IGBTs to their minimum switching time and maximum parctical frequency limits. The IXDI514 and IXDN514 can source and sink 14 Amps of Peak Current while producing voltage rise and fall times of less than 30ns. The inputs of the Drivers are compatible with TTL or CMOS and are virtually immune to latch up over the entire operating range! Patented* design innovations eliminate cross conduction and current "shoot-through". Improved speed and drive capabilities are further enhanced by very quick & matched rise and fall times.

The IXDI514 is configured as a Inverting Gate Driver, and the IXDN514 is configured as a Non-Inverting Gate Driver.

The IXDI514 and IXDN514 are each available in the 8-Pin P-DIP (PI) package, the 8-Pin SOIC (SIA) package, and the 6-Lead DFN (D1) package, (which occupies less than 65% of the board area of the 8-Pin SOIC).

*United States Patent 6,917,227

Ordering Information

Part Number	Description	Package Type	Packing Style	Pack Qty	Configuration
IXDI514PI	14A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50	Inverting
IXDI514SIA	14A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	
IXDI514SIAT/R	14A Low Side Gate Driver I.C.	8-Pin SOIC	13” Tape and Reel	2500	
IXDI514D1	14A Low Side Gate Driver I.C.	6-Lead DFN	2” x 2” Waffle Pack	56	
IXDI514D1T/R	14A Low Side Gate Driver I.C.	6-Lead DFN	13” Tape and Reel	2500	
IXDN514PI	14A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50	Non-Inverting
IXDN514SIA	14A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	
IXDN514SIAT/R	14A Low Side Gate Driver I.C.	8-Pin SOIC	13” Tape and Reel	2500	
IXDN514D1	14A Low Side Gate Driver I.C.	6-Lead DFN	2” x 2” Waffle Pack	56	
IXDN514D1T/R	14A Low Side Gate Driver I.C.	6-Lead DFN	13” Tape and Reel	2500	

NOTE: All parts are lead-free and RoHS Compliant

Figure 1 - IXDI514 Inverting 14A Gate Driver Functional Block Diagram

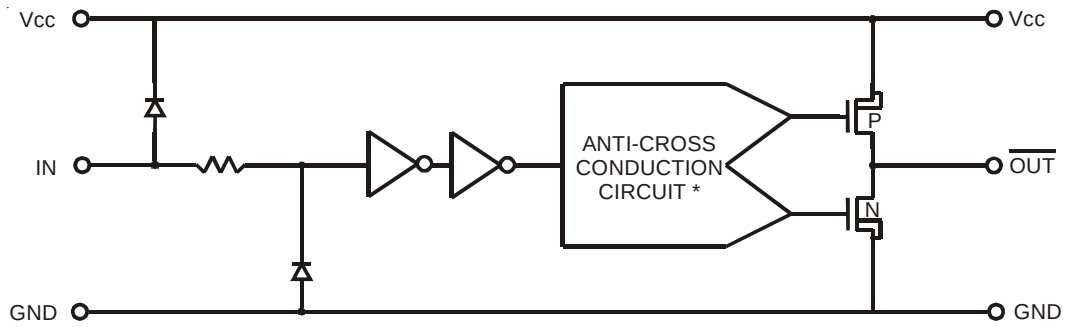
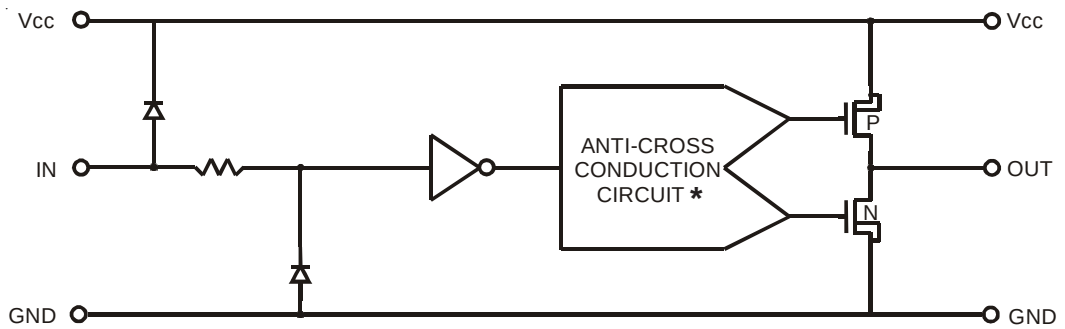


Figure 2 - IXDN514 14A Non-Inverting Gate Driver Functional Block Diagram



* **United States Patent 6,917,227**

Absolute Maximum Ratings (1)

Parameter	Value
Supply Voltage	35 V
All Other Pins	-0.3 V to V_{CC} + 0.3V
Junction Temperature	150 °C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 Sec)	300 °C

Operating Ratings (2)

Parameter			Value
Operating Supply Voltage			4.5V to 30V
Operating Temperature Range			-55 °C to 125 °C
Package Thermal Resistance *			
8-Pin PDIP	(PI)	θ_{J-A} (typ)	125 °C/W
8-Pin SOIC	(SIA)	θ_{J-A} (typ)	200 °C/W
6-Lead DFN	(D1)	θ_{J-A} (typ)	125-200 °C/W
6-Lead DFN	(D1)	θ_{J-C} (max)	1.5 °C/W
6-Lead DFN	(D1)	θ_{J-S} (typ)	5.8 °C/W

Electrical Characteristics @ T_A = 25 °C (3)

Unless otherwise noted, 4.5V ≤ V_{CC} ≤ 30V .
All voltage measurements with respect to GND. IXD_514 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ(4)	Max	Units
V_{IH}	High input voltage	4.5V ≤ V_{CC} ≤ 18V	2.5			V
V_{IL}	Low input voltage	4.5V ≤ V_{CC} ≤ 18V			1.0	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	I_{OUT} = 10mA, V_{CC} = 18V		600	1000	mΩ
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, V_{CC} = 18V		600	1000	mΩ
I_{PEAK}	Peak output current	V_{CC} is 18V		14		A
I_{DC}	Continuous output current	Limited by package power dissipation			4	A
t_R	Rise time	C_L=15nF Vcc=18V	23	25	40	ns
t_F	Fall time	C_L=15nF Vcc=18V	21	22	50	ns
t_{ONDLY}	On-time propagation delay	C_L=15nF Vcc=18V	29	30	30	ns
t_{OFFDLY}	Off-time propagation delay	C_L=15nF Vcc=18V	29	31	50	ns
V_{CC}	Power supply voltage		4.5	18	30	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

Electrical Characteristics @ temperatures over -55 ºC to 125 ºC (3)

Unless otherwise noted, 4.5V ≤ V_{CC} ≤ 30V , Tj < 150ºC
All voltage measurements with respect to GND. IXD_502 configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ (4)	Max	Units
V_{IH}	High input voltage	4.5V ≤ V_{CC} ≤ 18V	2.7			V
V_{IL}	Low input voltage	4.5V ≤ V_{CC} ≤ 18V			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	V_{CC} = 18V			1.25	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V			1.25	Ω
I_{DC}	Continuous output current				1	A
t_R	Rise time	C_L=10,000pF Vcc=18V		23	100	ns
t_F	Fall time	C_L=10,000pF Vcc=18V		30	100	ns
t_{ONDLY}	On-time propagation delay	C_L=10,000pF Vcc=18V		20	60	ns
t_{OFFDLY}	Off-time propagation delay	C_L=10,000pF Vcc=18V		40	60	ns
V_{CC}	Power supply voltage		4.5	18	30	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

Notes:
1. Operating the device beyond the parameters listed as “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The device is not intended to be operated outside of the Operating Ratings.
3. Electrical Characteristics provided are associated with the stated Test Conditions.
4. Typical values are presented in order to communicate how the device is expected to perform, but not necessarily to highlight any specific performance limits within which the device is guaranteed to function.

* The following notes are meant to define the conditions for the θ_{J-A}, θ_{J-C} and θ_{J-S} values:

1) The θ_{J-A} (typ) is defined as junction to ambient. The θ_{J-A} of the standard single die 8-Lead PDIP and 8-Lead SOIC are dominated by the resistance of the package, and the IXD_5XX are typical. The values for these packages are natural convection values with vertical boards and the values would be lower with natural convection. For the 6-Lead DFN package, the θ_{J-A} value supposes the DFN package is soldered on a PCB. The θ_{J-A} (typ) is 200 °C/W with no special provisions on the PCB, but because the center pad provides a low thermal resistance to the die, it is easy to reduce the θ_{J-A} by adding connected copper pads or traces on the PCB. These can reduce the θ_{J-A} (typ) to 125 °C/W easily, and potentially even lower. The θ_{J-A} for DFN on PCB without heatsink or thermal management will vary significantly with size, construction, layout, materials, etc. This typical range tells the user what he is likely to get if he does no thermal management.

2) θ_{J-C} (max) is defined as juction to case, where case is the large pad on the back of the DFN package. The θ_{J-C} values are generally not published for the PDIP and SOIC packages. The θ_{J-C} for the DFN packages are important to show the low thermal resistance from junction to the die attach pad on the back of the DFN, -- and a guardband has been added to be safe.

3) The θ_{J-S} (typ) is defined as junction to heatsink, where the DFN package is soldered to a thermal substrate that is mounted on a heatsink. The value must be typical because there are a variety of thermal substrates. This value was calculated based on easily available IMS in the U.S. or Europe, and not a premium Japanese IMS. A 4 mil dialectric with a thermal conductivity of 2.2W/mC was assumed. The result was given as typical, and indicates what a user would expect on a typical IMS substrate, and shows the potential low thermal resistance for the DFN package.

Pin Description

SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 30V.
IN	Input	Input signal-TTL or CMOS compatible.
OUT	Output	Driver Output. For application purposes, this pin is connected, through a resistor, to Gate of a MOSFET/IGBT.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.

CAUTION: Follow proper ESD procedures when handling and assembling this component.

Figure 3 - Characteristics Test Diagram

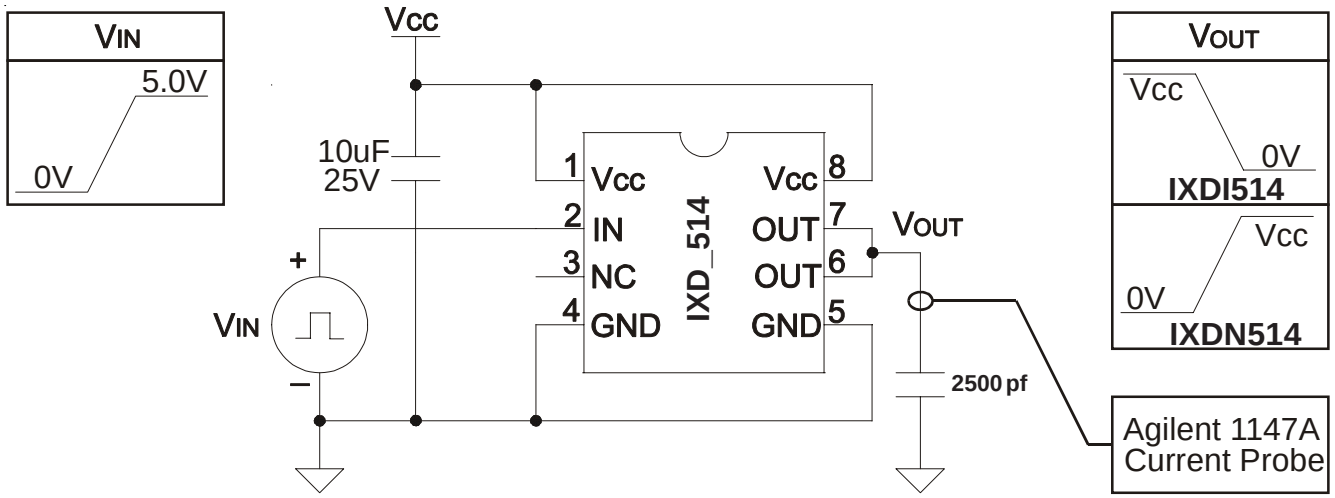
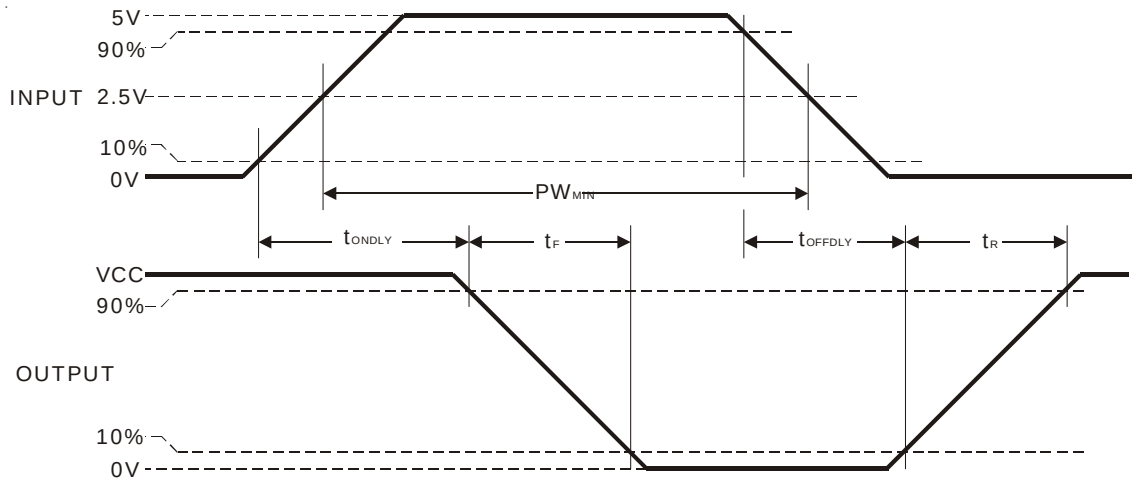
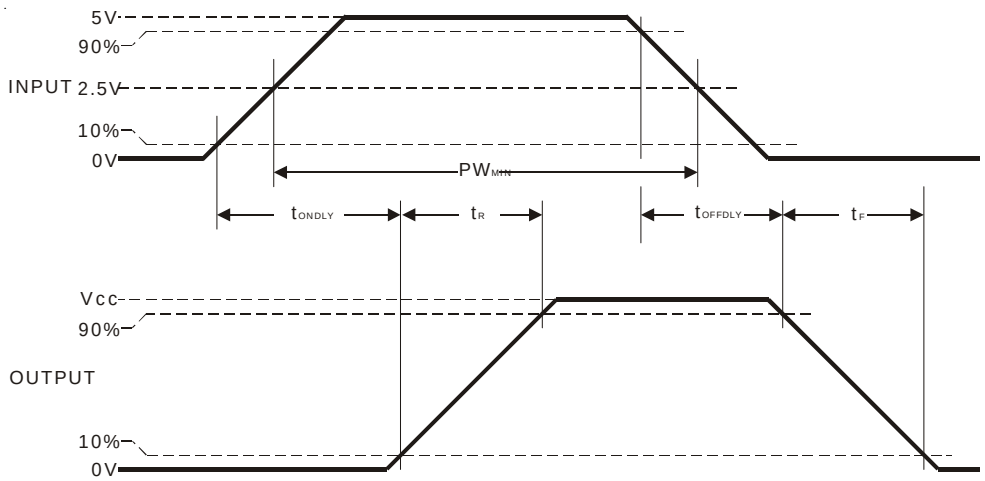


Figure 4 - Timing Diagrams

Inverting (IXDI514) Timing Diagram



Non-Inverting (IXDN514) Timing Diagram



Typical Performance Characteristics

Fig. 5 Rise Time vs. Supply Voltage

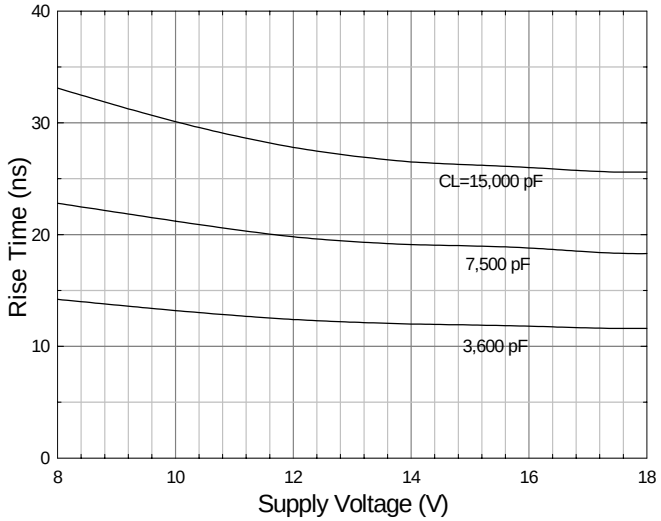


Fig. 6 Fall Time vs. Supply Voltage

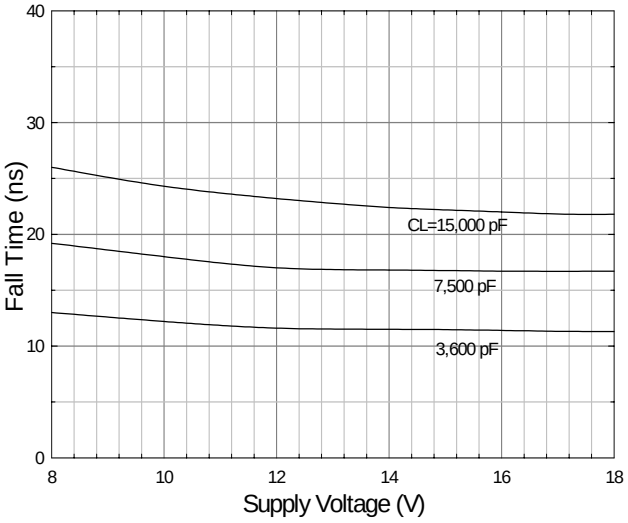


Fig. 7 Rise And Fall Times vs. Case Temperature
C_L = 15 nF, V_{cc} = 18V

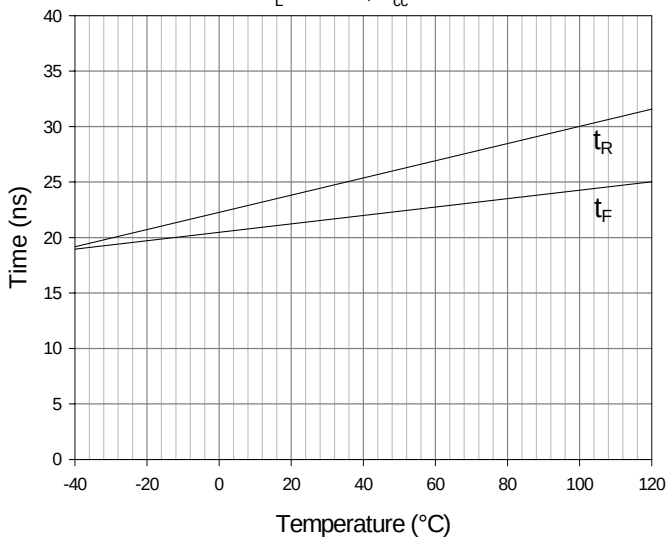


Fig. 8 Rise Time vs. Load Capacitance

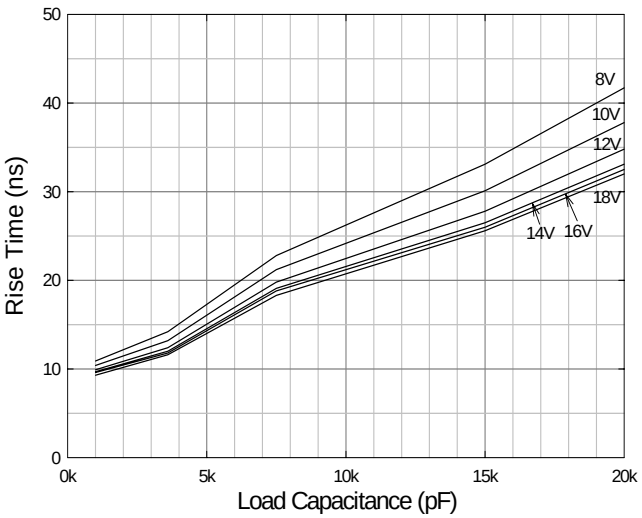


Fig. 9 Fall Time vs. Load Capacitance

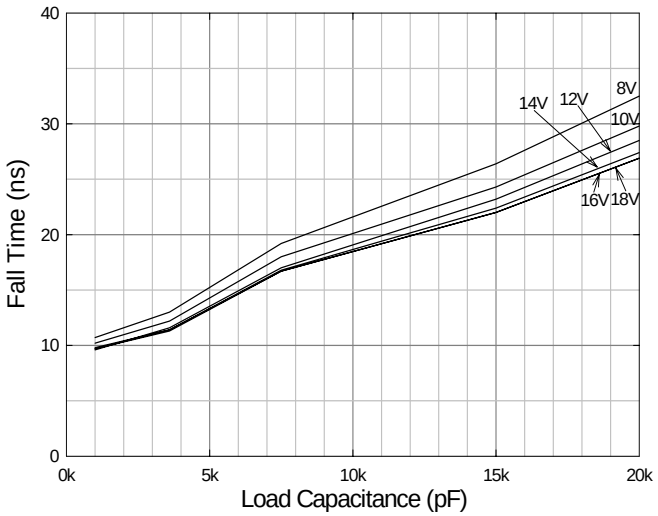


Fig. 10 Max / Min Input vs. Case Temperature
V_{CC}=18V C_L=15nF

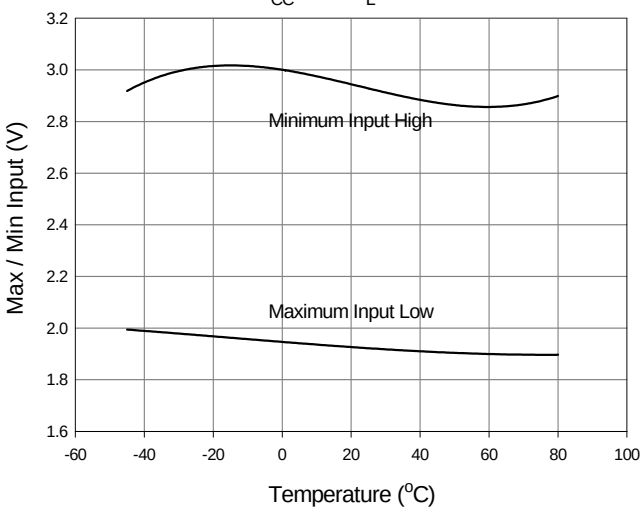


Fig. 11 Supply Current vs. Load Capacitance Vcc=18V

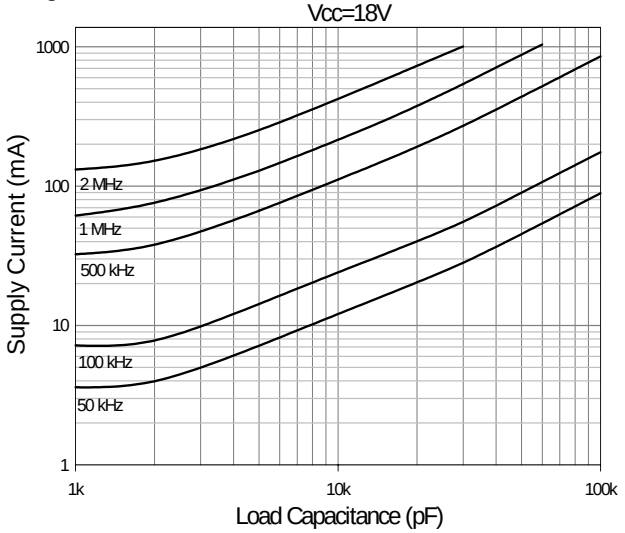


Fig. 12 Supply Current vs. Frequency Vcc=18V

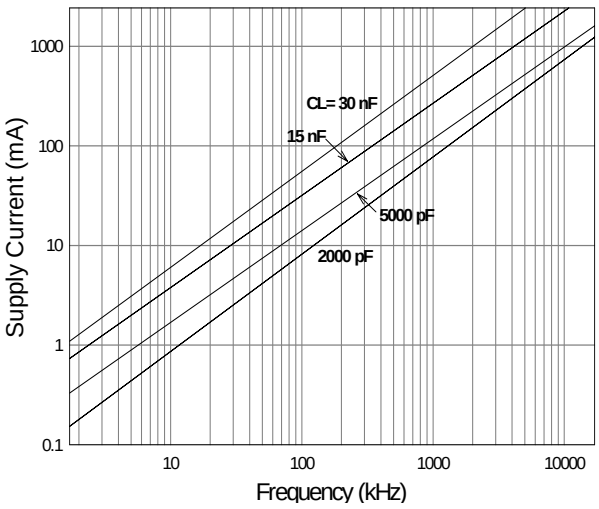


Fig. 13 Supply Current vs. Load Capacitance Vcc=12V

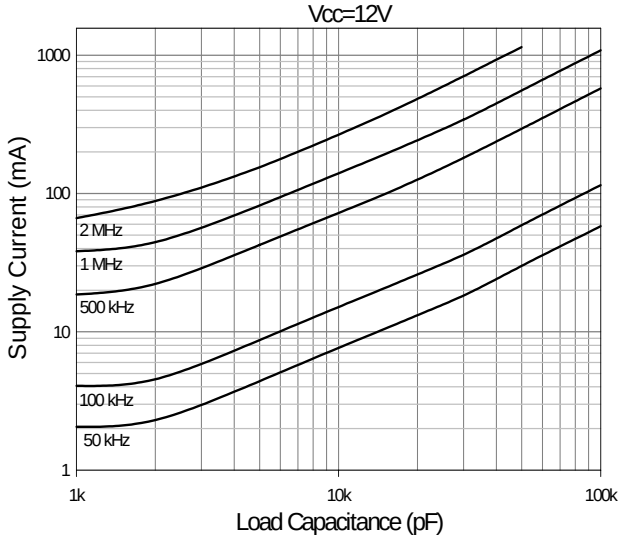


Fig. 14 Supply Current vs. Frequency Vcc=12V

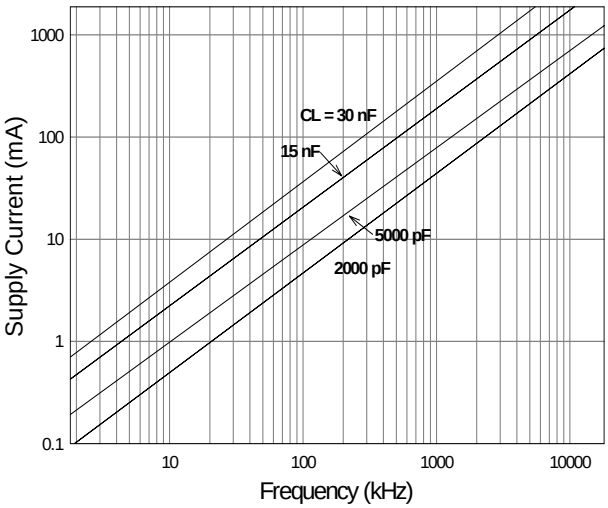


Fig. 15 Supply Current vs. Load Capacitance Vcc=8V

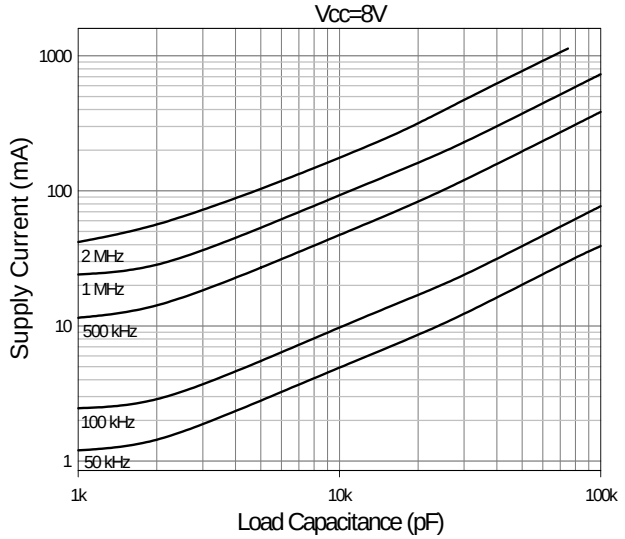


Fig. 16 Supply Current vs. Frequency Vcc=8V

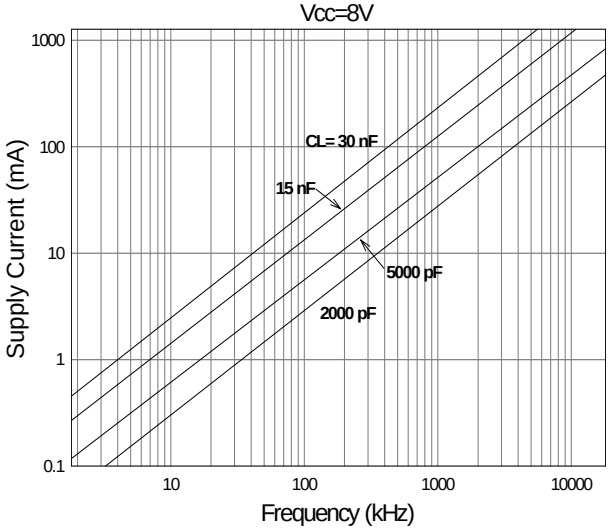


Fig. 17 Propagation Delay vs. Supply Voltage
C_L=15nF V_{IN}=5V@1kHz

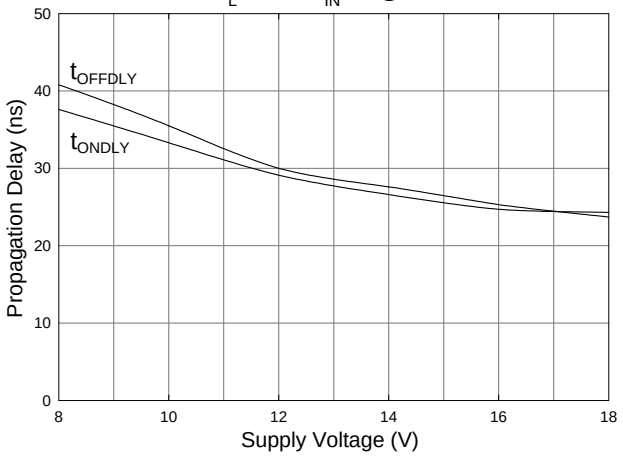


Fig. 18 Propagation Delay vs. Input Voltage
C_L=15nF V_{CC}=15V

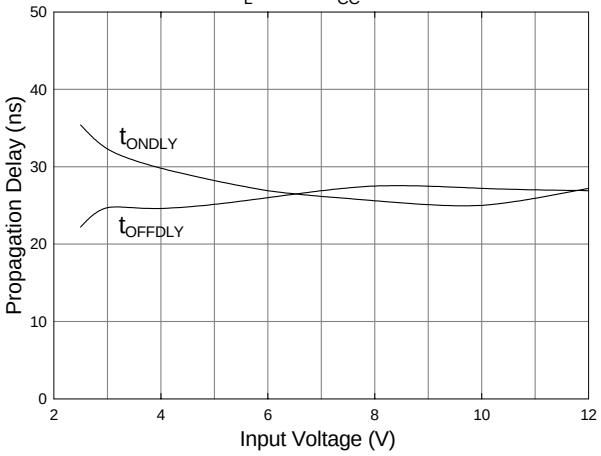


Fig. 19 Propagation Delay vs. Case Temperature
C_L = 2500pF, V_{CC} = 18V

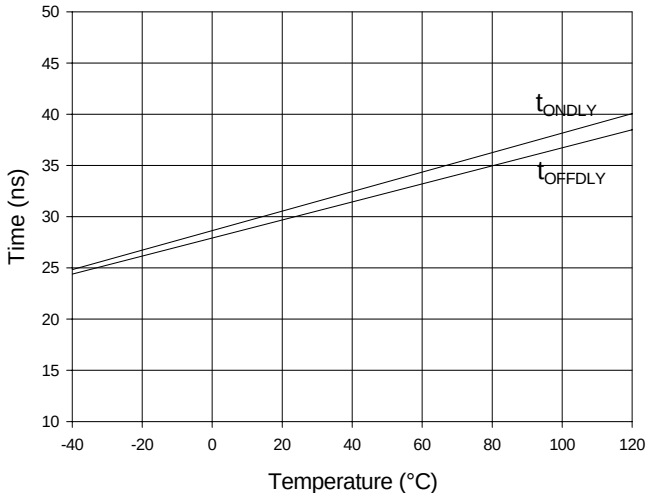


Fig. 20 Quiescent Supply Current vs. Case Temperature
V_{CC}=18V V_{IN}=5V@1kHz

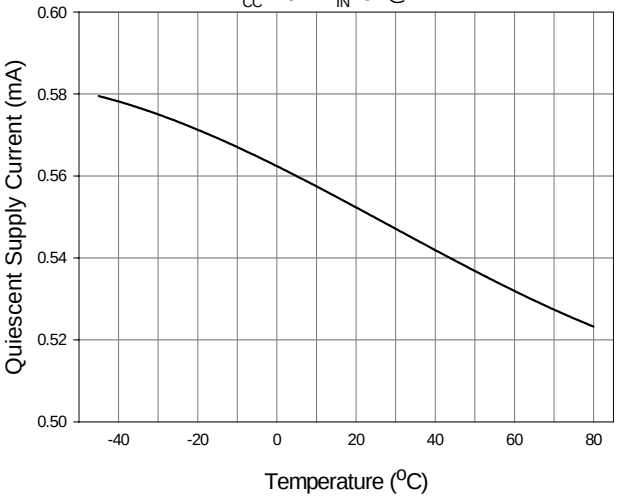


Fig. 21 P Channel Output Current vs. Case Temperature
V_{CC}=18V C_L=.1uF

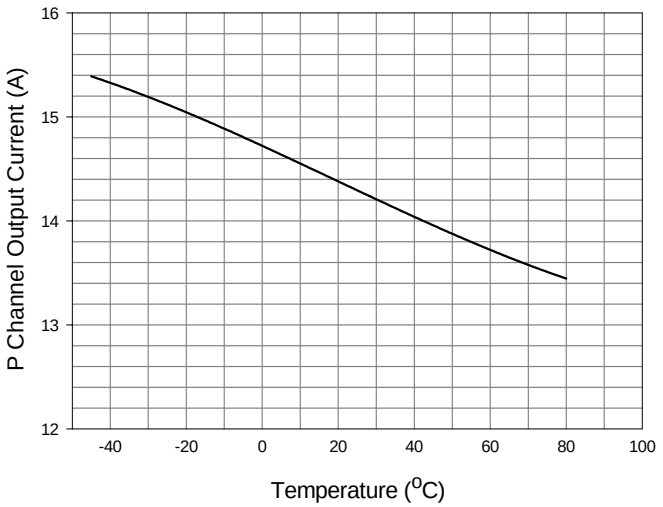


Fig. 22 N Channel Output Current vs. Case Temperature
V_{CC}=18V C_L=.1uF

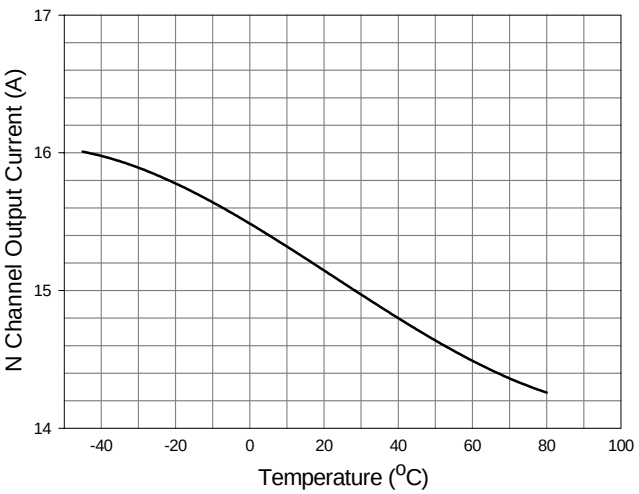


Fig. 23 Enable Threshold vs. Supply Voltage

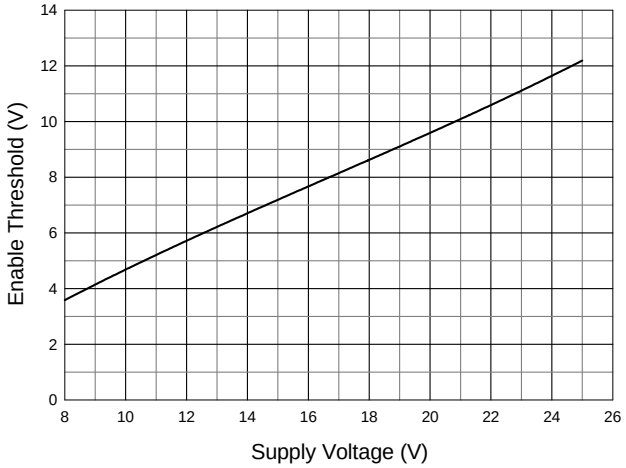


Fig. 24 High State Output Resistance vs. Supply Voltage

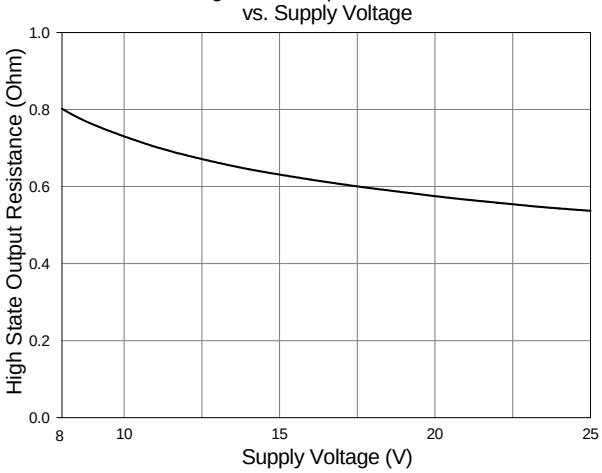


Fig. 25 Low-State Output Resistance vs. Supply Voltage

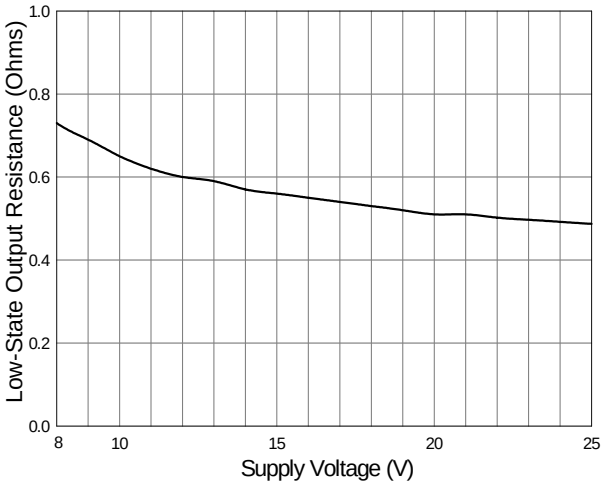


Fig. 26 V_{CC} vs. P Channel Output Current
C_L=.1uF V_{IN}=0-5V@1kHz

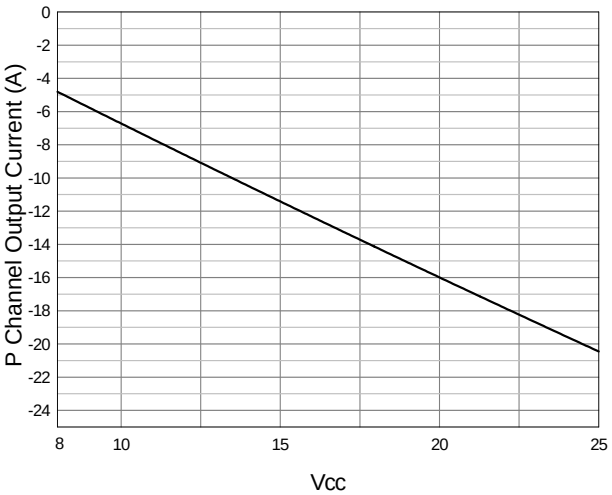
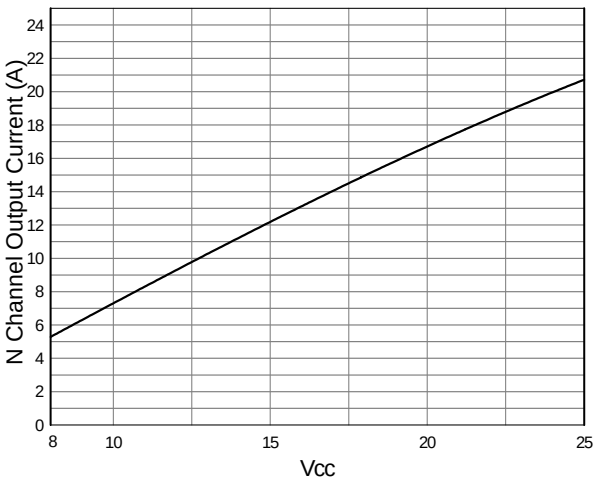
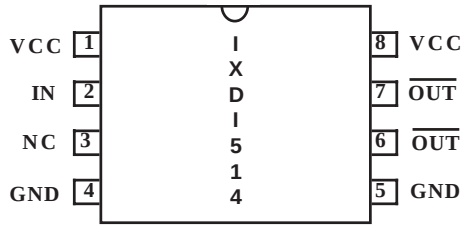


Fig. 27 Vcc vs. N Channel Output Current
C_L=.1uF V_{IN}=0-5V@1kHz

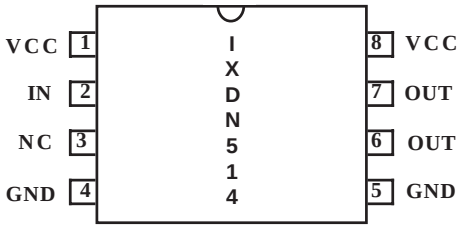


PIN CONFIGURATIONS

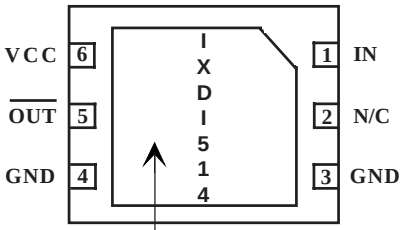
8 PIN DIP (PI)
8 PIN SOIC (SIA)



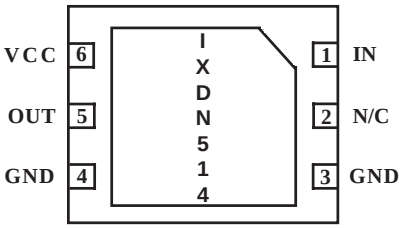
8 PIN DIP (PI)
8 PIN SOIC (SIA)



6 LEAD DFN (D1)
(Bottom View)



6 LEAD DFN (D1)
(Bottom View)



NOTE: Solder tabs on bottoms of DFN packages are grounded

Supply Bypassing, Grounding Practices And Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXD_514, it is very important to observe certain design criteria in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXD_514 to charge a 5000pF capacitive load from 0 to 25 volts in 25ns.

Using the formula: $I = \Delta V\ C / \Delta t$, where ΔV=25V C=5000pF & Δt=25ns, we can determine that to charge 5000pF to 25 volts in 25ns will take a constant current of 5A. (In reality, the charging current won't be constant, and will peak somewhere around 8A).

SUPPLY BYPASSING

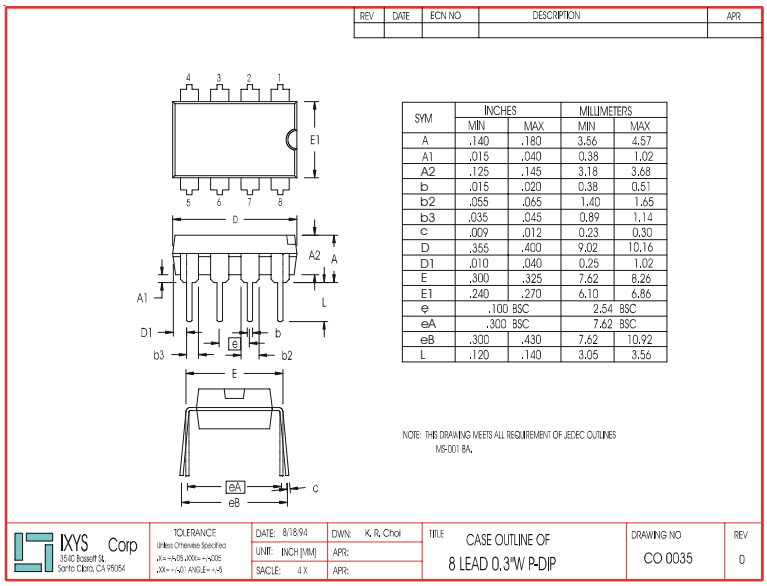
In order for our design to turn the load on properly, the IXD_514 must be able to draw this 5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is an order of magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected and should have low inductance, low resistance and high-pulse current-service ratings). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXD_514 to an absolute minimum.

GROUNDING

In order for the design to turn the load off properly, the IXD_514 must be able to drain this 5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXD_514 and its load. Path #2 is between the IXD_514 and its power supply. Path #3 is between the IXD_514 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXD_514.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible. If the driver must be placed farther than 2" (5mm) from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connected directly to the ground terminal of the load.

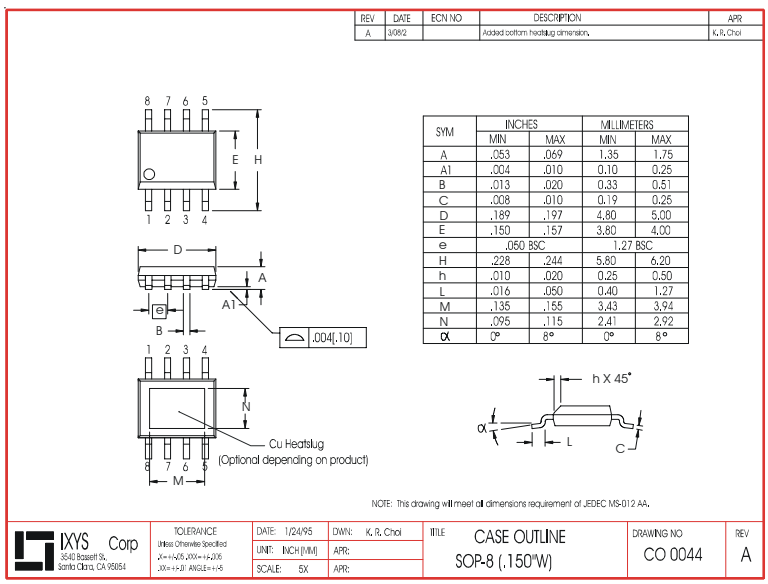


REV	DATE	ECN NO	DESCRIPTION	APR

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.355	.400	9.02	10.16
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 BA.

IXYS Corp, 3540 Bassett St, Santa Clara, CA 95054 | TOLERANCE: Unless Otherwise Specified .X= +/-0.05 .XXX= +/-0.005 .XX= +/-0.01 ANGLE= +/-5 | DATE: 8/18/94 | DWN: K. R. Choi | UNIT: INCH [MM] | APR: | SACLE: 4 X | APR: | TITLE: CASE OUTLINE OF 8 LEAD 0.3"W P-DIP | DRAWING NO: CO 0035 | REV: 0

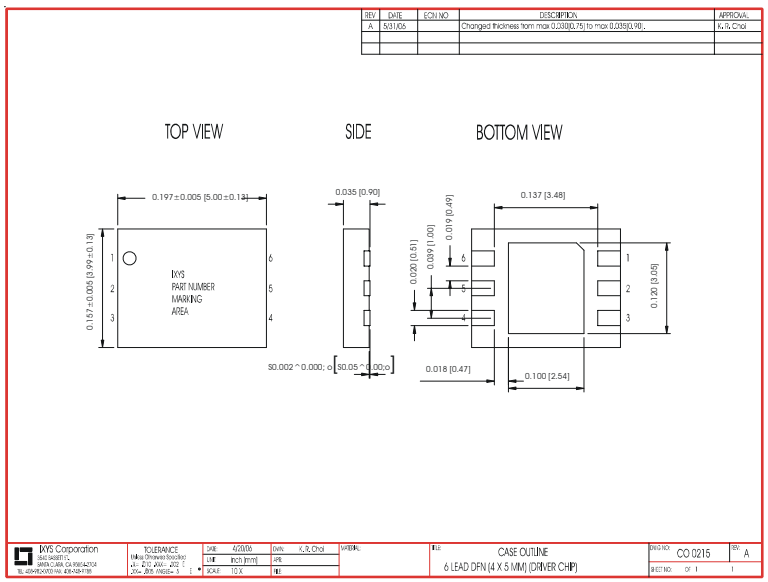


REV	DATE	ECN NO	DESCRIPTION	APR
A	3/08/2		Added bottom heatslug dimension.	K. R. Choi

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
M	.135	.155	3.43	3.94
N	.095	.115	2.41	2.92
α	0°	8°	0°	8°

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

IXYS Corp, 3540 Bassett St, Santa Clara, CA 95054 | TOLERANCE: Unless Otherwise Specified .X= +/-0.05 .XXX= +/-0.005 .XX= +/-0.01 ANGLE= +/-5 | DATE: 1/24/95 | DWN: K. R. Choi | UNIT: INCH [MM] | APR: | SCALE: 5X | APR: | TITLE: CASE OUTLINE SOP-8 (.150"W) | DRAWING NO: CO 0044 | REV: A



REV	DATE	ECN NO	DESCRIPTION	APPROVAL
A	5/31/06		Changed thickness from max 0.038[0.75] to max 0.035[0.90].	K. R. Choi

TOP VIEW SIDE BOTTOM VIEW

IXYS Corporation | TOLERANCE: Unless Otherwise Specified .X= ±0.10 .XXX= ±0.02 .XXX= ±0.005 ANGLE= ± 1 | DATE: 4/20/06 | DWN: K. R. Choi | UNIT: inch [mm] | APR: | SCALE: 10 X | MATERIAL: | TITLE: CASE OUTLINE 6 LEAD DFN (4 X 5 MM) (DRIVER CHIP) | DRAWING NO: CO 0215 | REV: A | SHEET NO: 1 OF 1

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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