

**NPN Silicon RF Transistor\***

- For low current applications
- Smallest Package 1.4 x 0.8 x 0.59 mm
- Noise figure  $F = 1.25$  dB at 1.8 GHz outstanding  $G_{ms} = 23$  dB at 1.8 GHz
- Transition frequency  $f_T = 25$  GHz
- Gold metallization for high reliability
- SIEGET ® 25 GHz fT - Line
- Pb-free (RoHS compliant) package<sup>1)</sup>
- Qualified according AEC Q101

\* Short term description



**ESD (Electrostatic discharge) sensitive device, observe handling precaution!**

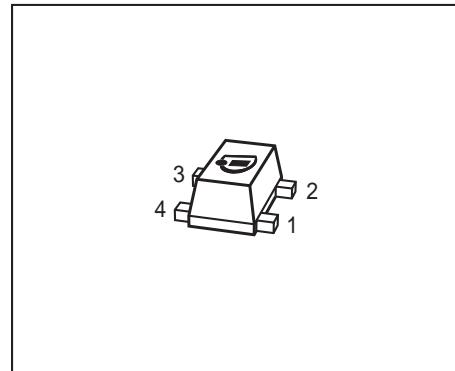
Type	Marking	Pin Configuration						Package
BFP405F	ALs	1=B	2=E	3=C	4=E	-	-	TSFP-4

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-emitter voltage $T_A > 0$ °C	$V_{CEO}$	4.5	V
$T_A \leq 0$ °C		4.1	
Collector-emitter voltage	$V_{CES}$	15	
Collector-base voltage	$V_{CBO}$	15	
Emitter-base voltage	$V_{EBO}$	1.5	
Collector current	$I_C$	12	mA
Base current	$I_B$	1	
Total power dissipation <sup>2)</sup> $T_S \leq 122$ °C	$P_{tot}$	55	mW
Junction temperature	$T_j$	150	°C
Ambient temperature	$T_A$	-65 ... 150	
Storage temperature	$T_{stq}$	-65 ... 150	

<sup>1</sup>Pb-containing package may be available upon special request

<sup>2</sup> $T_S$  is measured on the collector lead at the soldering point to the pcb



**Thermal Resistance**

Parameter	Symbol	Value	Unit
Junction - soldering point <sup>1)</sup>	$R_{thJS}$	$\leq 500$	K/W

**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

**DC Characteristics**

Collector-emitter breakdown voltage $I_C = 1 \text{ mA}, I_B = 0$	$V_{(\text{BR})\text{CEO}}$	4	5	-	V
Collector-emitter cutoff current $V_{CE} = 15 \text{ V}, V_{BE} = 0$	$I_{CES}$	-	-	10	$\mu\text{A}$
Collector-base cutoff current $V_{CB} = 5 \text{ V}, I_E = 0$	$I_{CBO}$	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 0.5 \text{ V}, I_C = 0$	$I_{EBO}$	-	-	1	$\mu\text{A}$
DC current gain $I_C = 5 \text{ mA}, V_{CE} = 4 \text{ V}$ , pulse measured	$h_{FE}$	60	95	130	-

<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>AC Characteristics</b> (verified by random sampling)					
Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 3 \text{ V}, f = 2 \text{ GHz}$	$f_T$	18	25	-	GHz
Collector-base capacitance $V_{CB} = 2 \text{ V}, f = 1 \text{ MHz}, V_{BE} = 0 \text{ V}$ , emitter grounded	$C_{cb}$	-	0.05	0.1	pF
Collector emitter capacitance $V_{CE} = 2 \text{ V}, f = 1 \text{ MHz}, V_{BE} = 0 \text{ V}$ , base grounded	$C_{ce}$	-	0.2	-	
Emitter-base capacitance $V_{EB} = 0.5 \text{ V}, f = 1 \text{ MHz}, V_{CB} = 0 \text{ V}$ , collector grounded	$C_{eb}$	-	0.25	-	
Noise figure $I_C = 2 \text{ mA}, V_{CE} = 2 \text{ V}, f = 1.8 \text{ GHz}, Z_S = Z_{Sopt}$	$F$	-	1.25	-	dB
Power gain, maximum stable <sup>1)</sup> $I_C = 5 \text{ mA}, V_{CE} = 2 \text{ V}, Z_S = Z_{Sopt}$ , $Z_L = Z_{Lopt}, f = 1.8 \text{ GHz}$	$G_{ms}$	-	22.5	-	dB
Insertion power gain $V_{CE} = 2 \text{ V}, I_C = 5 \text{ mA}, f = 1.8 \text{ GHz}$ , $Z_S = Z_L = 50 \Omega$	$ S_{21} ^2$	-	18	-	
Third order intercept point at output <sup>2)</sup> $V_{CE} = 2 \text{ V}, I_C = 5 \text{ mA}, f = 1.8 \text{ GHz}$ , $Z_S = Z_L = 50 \Omega$	$IP_3$	-	14	-	dBm
1dB Compression point at output $I_C = 5 \text{ mA}, V_{CE} = 2 \text{ V}, Z_S = Z_L = 50 \Omega$ , $f = 1.8 \text{ GHz}$	$P_{-1\text{dB}}$	-	0	-	

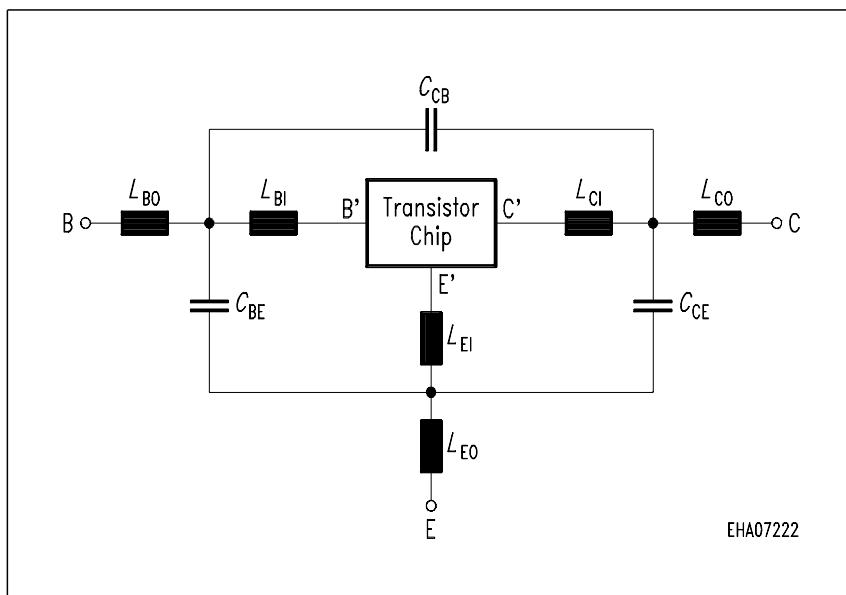
<sup>1</sup> $G_{ms} = |S_{21}| / S_{12}|$ 
<sup>2</sup>IP3 value depends on termination of all intermodulation frequency components.  
Termination used for this measurement is  $50\Omega$  from 0.1 MHz to 6 GHz

**SPICE Parameter (Gummel-Poon Model, Berkley-SPICE 2G.6 Syntax):**
**Transistor Chip Data:**

IS =	0.21024	fA	BF =	83.23	-	NF =	1.0405	-
VAF =	39.251	V	IKF =	0.16493	A	ISE =	15.761	fA
NE =	1.7763	-	BR =	10.526	-	NR =	0.96647	-
VAR =	34.368	V	IKR =	0.25052	mA	ISC =	0.037223	fA
NC =	1.3152	-	RB =	15	$\Omega$	IRB =	0.21215	mA
RBM =	1.3491	$\Omega$	RE =	1.9289	-	RC =	0.12691	$\Omega$
CJE =	3.7265	fF	VJE =	0.70367	V	MJE =	0.37747	-
TF =	4.5899	ps	XTF =	0.3641	-	VTF =	0.19762	V
ITF =	1.3364	A	PTF =	0	deg	CJC =	96.941	fF
VJC =	0.99532	V	MJC =	0.48652	-	XCJC =	0.08161	-
TR =	1.4935	ns	CJS =	0	fF	VJS =	0.75	V
MJS =	0	-	XTB =	0	-	EG =	1.11	eV
XTI =	3	-	FC =	0.99469		TNOM	300	K

**C`-E`-dioden Data (Berkley-Spice 1G.6 Syntax):** IS = 2 fA; N = 1.02 - , RS = 20  $\Omega$ 

All parameters are ready to use, no scaling is necessary.

**Package Equivalent Circuit:**


$L_{BO}$ =	0.22	nH
$L_{EO}$ =	0.28	nH
$L_{CO}$ =	0.22	nH
$L_{BI}$ =	0.42	nH
$L_{EI}$ =	0.26	nH
$L_{CI}$ =	0.35	nH
$C_{BE}$ =	34	fF
$C_{BC}$ =	2	fF
$C_{CE}$ =	33	fF
$K_{BO-EO}$ =	0.1	-
$K_{BO-CO}$ =	0.01	-
$K_{EO-CO}$ =	0.11	-
$K_{CI-EI}$ =	-0.05	-
$K_{BI-CI}$ =	-0.08	-
$K_{BI-EI}$ =	0.2	-
$R_{LBI}$ =	0.15	$\Omega$
$R_{LEI}$ =	0.11	$\Omega$
$R_{LCI}$ =	0.13	$\Omega$

Valid up to 6GHz

The TSFP-4 package has two emitter leads. To avoid high complexity for the package equivalent circuit, both leads are combined in one electrical connection.

RLXI are series resistors for the inductances LxI and  $K_{xa-by}$  are the coupling coefficients between the inductances  $L_{ax}$  and  $L_{yb}$ . The reference pin for the couple ports are B, E, C, B', E', C

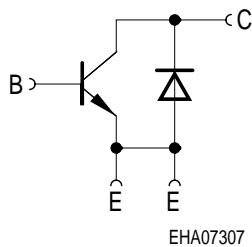
For examples and ready to use parameters please contact your local Infineon Technologies distributor or sales office to obtain a InfineonTechnologies CD-ROM or see Internet:  
<http://www.infineon.com/silicondiscretes>

**For non-linear simulation:**

- Use transistor chip parameters in Berkeley SPICE 2G.6 syntax for all simulators.
- If you need simulation of the reverse characteristics, add the diode with the C'-E'- diode data between collector and emitter.
- Simulation of package is not necessary for frequencies < 100MHz.  
For higher frequencies add the wiring of package equivalent circuit around the non-linear transistor and diode model.

**Note:**

- This transistor is constructed in a common emitter configuration. This feature causes an additional reverse biased diode between emitter and collector, which does not effect normal operation.

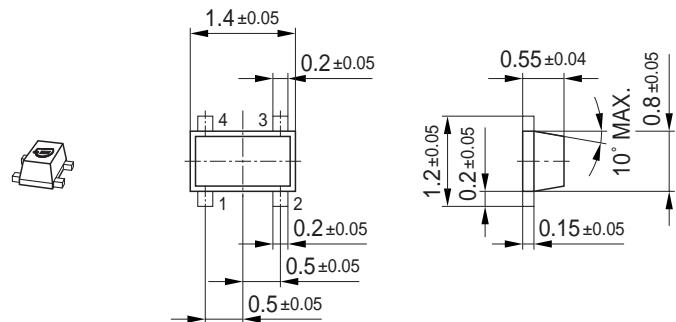
**Transistor Schematic Diagram**

The common emitter configuration shows the following advantages:

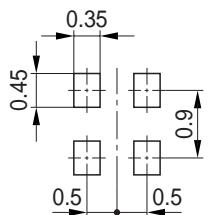
- Higher gain because of lower emitter inductance.
- Power is dissipated via the grounded emitter leads, because the chip is mounted on copper emitter leadframe.

Please note, that the broadest lead is the emitter lead.

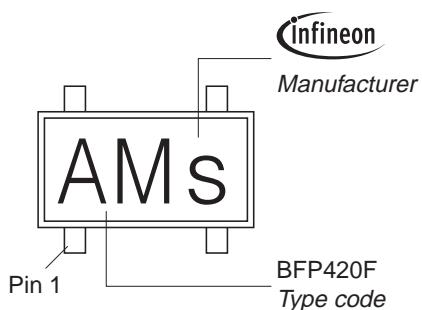
## Package Outline



## Foot Print

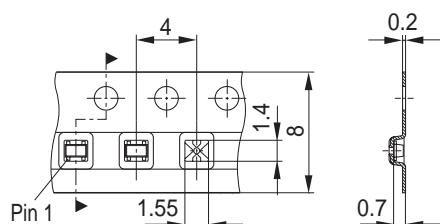


## Marking Layout (Example)



## Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel  
 Reel ø330 mm = 10.000 Pieces/Reel



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