

## 8-Pin, 8-Bit Flash Microcontroller Product Brief

### High-Performance RISC CPU:

- Only 35 single-word instructions to learn
- All single-cycle instructions except for program branches which are two-cycle
- Eight-level deep hardware stack
- Direct, Indirect and Relative Addressing modes for data and instructions
- Operating speed:
  - DC – 20 MHz clock input
  - DC – 200 ns instruction cycle

### Special Microcontroller Features:

- Program Memory Read Capability
- Program Memory Write Capability
- Precision Internal Oscillator:
  - Selectable 4 MHz or 8 MHz frequency
  - Factory calibrated to  $\pm 1\%$
- Power-saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT) with dedicated on-chip RC oscillator for reliable operation
- Multiplexed MCLR input pin with internal pull-up
- Programmable code protection
- Selectable oscillator options:
  - INTOSC: Precision internal oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power-saving, low-frequency crystal
  - EC: High-speed external clock input
- In-Circuit Serial Programming™ (ICSP™)
- Programmable Interrupt-on-Change pins

### Low-Power Features

- Operating current:
  - 130  $\mu\text{A}$  @ 2V, 1 MHz, typical
  - 240  $\mu\text{A}$  @ 2V, 4 MHz, typical
- Standby current:
  - 50 nA @ 2V, typical
- Watchdog Timer current:
  - 1  $\mu\text{A}$  @ 2V, typical

### CMOS Technology:

- Low-power, high-speed Flash technology:
  - 100,000 Flash endurance
  - > 40-year retention
- Fully static design
- Wide operating voltage range: 2.0V – 5.5V
- Wide temperature range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

### Peripheral Features:

- I/O pins:
  - 5 I/O pins with individual direction control
  - 1 input-only pin
  - Individually selectable weak pull-ups
  - High current sink/source for direct LED drive
- Analog-to-Digital (A/D) Converter:
  - 10-bit resolution
  - 4 external channels
  - 3 internal channels to convert internal voltage references
- Analog Comparator:
  - One comparator
  - Comparator inputs and output accessible externally
  - On-chip 0.6V absolute voltage reference
  - Programmable on-chip voltage reference (CVREF) module (% of VDD)
- Timer0 module: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1 module:
  - 16-bit timer/counter with prescaler
  - External gate input
  - Option to use OSC1/OSC2 input in LP mode as Timer1 oscillator when in INTOSC mode
  - Option to use system clock source as Timer1 clock input
- Timer2 module: 8-bit timer/counter with 8-bit prescaler and postscaler
- Enhanced Capture Compare/PWM module (ECCP):
  - User selectable simultaneous PWM and complementary PWM output for bridge drive applications
  - 16-bit capture maximum resolution 12.5 ns
  - Compare maximum resolution 200 ns
  - 10-bit PWM maximum frequency 20 kHz

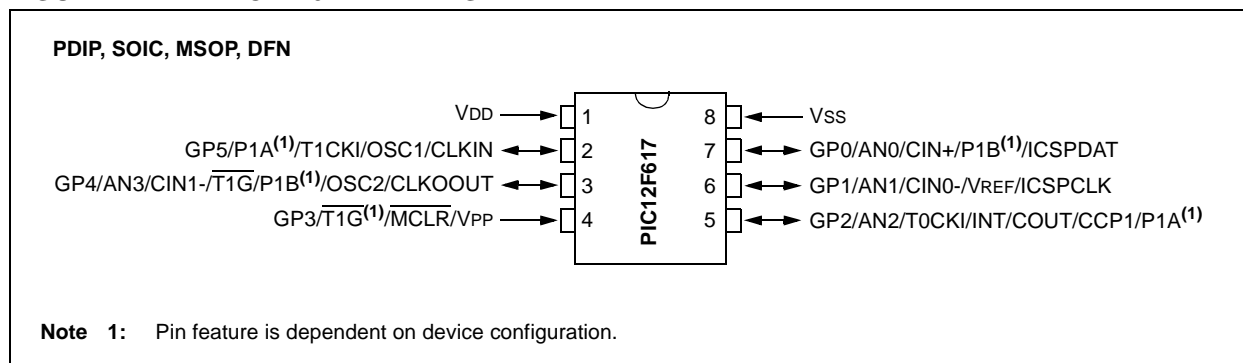
# PIC12F617

**TABLE 1: PIC12F617 FEATURE SUMMARY**

| Device    | Program Memory Flash (Words) | Self Read/ Self Write | SRAM (bytes) | I/O | Timers 8/16 bit | 10-bit A/D Channels | Comparators | ECCP |
|-----------|------------------------------|-----------------------|--------------|-----|-----------------|---------------------|-------------|------|
| PIC12F617 | 2048 x 14                    | Yes/Yes               | 128          | 6   | 2/1             | 4                   | 1           | Yes  |

**Note:** Pin details are subject to change.

**FIGURE 1: PIC12F617 PIN DIAGRAM**



**TABLE 2: PIC12F617 PIN SUMMARY (PDIP, SOIC, MSOP, DFN)**

| I/O | 8-pin PDIP, SOIC, MSOP, DFN | A/D | Reference | Comparator | Timers             | ECCP                      | Pull-up          | Interrupt  | Basic       |
|-----|-----------------------------|-----|-----------|------------|--------------------|---------------------------|------------------|------------|-------------|
| GP0 | 7                           | AN0 | —         | CIN+       | —                  | P1B <sup>(1)</sup>        | Y                | IOC        | ICSPDAT     |
| GP1 | 6                           | AN1 | VREF      | CIN0-      | —                  | —                         | Y                | IOC        | ICSPCLK     |
| GP2 | 5                           | AN2 | —         | COU        | T0CKI              | CCP1 / P1A <sup>(1)</sup> | Y                | INT<br>IOC | —           |
| GP3 | 4                           | —   | —         | —          | T1G <sup>(1)</sup> | —                         | Y <sup>(2)</sup> | IOC        | MCLR/VPP    |
| GP4 | 3                           | AN3 | —         | CIN1-      | T1G <sup>(1)</sup> | P1B <sup>(1)</sup>        | Y                | IOC        | OSC2/CLKOUT |
| GP5 | 2                           | —   | —         | —          | T1CKI              | P1A <sup>(1)</sup>        | Y                | IOC        | OSC1/CLKIN  |
| VDD | 1                           | —   | —         | —          | —                  | —                         | —                | —          | —           |
| VSS | 8                           | —   | —         | —          | —                  | —                         | —                | —          | —           |

**Note 1:** Pin feature is dependent on device configuration.

**2:** Pull-up only available when pin is configured as MCLR.

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