IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

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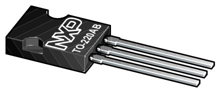

BT148-600R

SCR

13 March 2014 **Product data sheet**

1. General description

Planar passivated SCR with sensitive gate in a SIP3 (SOT82) plastic package intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs

3. Applications

- Adapters
- Battery powered applications
- Industrial automation

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	35	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; T_{mb} ≤ 113 °C; Fig. 2; Fig. 3		-	-	4	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	15	200	µA

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

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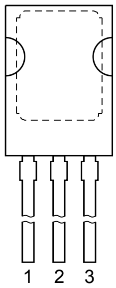
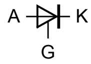
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 SIP3 (SOT82)	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT148-600R	SIP3	plastic single-ended package; 3 leads (in-line)	SOT82

7. Limiting values

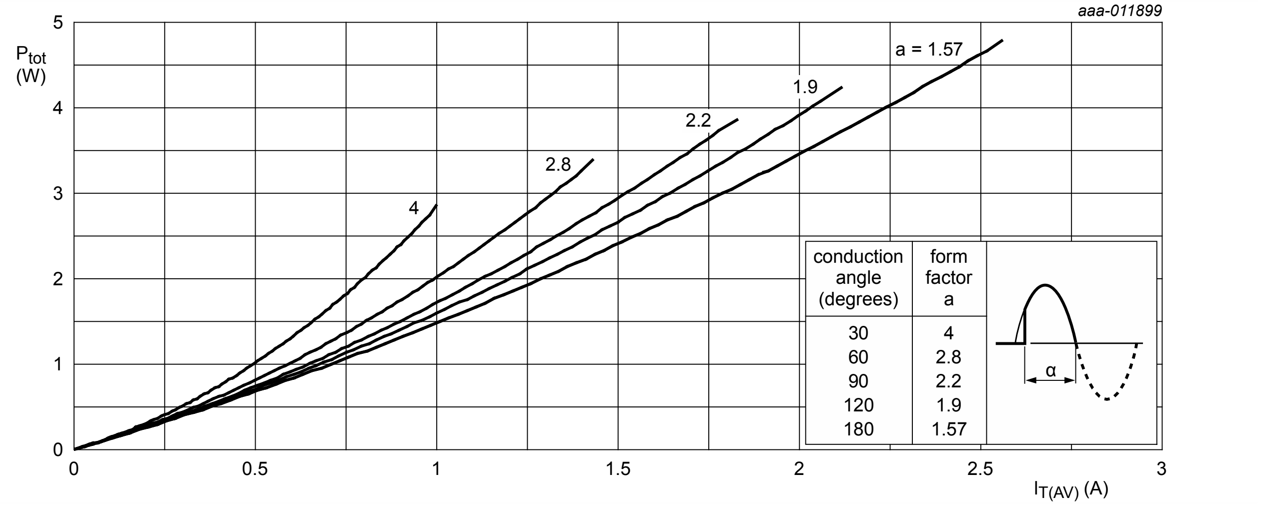
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; T_{mb} ≤ 113 °C; Fig. 1		-	2.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; T_{mb} ≤ 113 °C; Fig. 2; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	35	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	38	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	6.1	A^2s
dI_T/dt	rate of rise of on-state current	I_T = 10 A; I_G = 50 mA; dI_G/dt = 50 mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature		[2]	-	125	°C

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

[2] Operation above 110˚C may require the use of a gate to cathode resistor of 1kΩ or less.



α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

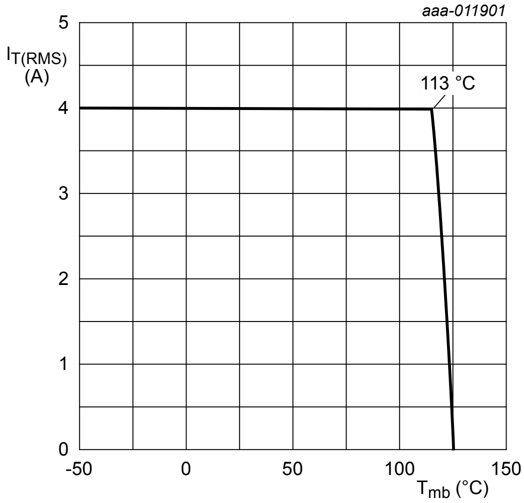
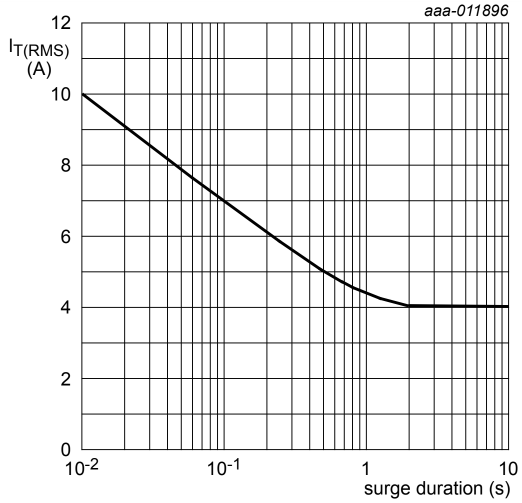
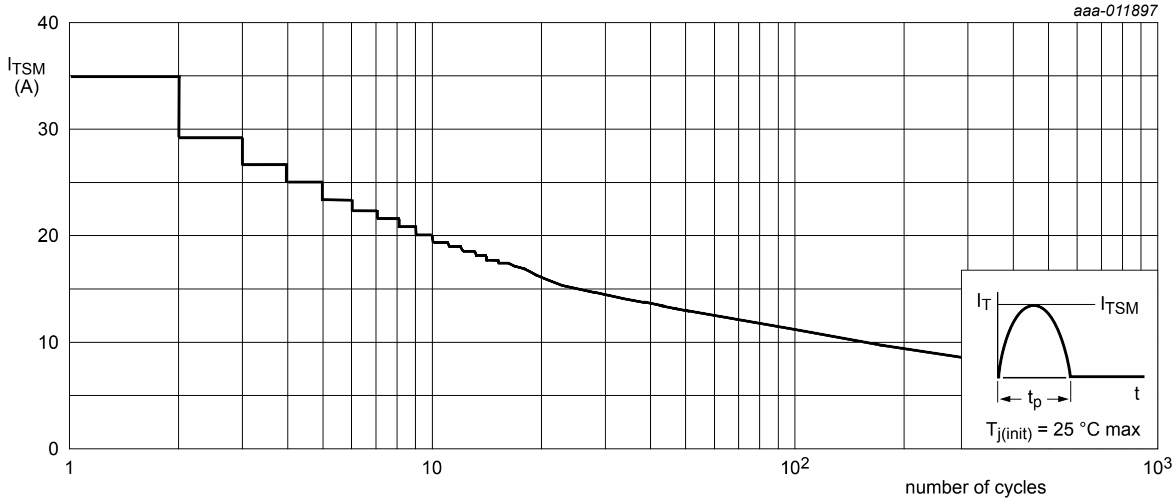


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



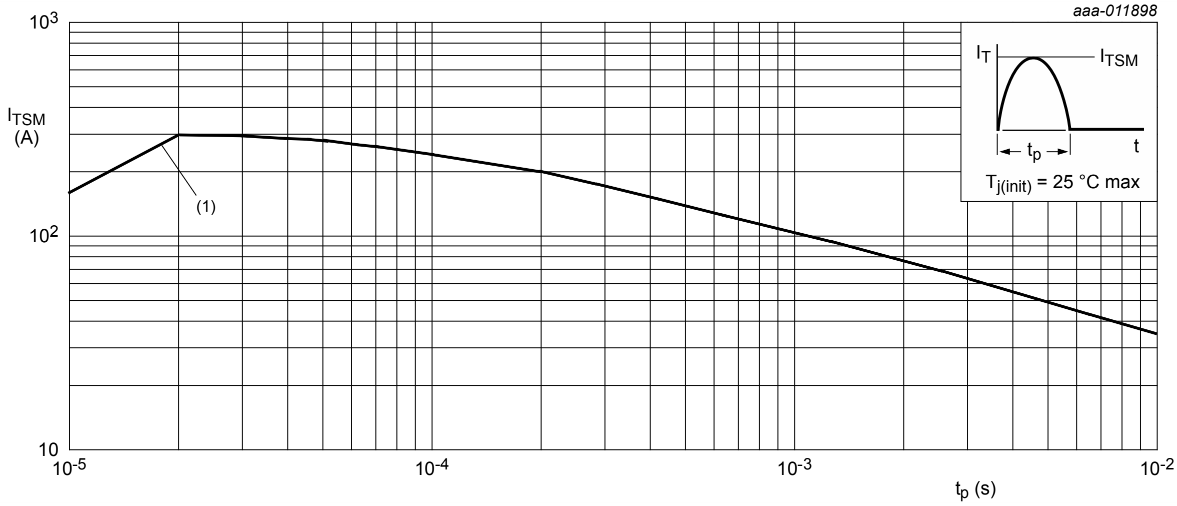
f = 50 Hz; T_{mb} = 113 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	2.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	95	-	K/W

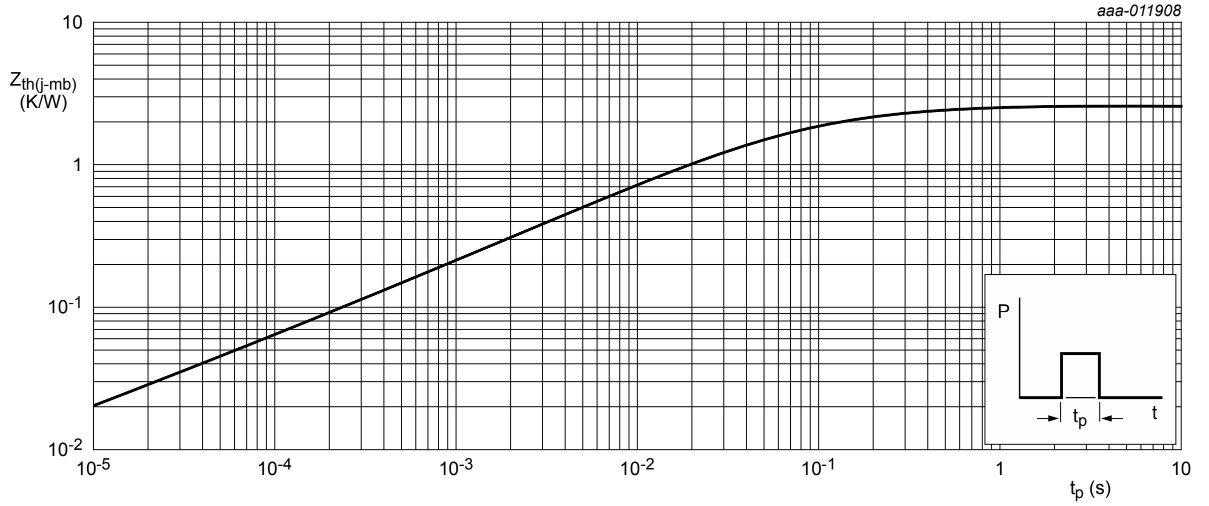


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	15	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	0.17	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	0.1	6	mA
V_T	on-state voltage	I_T = 5 A; T_j = 25 °C; Fig. 10		-	1.23	1.8	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.4	1	V
		V_D = 600 V; I_T = 0.1 A; T_j = 110 °C; Fig. 11		0.1	0.2	-	V
I_D	off-state current	V_D = 600 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 600 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		-	50	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 10 A; V_D = 600 V; I_G = 5 mA; dI_G/dt = 0.2 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 402 V; T_j = 125 °C; I_{TM} = 8 A; V_R = 10 V; $(dI_T/dt)_M$ = 10 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

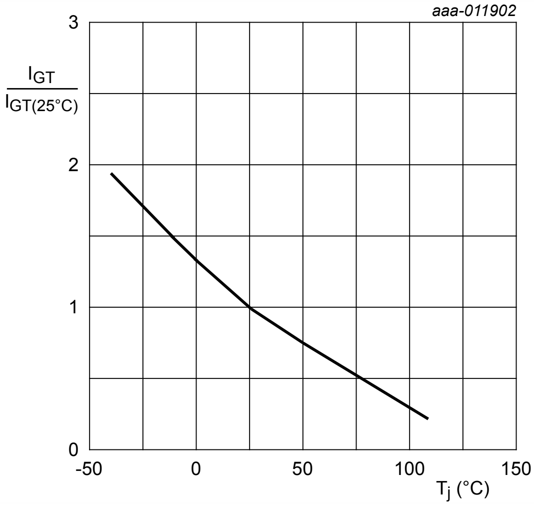
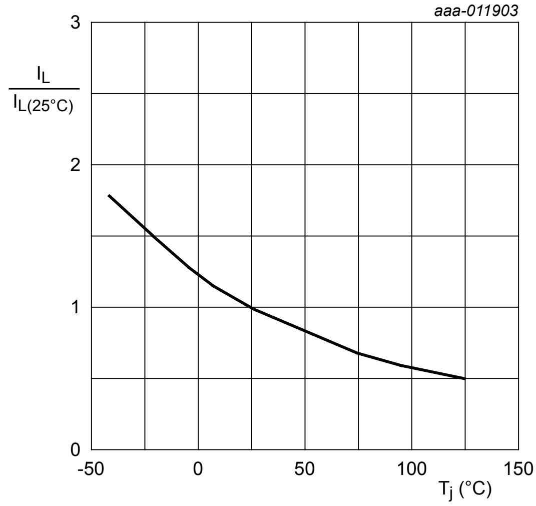
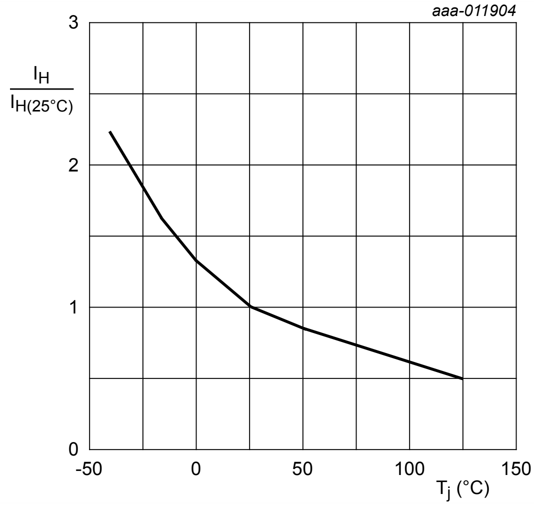


Fig. 7. Normalized gate trigger current as a function of junction temperature



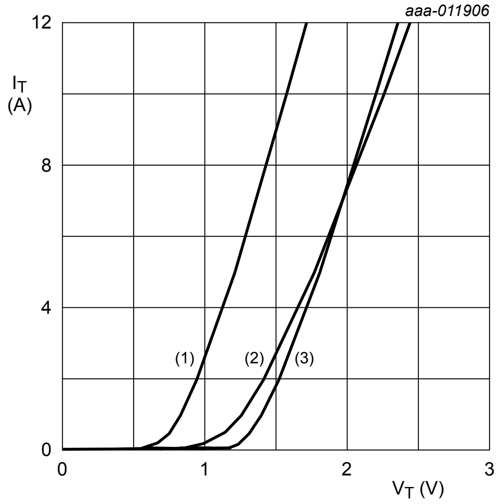
R_{GK} = 1 kΩ

Fig. 8. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.26 V; R_s = 0.099 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

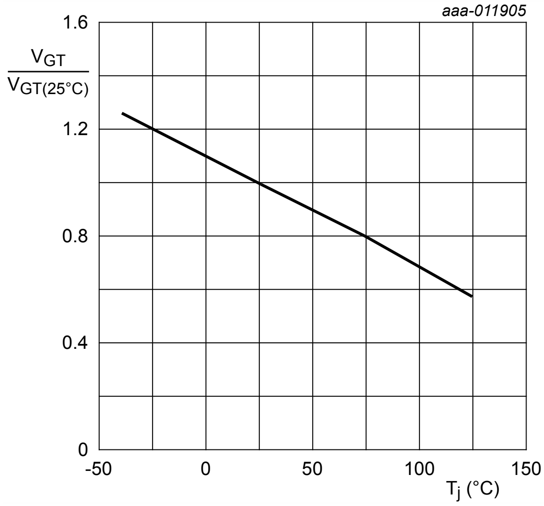
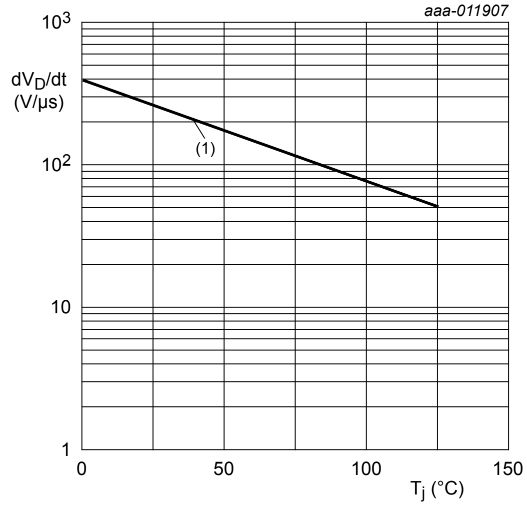


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

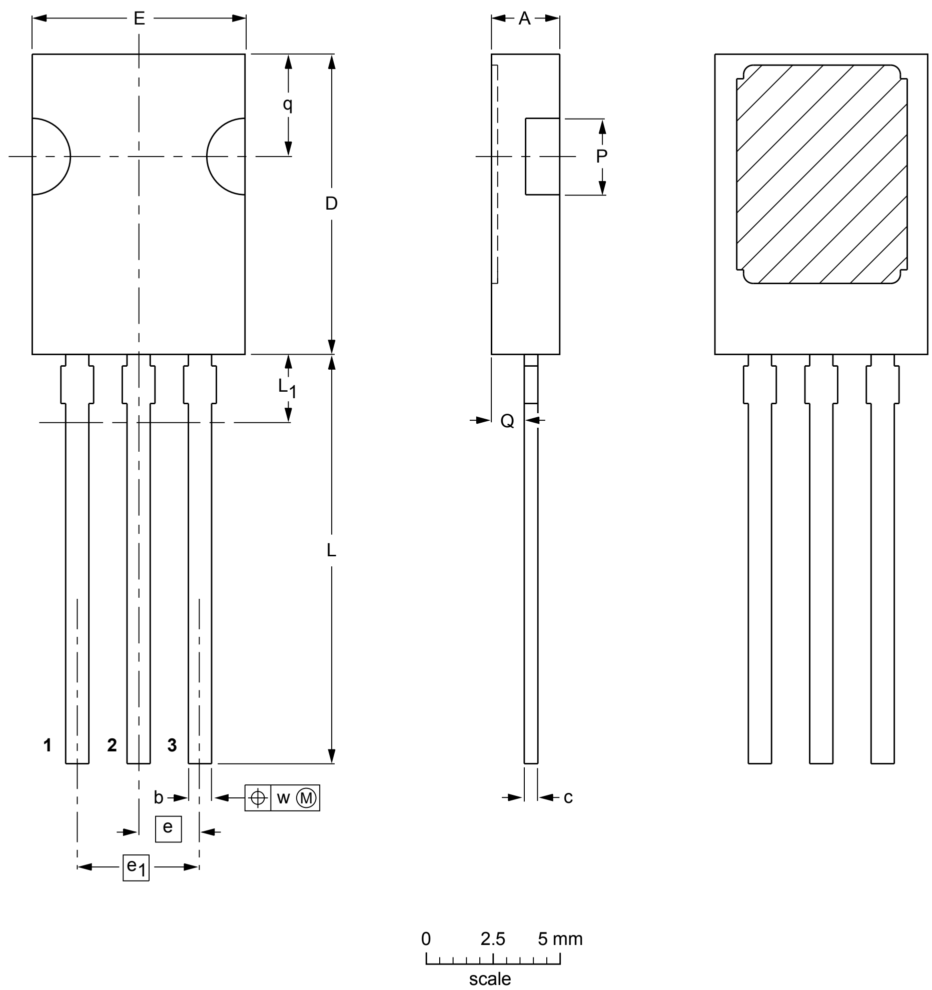


(1) R_{GK} = 100 Ω

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

Plastic single-ended package; 3 leads (in-line) **SOT82**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	e_1	L	L_1(1) max.	P	Q	q	w
mm	2.8 2.3	0.88 0.65	0.58 0.47	11.1 10.5	7.8 7.2	2.29	4.58	16.5 15.3	2.54	3.1 2.5	1.5 0.9	3.9 3.5	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT82						97-06-11

Fig. 13. Package outline SIP3 (SOT82)

11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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