



VND10N06 VND10N06-1

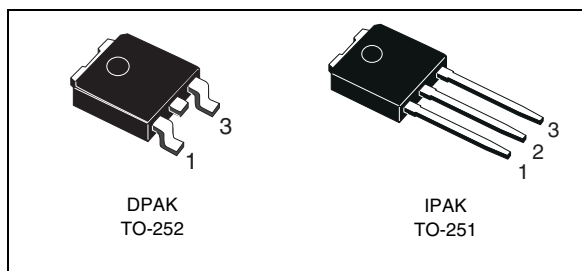
"OMNIFET"

fully autoprotected Power MOSFET

Features

Max on-state resistance (per ch.)	$R_{DS(on)}$	0.3 Ω
Current limitation (typ)	I_{lim}	10A
Drain-Source clamp voltage	V_{CLAMP}	60V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Logic level input threshold
- ESD protection
- Schmitt trigger on input
- High noise immunity



Description

The VND10N06 and VND10N06-1 are monolithic devices designed in STMicroelectronics VIPower M0-2 technology, intended for replacement of standard Power MOSFETs in DC to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
DPAK	VND10N06	VND10N06TR
IPAK	VND10N06-1	

Contents

1	Block diagram and pin description	5
2	Electrical specifications	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	6
2.3	Electrical characteristics	7
2.4	Electrical characteristics curves	12
3	Protection features	16
4	Thermal data	17
5	Package and packing information	18
5.1	ECOPACK® packages	18
5.2	DPAK mechanical data	18
5.3	IPAK mechanical data	20
5.4	DPAK packing information	21
5.5	IPAK packing information	23
6	Revision history	24

List of tables

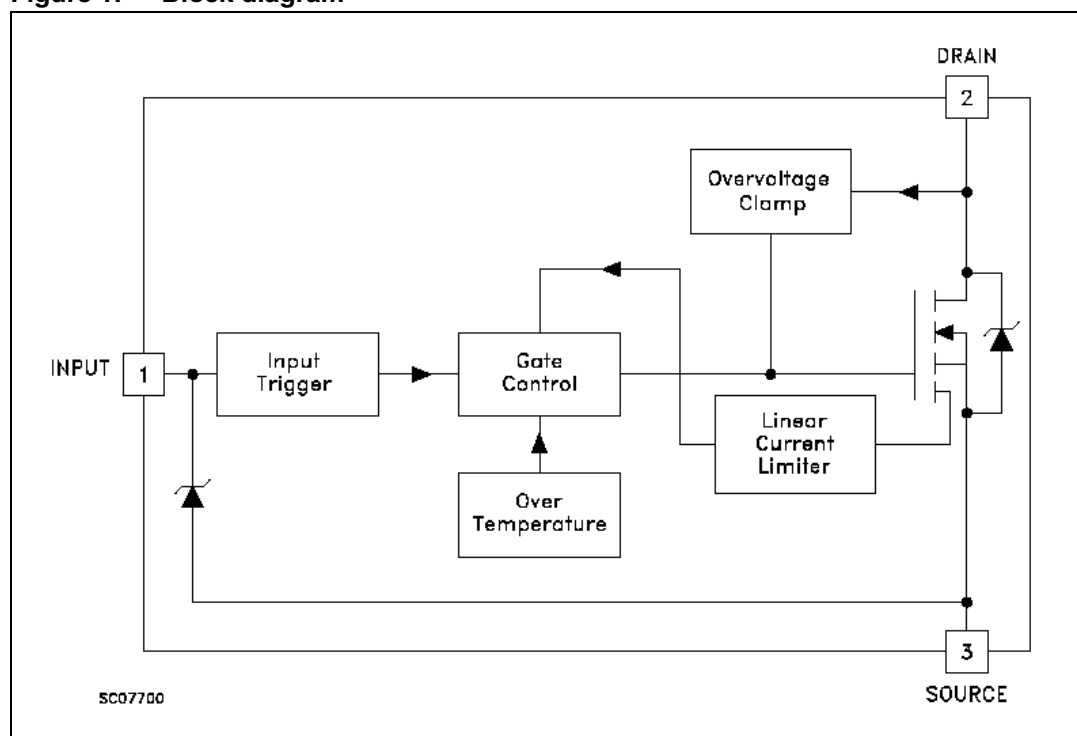
Table 1.	Device summary	1
Table 2.	Absolute maximum ratings	6
Table 3.	Thermal data.	6
Table 4.	Off	7
Table 5.	Switching	7
Table 6.	On	7
Table 7.	Dynamic	8
Table 8.	Source Drain diode	8
Table 9.	Protections (-40°C < T _j < 150°C, unless otherwise specified)	8
Table 10.	DPAK mechanical data	19
Table 11.	IPAK mechanical data	20
Table 12.	Document revision history	24

List of figures

Figure 1.	Block diagram	5
Figure 2.	Switching waveforms	8
Figure 3.	Switching time test circuit for resistive load	9
Figure 4.	Test circuit for inductive load switching and diode recovery time	9
Figure 5.	Unclamped inductive load test circuits	10
Figure 6.	Input charge test circuit.	10
Figure 7.	Unclamped inductive waveforms	11
Figure 8.	Static Drain-Source on resistance ($V_{IN} = 3.5V$)	12
Figure 9.	Static Drain-Source on resistance ($V_{IN} = 5V$)	12
Figure 10.	Derating curve	12
Figure 11.	Static Drain-Source on resistance vs. input voltage	12
Figure 12.	Current limit Vs. junction temperature	12
Figure 13.	Source-Drain diode voltage Vs. junction temperature	12
Figure 14.	Step response current limit.	13
Figure 15.	Switching time resistive load.	13
Figure 16.	Turn-on current slope ($V_{IN} = 3.5V$)	13
Figure 17.	Turn-on current slope ($V_{IN} = 7V$)	13
Figure 18.	Input voltage Vs. input charge	13
Figure 19.	Turn-off Drain-Source voltage slope.	13
Figure 20.	Turn-off Drain-Source voltage slope.	14
Figure 21.	Capacitance variations	14
Figure 22.	Switching time resistive load.	14
Figure 23.	Normalized on resistance Vs. temperature ($V_{IN} = 7V$)	14
Figure 24.	Output characteristics	14
Figure 25.	Normalized on resistance Vs. temperature ($V_{IN} = 3.5V$)	14
Figure 26.	Normalized input threshold voltage Vs. temperature	15
Figure 27.	Thermal impedance for DPAK / IPAK.	17
Figure 28.	DPAK package dimensions	18
Figure 29.	IPAK mechanical data and package outline	20
Figure 30.	DPAK footprint	21
Figure 31.	DPAK tube shipment (no suffix)	21
Figure 32.	DPAK tape and reel shipment (suffix "TR")	22
Figure 33.	IPAK tube shipment (no suffix)	23

1 Block diagram and pin description

Figure 1. Block diagram



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-Source voltage ($V_{in} = 0V$)	Internally clamped	V
V_{INn}	Input voltage	Internally clamped	V
I_{in}	Input current	± 20	mA
I_{Dn}	Drain current	Internally limited	A
I_{Rn}	Reverse DC output current	- 15	A
V_{ESD}	Electrostatic discharge ($R = 1.5K\Omega$, $C = 100pF$)	4000	V
P_{tot}	Total dissipation at $T_c = 25^\circ C$	35	W
T_j	Operating junction temperature	Internally limited	$^\circ C$
T_c	Case operating temperature	Internally limited	$^\circ C$
T_{stg}	Storage temperature	- 55 to 150	$^\circ C$

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.5	$^\circ C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	100	$^\circ C/W$

2.3 Electrical characteristics

T_{case} = 25 °C unless otherwise stated.

Table 4. Off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CLAMP}	Drain-Source clamp voltage	V _{IN} = 0V; I _D = 200mA	50	60	70	V
V _{IL}	Input low level voltage	I _D = 100 µA; V _{DS} = 16 V			1.5	V
V _{IH}	Input high Level voltage	R _L = 27Ω; V _{DD} = 16 V V _{DS} = 0.5 V	3.2			V
I _{ISS}	Supply current from input pin	V _{DS} = 0V; V _{IN} = 5V		150	300	µA
V _{INCL}	Input-Source reverse clamp voltage	I _{IN} = -1mA I _{IN} = 1mA	-1 8		-0.3 11	V V
I _{DSS}	Zero input voltage drain current (V _{IN} = 0V)	V _{DS} = 50V; V _{IN} = V _{IL} ; V _{DS} < 35V; V _{IN} = V _{IL}			250 100	µA µA

Table 5. Switching⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 16V; I _D = 1A V _{gen} = 7V; R _{gen} = 10Ω (see Figure 2)		1100	1600	ns
t _r	Rise time			550	900	ns
t _{d(off)}	Turn-off delay time			200	400	ns
t _f	Fall time			100	200	ns
t _{d(on)}	Turn-on delay time	V _{DD} = 16V; I _D = 1A V _{gen} = 7V; R _{gen} = 1000Ω (see Figure 2)		1.2	1.8	µs
t _r	Rise time			1	1.5	µs
t _{d(off)}	Turn-off delay time			1.6	2.3	µs
t _f	Fall time			1.2	1.8	µs
(di/dt) _{on}	Turn-on current slope	V _{DD} = 16V; I _D = 1A V _{in} = 7V; R _{gen} = 10Ω		1.5		A/µs
Q _i	Total input charge	V _{DD} = 12V; I _D = 1A; V _{IN} = 7V		13		nC

1. Parameters guaranteed by design / characterization.

Table 6. On⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{DS(on)}	Static Drain-Source on resistance	V _{IN} = 7V; I _D = 1 A; T _j < 125 °C		0.15	0.3	Ω

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%.

Table 7. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{OSS}	Output capacitance	$V_{DS} = 13V$; $f = 1MHz$; $V_{IN} = 0V$		350	500	pF

Table 8. Source Drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 1A$; $V_{IN} = V_{IL}$		0.8	1.6	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 1A$; $di/dt = 100A/\mu s$ $V_{DD} = 30V$; $T_j = 25^\circ C$ (see Figure 4)		125		ns
$Q_{rr}^{(2)}$	Reverse recovery charge			0.22		μC
$I_{RRM}^{(2)}$	Reverse recovery current			3.5		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.
2. Parameters guaranteed by design / characterization.

Table 9. Protections ($-40^\circ C < T_j < 150^\circ C$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain current limit	$V_{IN} = 7V$; $V_{DS}=13V$	6	10	15	A
$t_{dlim}^{(1)}$	Step response current limit	$V_{IN} = 7V$; V_{DS} step from 0 to 13V		12	20	μs
$T_{jsh}^{(1)}$	Overtemperature shutdown		150			$^\circ C$
$T_{jrs}^{(1)}$	Overtemperature reset		135			$^\circ C$
$E_{as}^{(1)}$	Single pulse avalanche energy	Starting $T_j = 25^\circ C$; $V_{DD} = 24V$ $V_{IN} = 7V$ $R_{gen} = 1k\Omega$; $L = 10mH$	250			mJ

1. Parameters guaranteed by design / characterization.

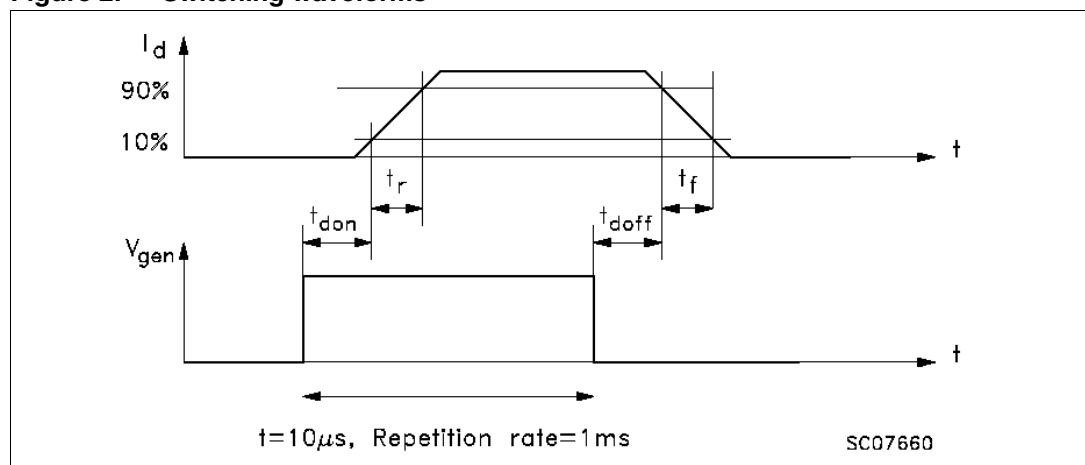
Figure 2. Switching waveforms

Figure 3. Switching time test circuit for resistive load

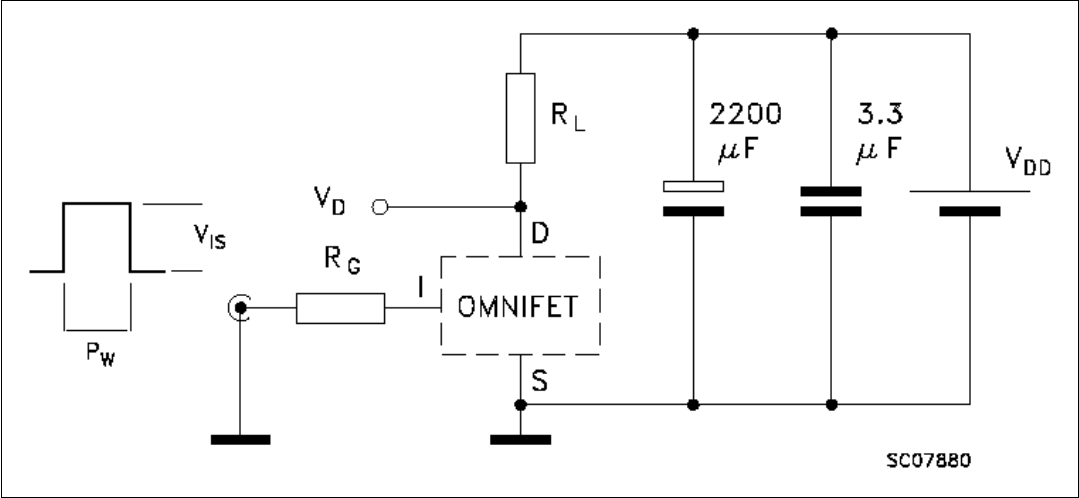


Figure 4. Test circuit for inductive load switching and diode recovery time

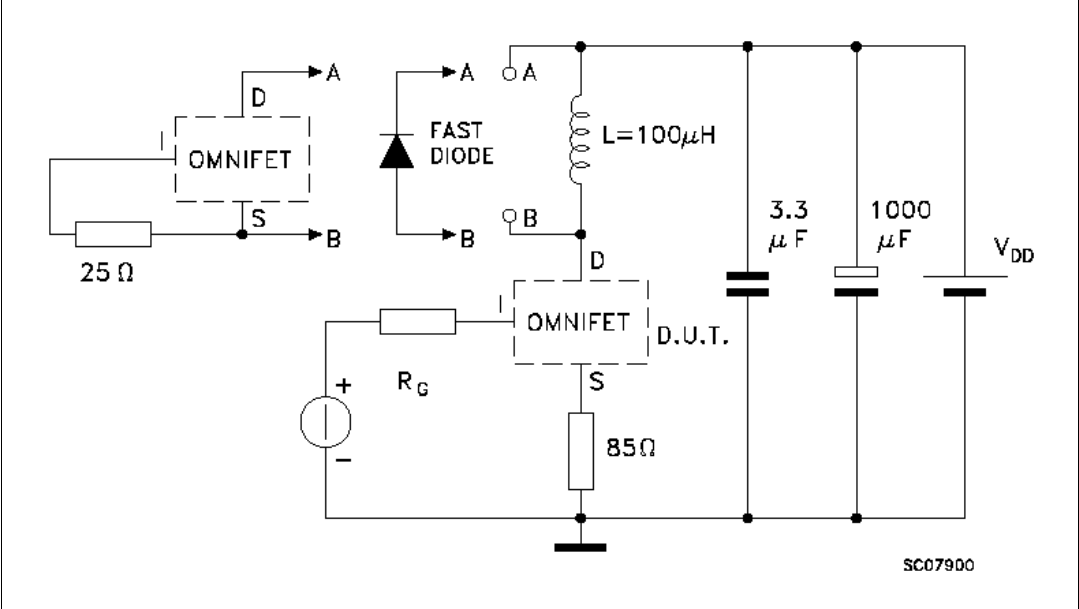


Figure 5. Unclamped inductive load test circuits

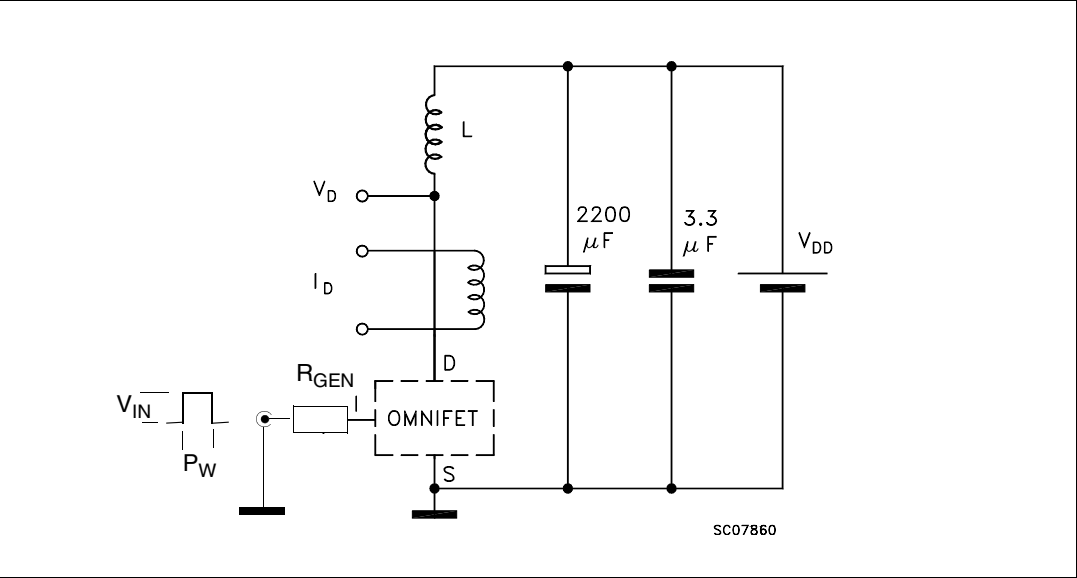


Figure 6. Input charge test circuit

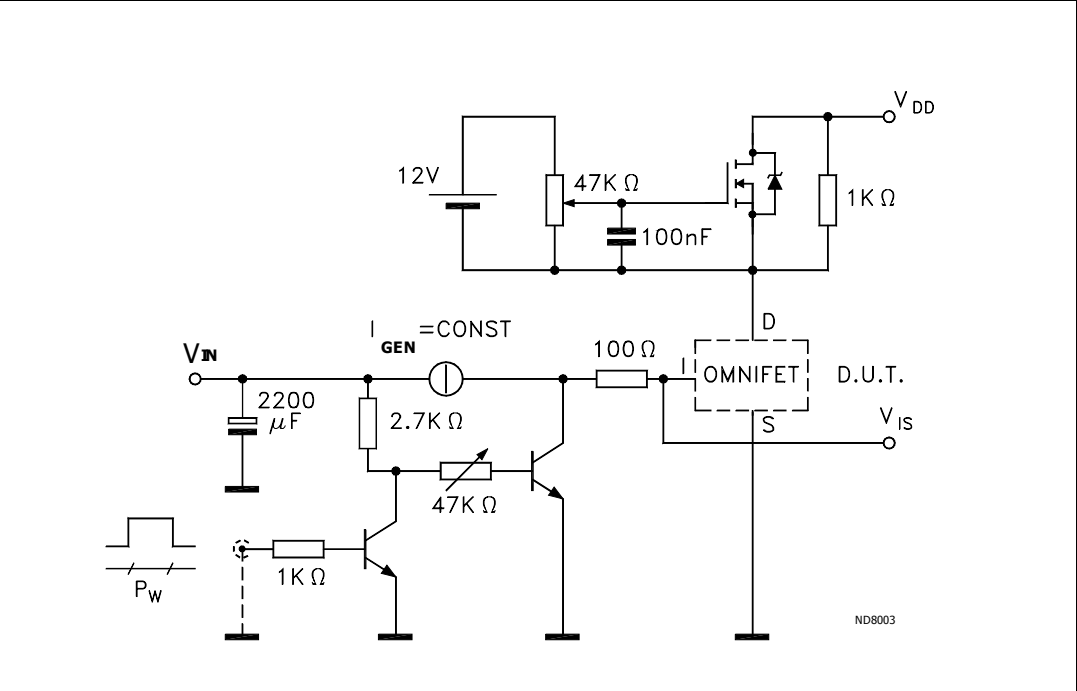
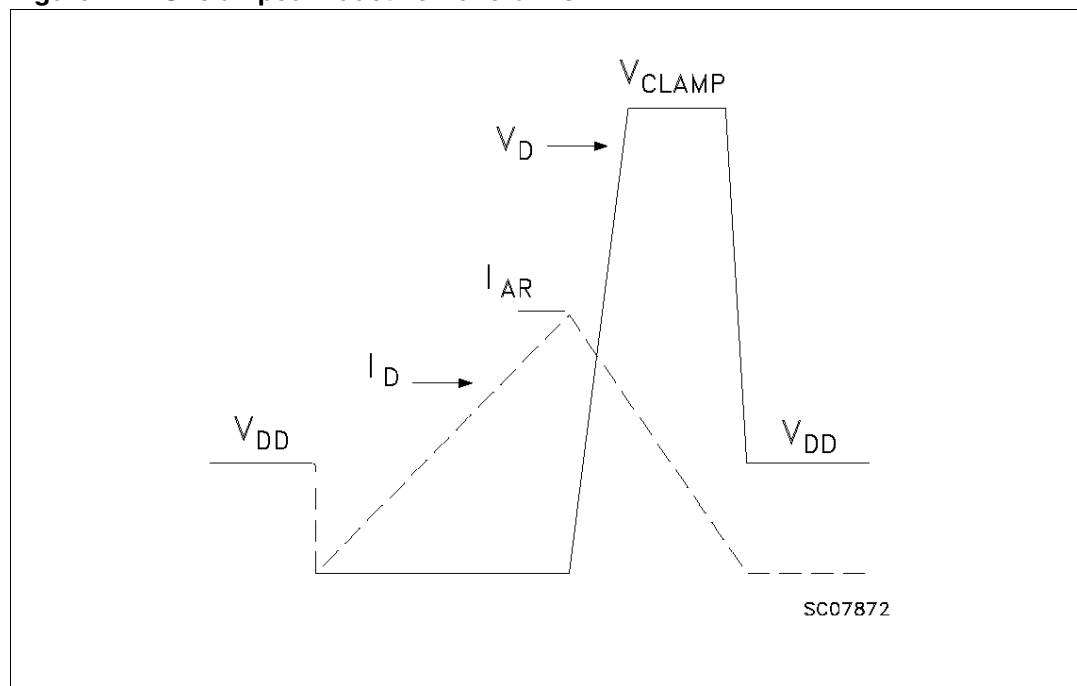


Figure 7. Unclamped inductive waveforms

2.4 Electrical characteristics curves

Figure 8. Static Drain-Source on resistance ($V_{IN} = 3.5V$)

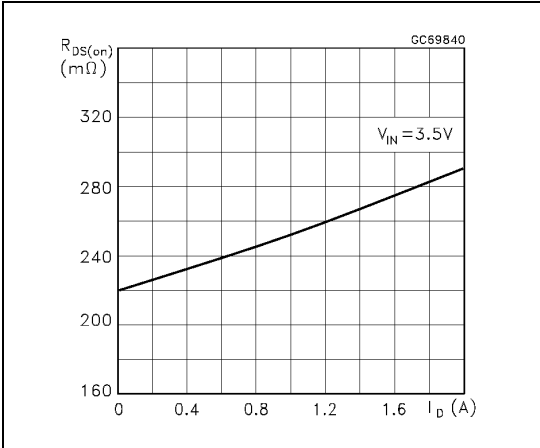


Figure 9. Static Drain-Source on resistance ($V_{IN} = 5V$)

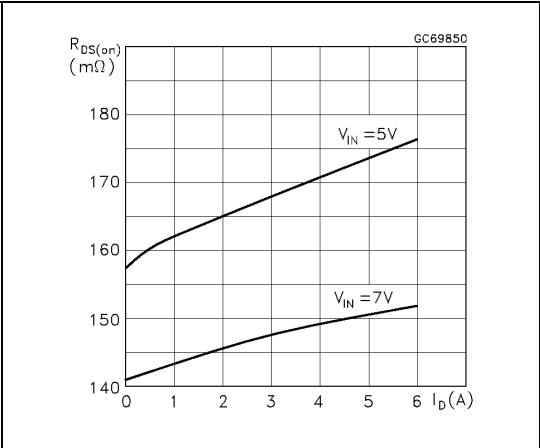


Figure 10. Derating curve

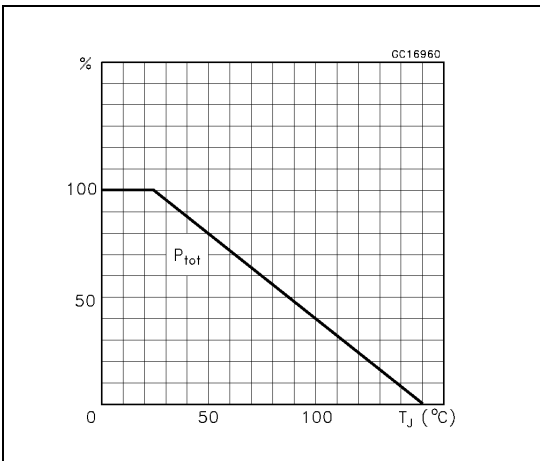


Figure 11. Static Drain-Source on resistance vs. input voltage

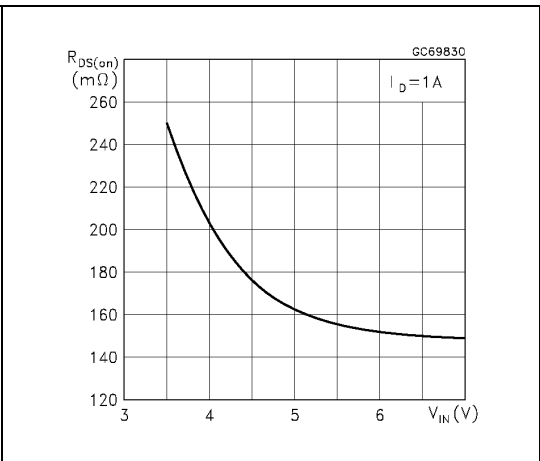


Figure 12. Current limit Vs. junction temperature

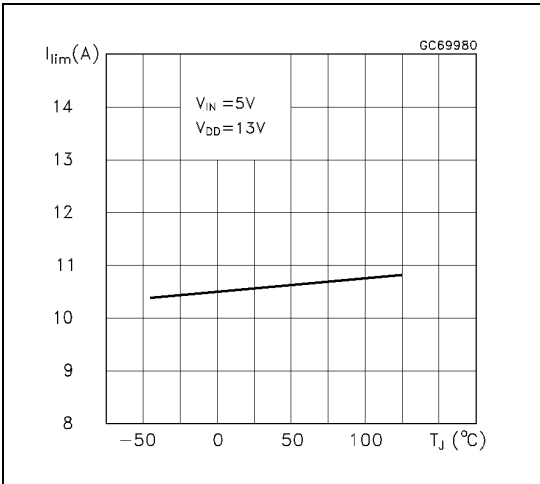


Figure 13. Source-Drain diode voltage Vs. junction temperature

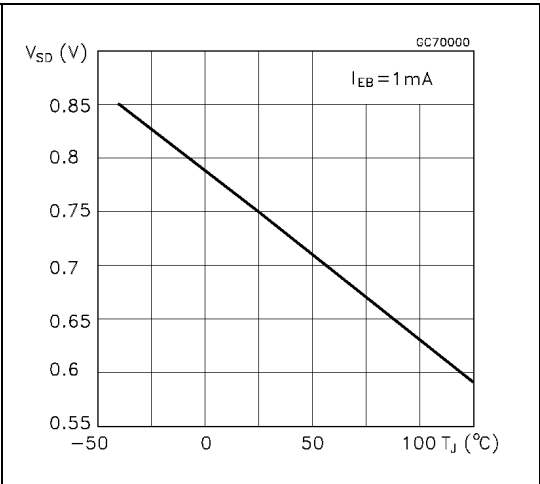


Figure 14. Step response current limit

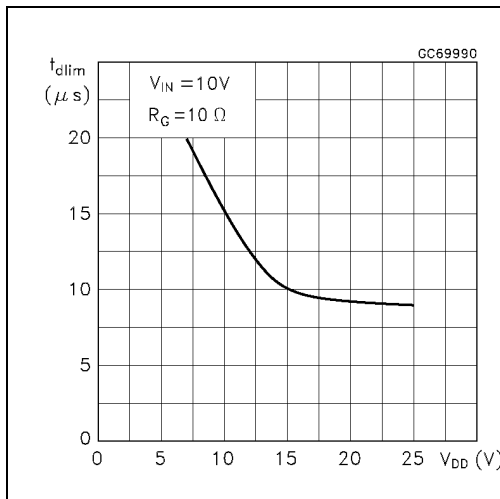


Figure 15. Switching time resistive load

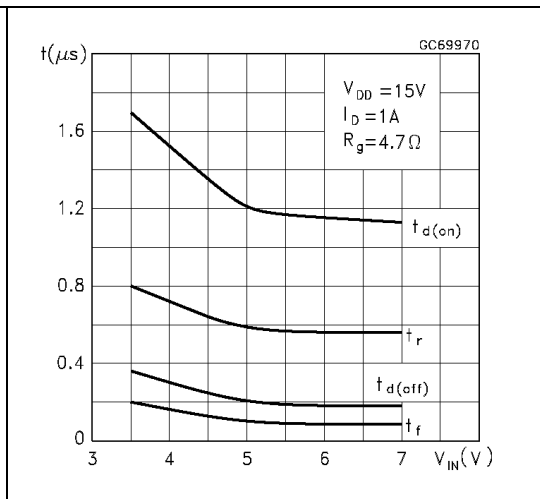
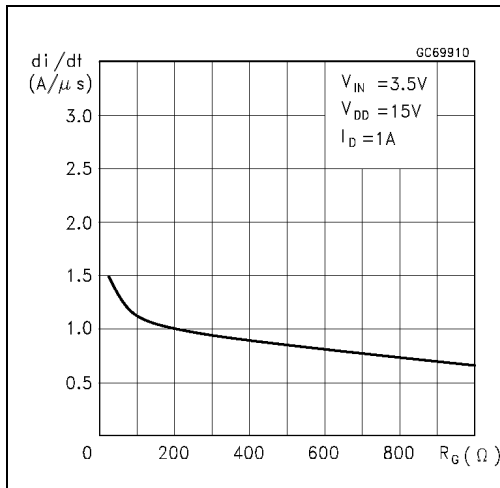
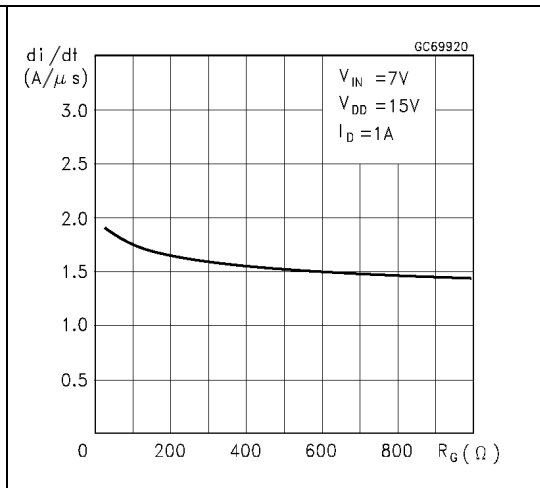
Figure 16. Turn-on current slope
($V_{IN} = 3.5V$)Figure 17. Turn-on current slope
($V_{IN} = 7V$)

Figure 18. Input voltage Vs. input charge

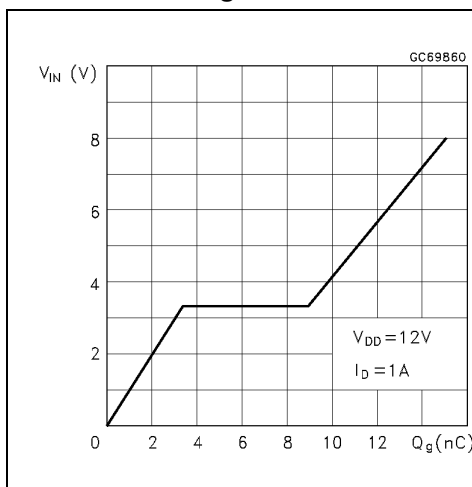


Figure 19. Turn-off Drain-Source voltage slope

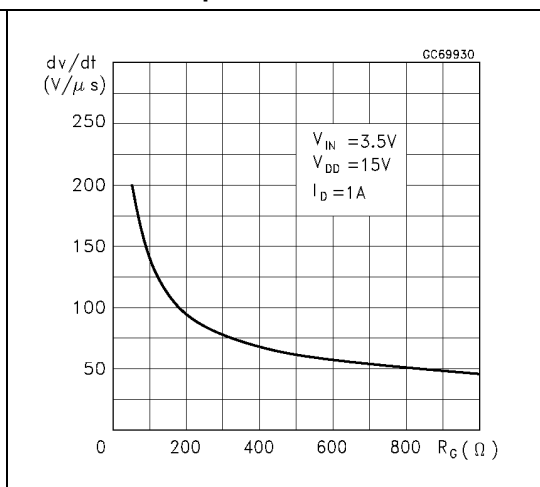


Figure 20. Turn-off Drain-Source voltage slope

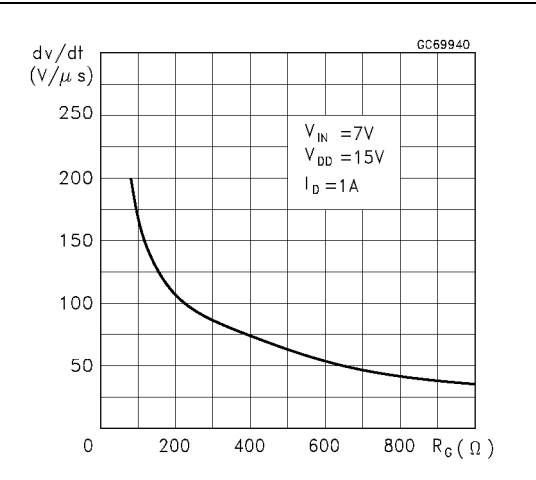


Figure 21. Capacitance variations

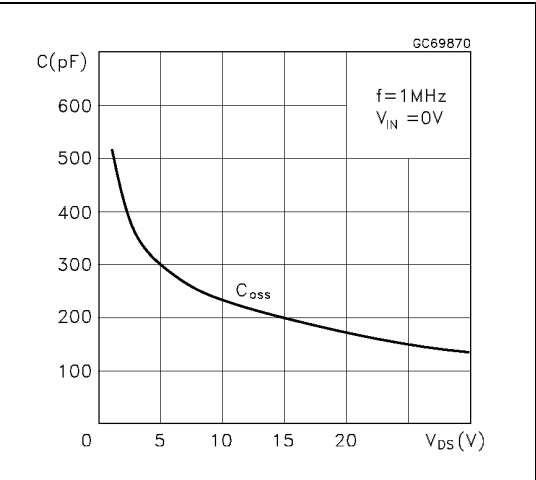


Figure 22. Switching time resistive load

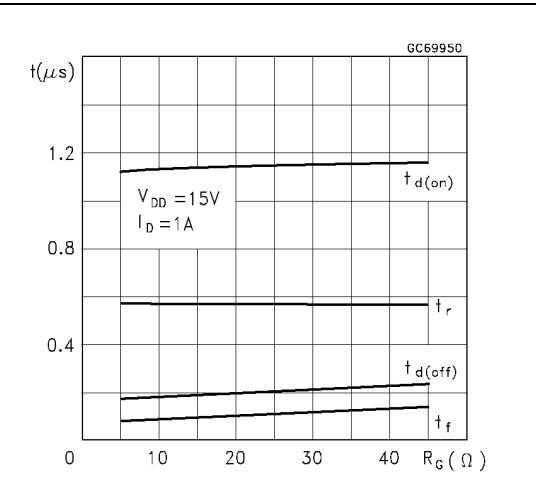


Figure 23. Normalized on resistance Vs. temperature ($V_{IN} = 7V$)

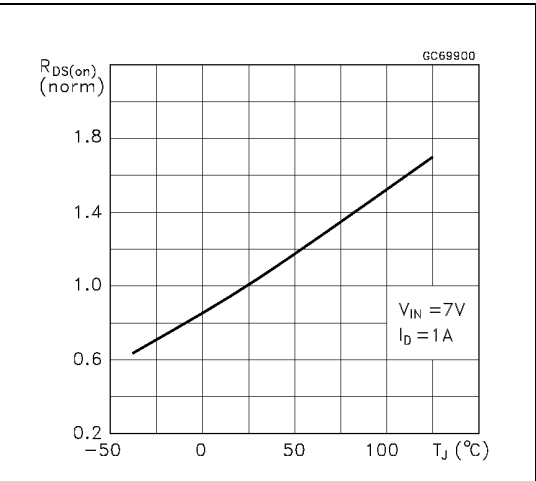


Figure 24. Output characteristics

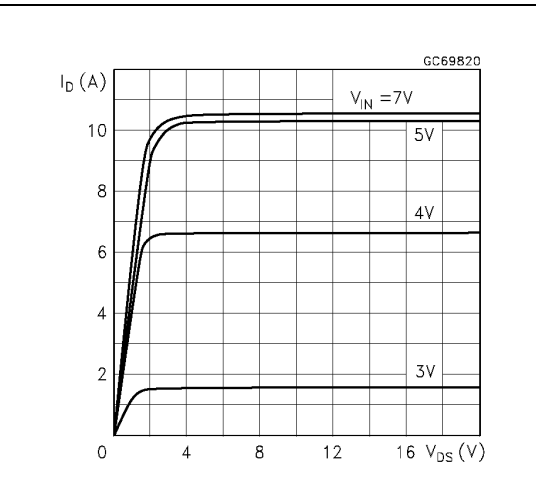


Figure 25. Normalized on resistance Vs. temperature ($V_{IN} = 3.5V$)

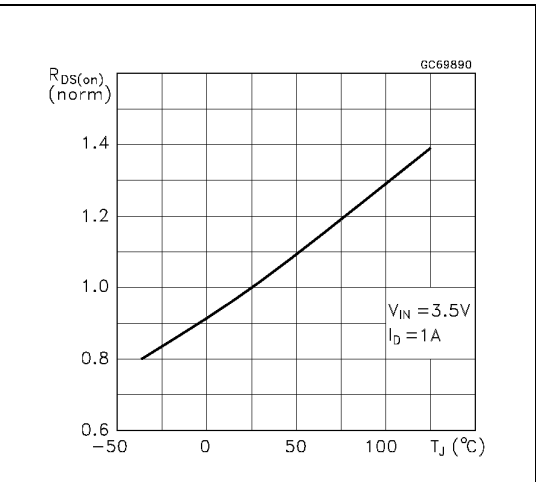
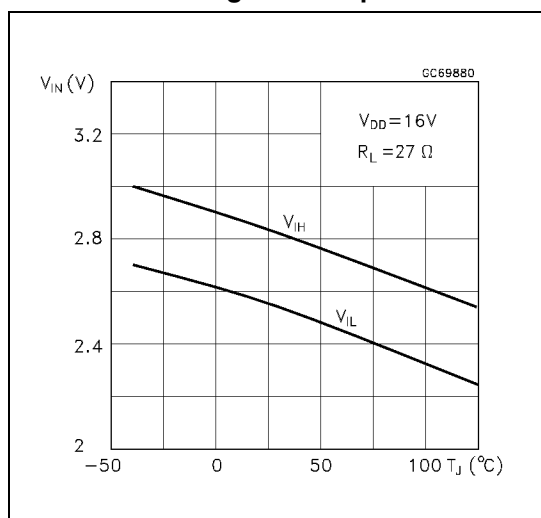


Figure 26. Normalized input threshold voltage Vs. temperature



3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path as soon as $V_{IN} > V_{IH}$.

The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} flows into the INPUT pin in order to supply the internal circuitry.

During turn-off of an unclamped inductive load the output voltage is clamped to a safe level by an integrated Zener clamp between DRAIN pin and the gate of the internal Power MOSFET.

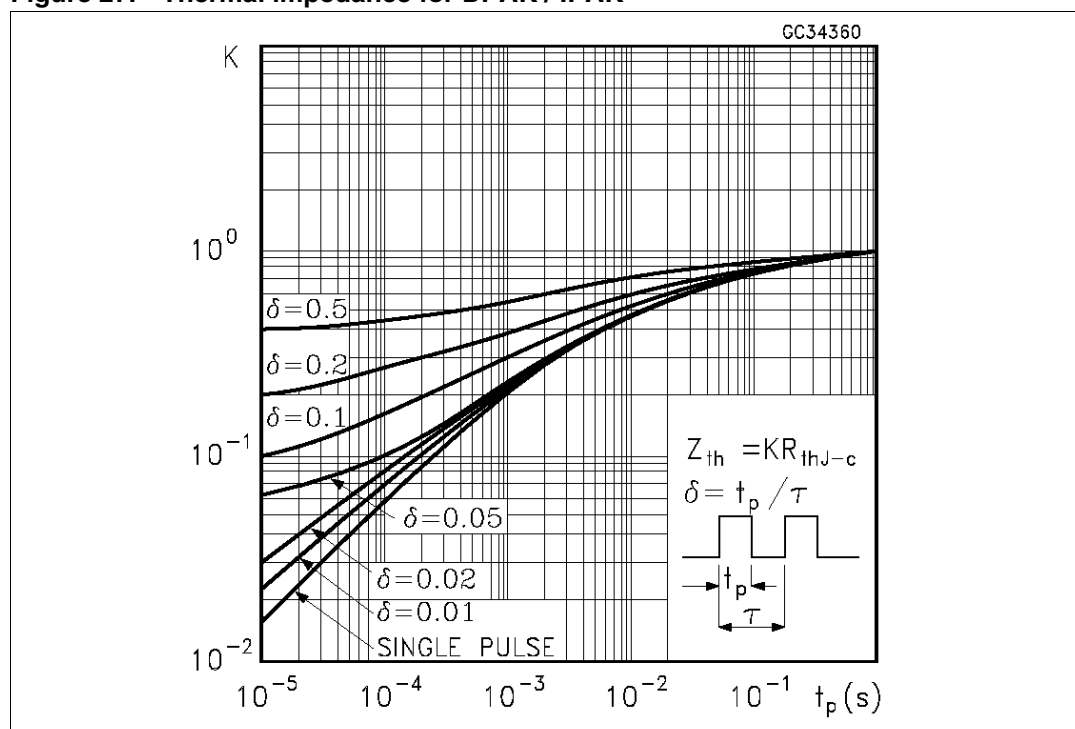
In this condition, the Power MOSFET gate is set to a voltage high enough to sustain the inductive load current even if the INPUT pin is driven to 0V. The device integrates an active current limiter circuit which limits the drain current I_D to I_{lim} whatever the INPUT pin Voltage.

When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the heatsinking capability. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

If T_j reaches T_{jsh} , the device shuts down whatever the INPUT pin voltage. The device will restart automatically when T_j has cooled down to T_{jrs} .

4 Thermal data

Figure 27. Thermal impedance for DPAK / IPAK



5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 DPAK mechanical data

Figure 28. DPAK package dimensions

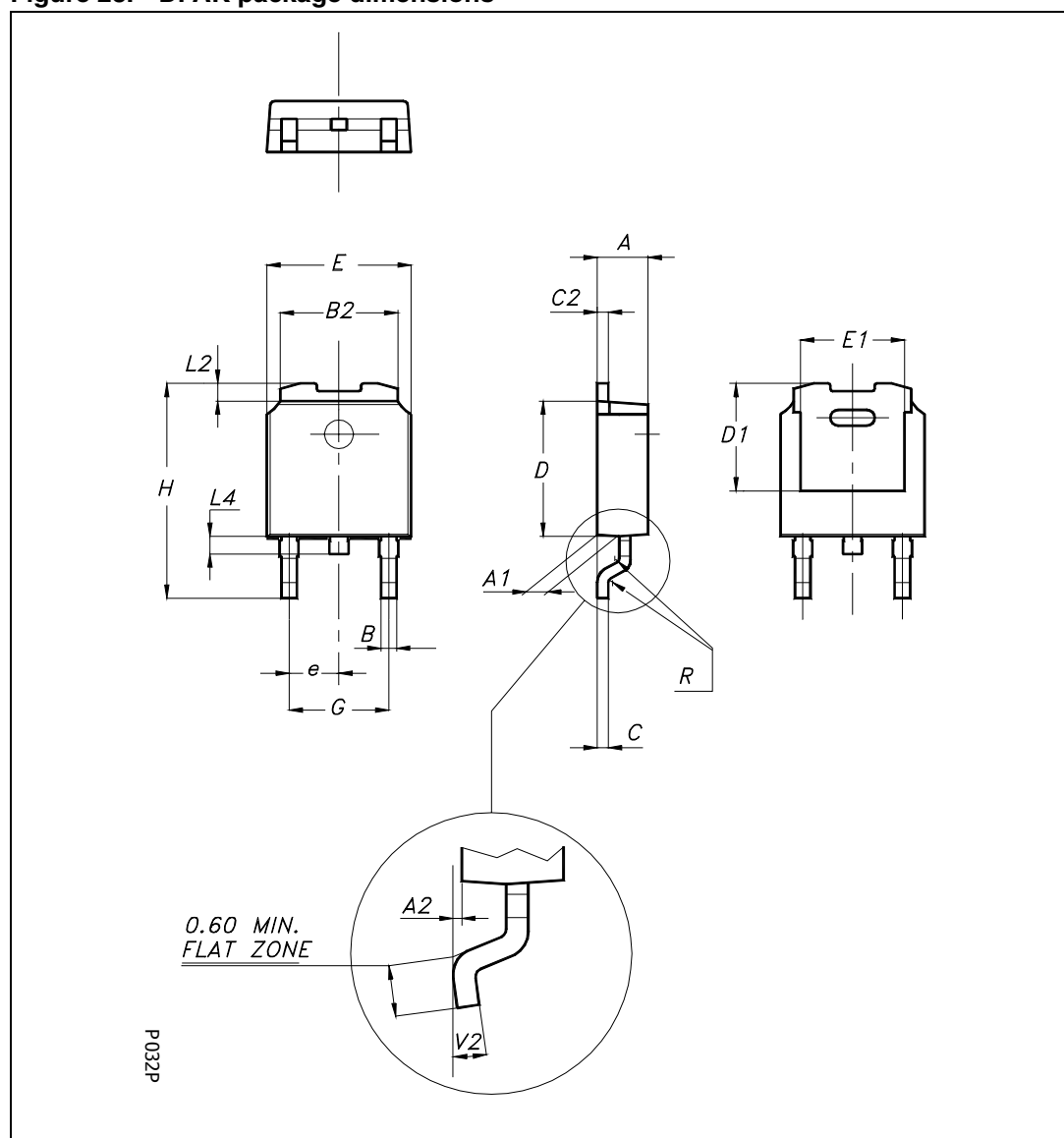


Table 10. DPAK mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package weight	Gr. 0.29		

5.3 IPAK mechanical data

Figure 29. IPAK mechanical data and package outline

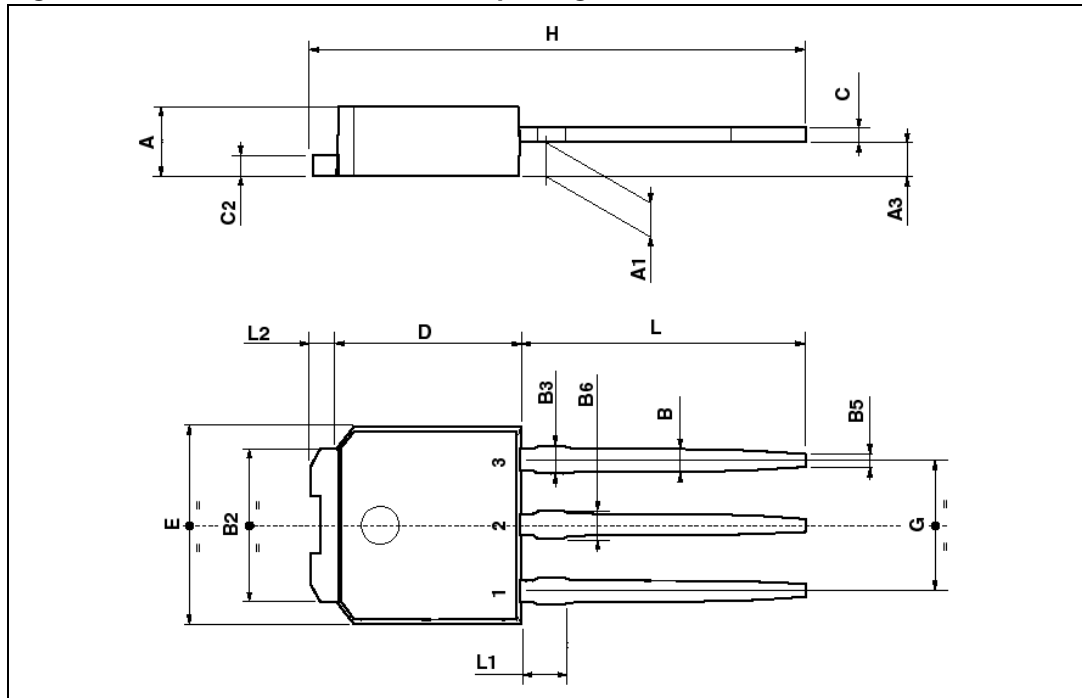


Table 11. IPAK mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

5.4 DPAK packing information

The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#)).

Figure 30. DPAK footprint

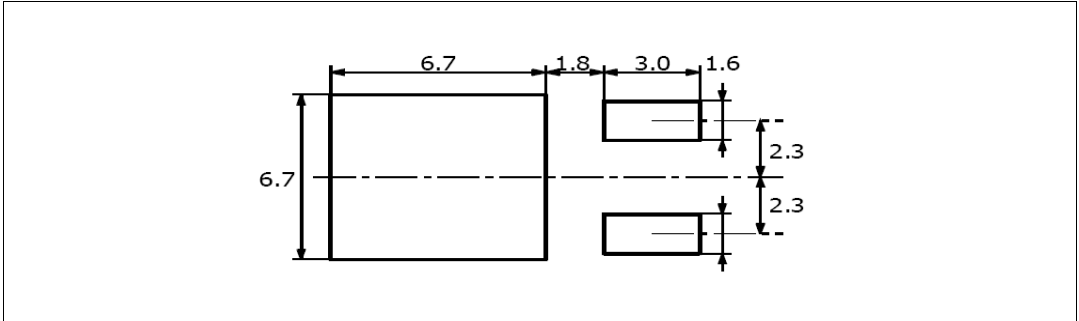
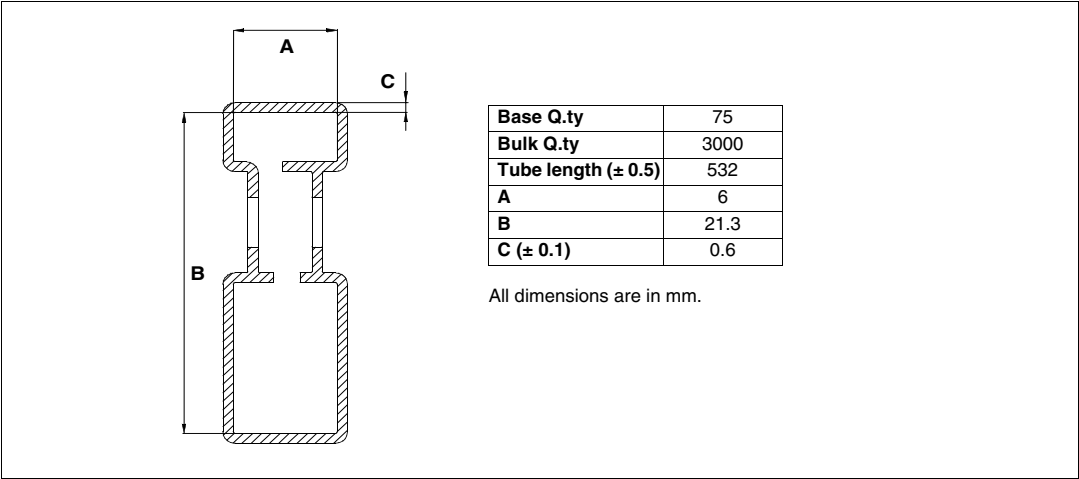


Figure 31. DPAK tube shipment (no suffix)



Reel dimensions

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

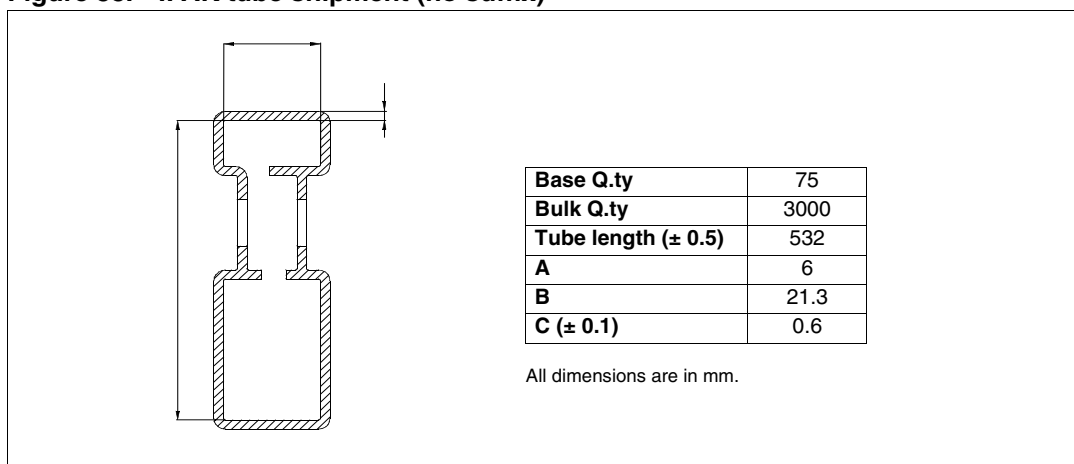
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	7.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

5.5 IPAK packing information

Figure 33. IPAK tube shipment (no suffix)



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
Oct-1997	1	Initial release.
22-Aug-2006	2	Document restructured.
12-Dec-2008	3	Document restructured and reformatted. Added <i>ECOPACK[®] packages</i> information.
25-Sep-2013	4	Updated disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

