

## SNx4HC175 Quadruple D-Type Flip-Flops With Clear

### 1 Features

- Wide operating voltage range of 2 V to 6 V
- Outputs can drive up to 10 LSTTL Loads
- Low power consumption, 80- $\mu$ A max  $I_{CC}$
- Contain four flip-flops with double-rail outputs
- Typical  $t_{pd} = 13$  ns
- $\pm 4$ -mA output drive at 5 V
- Low input current of 1  $\mu$ A max

### 2 Applications

- Buffer/storage registers
- Shift registers
- Pattern generators

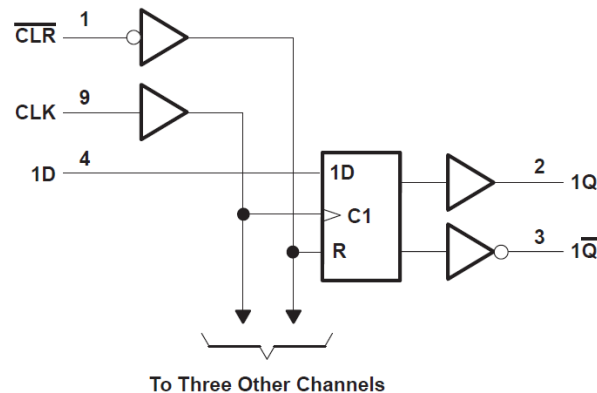
### 3 Description

These positive-edge-triggered D-type flip-flops have a direct clear ( $\overline{CLR}$ ) input. The 'HC175 devices feature complementary outputs from each flip-flop.

#### Device Information

| PART NUMBER  | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)    |
|--------------|------------------------|--------------------|
| SN54HC175J   | CDIP (16)              | 24.38 mm × 6.92 mm |
| SN74HC175D   | SOIC (16)              | 9.90 mm × 3.90 mm  |
| SN74HC175DBR | SSOP (16)              | 6.20 mm × 5.30 mm  |
| SN74HC175N   | PDIP (16)              | 19.31 mm × 6.35 mm |
| SN74HC175NSR | SO (16)                | 6.20 mm × 5.30 mm  |
| SN74HC175PW  | TSSOP (16)             | 5.00 mm × 4.40 mm  |
| SNJ54HC175FK | LCCC (20)              | 8.89 mm × 8.45 mm  |
| SNJ54HC175W  | CFP (16)               | 10.16 mm × 6.73 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

### Functional Block Diagram



## Table of Contents

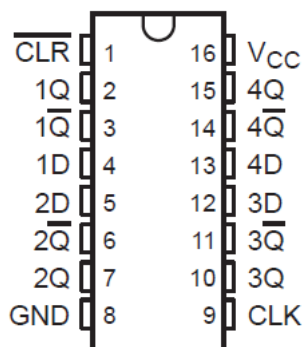
|                                                           |          |                                                        |           |
|-----------------------------------------------------------|----------|--------------------------------------------------------|-----------|
| <b>1 Features</b> .....                                   | <b>1</b> | 8.1 Overview.....                                      | <b>8</b>  |
| <b>2 Applications</b> .....                               | <b>1</b> | 8.2 Functional Block Diagram.....                      | <b>8</b>  |
| <b>3 Description</b> .....                                | <b>1</b> | 8.3 Device Functional Modes.....                       | <b>8</b>  |
| <b>4 Revision History</b> .....                           | <b>2</b> | <b>9 Power Supply Recommendations</b> .....            | <b>9</b>  |
| <b>5 Pin Configuration and Functions</b> .....            | <b>3</b> | <b>10 Layout</b> .....                                 | <b>9</b>  |
| <b>6 Specifications</b> .....                             | <b>4</b> | 10.1 Layout Guidelines.....                            | <b>9</b>  |
| 6.1 Absolute Maximum Ratings .....                        | <b>4</b> | <b>11 Device and Documentation Support</b> .....       | <b>10</b> |
| 6.2 Recommended Operating Conditions <sup>(1)</sup> ..... | <b>4</b> | 11.1 Receiving Notification of Documentation Updates.. | <b>10</b> |
| 6.3 Thermal Information.....                              | <b>4</b> | 11.2 Support Resources.....                            | <b>10</b> |
| 6.4 Electrical Characteristics.....                       | <b>5</b> | 11.3 Trademarks.....                                   | <b>10</b> |
| 6.5 Timing Requirements.....                              | <b>5</b> | 11.4 Electrostatic Discharge Caution.....              | <b>10</b> |
| 6.6 Switching Characteristics .....                       | <b>6</b> | 11.5 Glossary.....                                     | <b>10</b> |
| 6.7 Operating Characteristics.....                        | <b>6</b> | <b>12 Mechanical, Packaging, and Orderable</b>         |           |
| <b>7 Parameter Measurement Information</b> .....          | <b>7</b> | <b>Information</b> .....                               | <b>10</b> |
| <b>8 Detailed Description</b> .....                       | <b>8</b> |                                                        |           |

## 4 Revision History

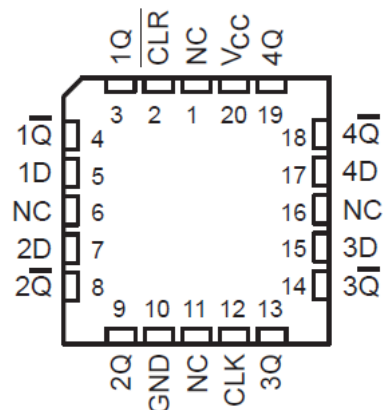
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision E (February 2022) to Revision F (June 2022)</b>                                                                                                                                                            | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <ul style="list-style-type: none"> <li>Junction-to-ambient thermal resistance values increased. D was 73 is now 117.2, DB was 67 is now 102.7, N was 82 is now 60.5, NS was 64 is now 88.6, PW was 108 is now 137.5.....</li> </ul> | <b>4</b>    |
| <b>Changes from Revision D (September 2003) to Revision E (February 2022)</b>                                                                                                                                                       | <b>Page</b> |
| <ul style="list-style-type: none"> <li>Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....</li> </ul>                                      | <b>1</b>    |

## 5 Pin Configuration and Functions



**J, W, D, DB, N, NS, or PW Package**  
**16-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP**  
**Top View**



NC - No internal connection

**FK Package**  
**20-Pin LCCC**  
**Top View**

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                            |                             | MIN  | MAX | UNIT |
|-----------|--------------------------------------------|-----------------------------|------|-----|------|
| $V_{CC}$  | Supply voltage range                       |                             | –0.5 | 7   | V    |
| $I_{IK}$  | Input clamp current <sup>(2)</sup>         | $V_I < 0$ or $V_I > V_{CC}$ |      | ±20 | mA   |
| $I_{OK}$  | Output clamp current <sup>(2)</sup>        | $V_O < 0$ or $V_O > V_{CC}$ |      | ±20 | mA   |
| $I_O$     | Continuous output current                  | $V_O = 0$ to $V_{CC}$       |      | ±25 | mA   |
|           | Continuous current through $V_{CC}$ or GND |                             |      | ±50 | mA   |
| $T_J$     | Junction temperature                       |                             |      | 150 | °C   |
| $T_{stg}$ | Storage temperature range                  |                             | –65  | 150 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 Recommended Operating Conditions<sup>(1)</sup>

|          |                                 |                  | SN54HC175 |     |          | SN74HC175 |     |          | UNIT |
|----------|---------------------------------|------------------|-----------|-----|----------|-----------|-----|----------|------|
|          |                                 |                  | MIN       | NOM | MAX      | MIN       | NOM | MAX      |      |
| $V_{CC}$ | Supply voltage                  |                  | 2         | 5   | 6        | 2         | 5   | 6        | V    |
| $V_{IH}$ | High-level input voltage        | $V_{CC} = 2$ V   | 1.5       |     |          | 1.5       |     |          | V    |
|          |                                 | $V_{CC} = 4.5$ V | 3.15      |     |          | 3.15      |     |          |      |
|          |                                 | $V_{CC} = 6$ V   | 4.2       |     |          | 4.2       |     |          |      |
| $V_{IL}$ | Low-level input voltage         | $V_{CC} = 2$ V   |           |     | 0.5      |           |     | 0.5      | V    |
|          |                                 | $V_{CC} = 4.5$ V |           |     | 1.35     |           |     | 1.35     |      |
|          |                                 | $V_{CC} = 6$ V   |           |     | 1.8      |           |     | 1.8      |      |
| $V_I$    | Input voltage                   |                  | 0         |     | $V_{CC}$ | 0         |     | $V_{CC}$ | V    |
| $V_O$    | Output voltage                  |                  | 0         |     | $V_{CC}$ | 0         |     | $V_{CC}$ | V    |
| $t_t$    | Input transition rise/fall time | $V_{CC} = 2$ V   |           |     | 1000     |           |     | 1000     | ns   |
|          |                                 | $V_{CC} = 4.5$ V |           |     | 500      |           |     | 500      |      |
|          |                                 | $V_{CC} = 6$ V   |           |     | 400      |           |     | 400      |      |
| $T_A$    | Operating free-air temperature  |                  | –55       |     | 125      | –40       |     | 85       | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.3 Thermal Information

|                      |                                                       | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|----------------------|-------------------------------------------------------|----------|-----------|----------|---------|------------|------|
| THERMAL METRIC       |                                                       | 16 PINS  | 16 PINS   | 16 PINS  | 16 PINS | 16 PINS    |      |
| $R_{\theta JA}$      | Junction-to-ambient thermal resistance <sup>(1)</sup> | 117.2    | 102.7     | 60.5     | 88.6    | 137.5      | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance             | 77.2     | 48.6      | 48       | 46.2    | 75.3       | °C/W |
| $R_{\theta JB}$      | Junction-to-board thermal resistance                  | 75.6     | 54.4      | 40.5     | 50.8    | 82.2       | °C/W |
| $\Psi_{JT}$          | Junction-to-top characterization parameter            | 38.1     | 11.6      | 27.4     | 13.4    | 25.1       | °C/W |
| $\Psi_{JB}$          | Junction-to-board characterization parameter          | 75.3     | 53.6      | 40.3     | 50.4    | 81.8       | °C/W |

### 6.3 Thermal Information (continued)

| THERMAL METRIC       |                                              | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|----------------------|----------------------------------------------|----------|-----------|----------|---------|------------|------|
|                      |                                              | 16 PINS  | 16 PINS   | 16 PINS  | 16 PINS | 16 PINS    |      |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A      | N/A       | N/A      | N/A     | N/A        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

### 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                       |                            | $V_{CC}$   | $T_A = 25^\circ\text{C}$ |           |           | SN54HC175 |            | SN74HC175 |            | UNIT          |
|-----------|---------------------------------------|----------------------------|------------|--------------------------|-----------|-----------|-----------|------------|-----------|------------|---------------|
|           |                                       |                            |            | MIN                      | TYP       | MAX       | MIN       | MAX        | MIN       | MAX        |               |
| $V_{OH}$  | $V_I = V_{IH} \text{ or } V_{IL}$     | $I_{OH} = -20 \mu\text{A}$ | 2 V        | 1.9                      | 1.998     |           | 1.9       |            | 1.9       |            | V             |
|           |                                       |                            | 4.5 V      | 4.4                      | 4.499     |           | 4.4       |            | 4.4       |            |               |
|           |                                       |                            | 6 V        | 5.9                      | 5.999     |           | 5.9       |            | 5.9       |            |               |
|           |                                       | $I_{OH} = -4 \text{ mA}$   | 4.5 V      | 3.98                     | 4.3       |           | 3.7       |            | 3.84      |            |               |
|           |                                       | $I_{OH} = -5.2 \text{ mA}$ | 6 V        | 5.48                     | 5.8       |           | 5.2       |            | 5.34      |            |               |
| $V_{OL}$  | $V_I = V_{IH} \text{ or } V_{IL}$     | $I_{OL} = 20 \mu\text{A}$  | 2 V        |                          | 0.002     | 0.1       |           | 0.1        |           | 0.1        | V             |
|           |                                       |                            | 4.5 V      |                          | 0.001     | 0.1       |           | 0.1        |           | 0.1        |               |
|           |                                       |                            | 6 V        |                          | 0.001     | 0.1       |           | 0.1        |           | 0.1        |               |
|           |                                       | $I_{OL} = 4 \text{ mA}$    | 4.5 V      |                          | 0.17      | 0.26      |           | 0.4        |           | 0.33       |               |
|           |                                       | $I_{OL} = 5.2 \text{ mA}$  | 6 V        |                          | 0.15      | 0.26      |           | 0.4        |           | 0.33       |               |
| $I_I$     | $V_I = V_{CC} \text{ or } 0$          |                            | 6 V        |                          | $\pm 0.1$ | $\pm 100$ |           | $\pm 1000$ |           | $\pm 1000$ | nA            |
| $I_{CC}$  | $V_I = V_{CC} \text{ or } 0, I_O = 0$ |                            | 6 V        |                          |           | 8         |           | 160        |           | 80         | $\mu\text{A}$ |
| $C_i$     |                                       |                            | 2 V to 6 V |                          | 3         | 10        |           | 10         |           | 10         | pF            |

### 6.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

|                    |                                  |                 | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     | SN54HC175 |     | SN74HC175 |     | UNIT |
|--------------------|----------------------------------|-----------------|----------|--------------------------|-----|-----------|-----|-----------|-----|------|
|                    |                                  |                 |          | MIN                      | MAX | MIN       | MAX | MIN       | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                  |                 | 2 V      |                          | 6   |           | 4.2 |           | 5   | MHz  |
|                    |                                  |                 | 4.5 V    |                          | 31  |           | 21  |           | 25  |      |
|                    |                                  |                 | 6 V      |                          | 36  |           | 25  |           | 29  |      |
| $t_w$              | Pulse duration                   | CLR low         | 2 V      | 80                       |     | 120       |     | 100       |     | ns   |
|                    |                                  |                 | 4.5 V    | 16                       |     | 24        |     | 20        |     |      |
|                    |                                  |                 | 6 V      | 14                       |     | 20        |     | 17        |     |      |
|                    |                                  | CLK high or low | 2 V      | 80                       |     | 120       |     | 100       |     |      |
|                    |                                  |                 | 4.5 V    | 16                       |     | 24        |     | 20        |     |      |
|                    |                                  |                 | 6 V      | 14                       |     | 20        |     | 17        |     |      |
| $t_{su}$           | Setup time before CLK $\uparrow$ | Data            | 2 V      | 100                      |     | 150       |     | 125       |     | ns   |
|                    |                                  |                 | 4.5 V    | 20                       |     | 30        |     | 25        |     |      |
|                    |                                  |                 | 6 V      | 17                       |     | 25        |     | 21        |     |      |
|                    |                                  | CLR inactive    | 2 V      | 100                      |     | 150       |     | 125       |     |      |
|                    |                                  |                 | 4.5 V    | 20                       |     | 30        |     | 25        |     |      |
|                    |                                  |                 | 6 V      | 17                       |     | 25        |     | 21        |     |      |

## 6.5 Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted)

|       |                                      | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     | SN54HC175 |     | SN74HC175 |     | UNIT |
|-------|--------------------------------------|----------|--------------------------|-----|-----------|-----|-----------|-----|------|
|       |                                      |          | MIN                      | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_h$ | Hold time, data after CLK $\uparrow$ | 2 V      | 0                        |     | 0         |     | 0         |     | ns   |
|       |                                      | 4.5 V    | 0                        |     | 0         |     | 0         |     |      |
|       |                                      | 6 V      | 0                        |     | 0         |     | 0         |     |      |

## 6.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Parameter Measurement Information](#))

| PARAMETER | FROM (INPUT)     | TO (OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC175 |     | SN74HC175 |     | UNIT |
|-----------|------------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                  |             |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $f_{max}$ |                  |             | 2 V      | 6                        | 12  |     | 4.2       |     | 5         |     | MHz  |
|           |                  |             | 4.5 V    | 31                       | 50  |     | 21        |     | 25        |     |      |
|           |                  |             | 6 V      | 36                       | 60  |     | 25        |     | 29        |     |      |
| $t_{pd}$  | $\overline{CLR}$ | Any         | 2 V      |                          | 52  | 150 |           | 255 |           | 190 | ns   |
|           |                  |             | 4.5 V    |                          | 15  | 30  |           | 45  |           | 38  |      |
|           |                  |             | 6 V      |                          | 13  | 26  |           | 38  |           | 32  |      |
|           | CLK              | Any         | 2 V      |                          | 58  | 150 |           | 255 |           | 190 |      |
|           |                  |             | 4.5 V    |                          | 16  | 30  |           | 45  |           | 38  |      |
|           |                  |             | 6 V      |                          | 13  | 26  |           | 38  |           | 32  |      |
| $t_t$     |                  | Any         | 2 V      |                          | 38  | 75  |           | 110 |           | 90  | ns   |
|           |                  |             | 4.5 V    |                          | 8   | 15  |           | 22  |           | 19  |      |
|           |                  |             | 6 V      |                          | 6   | 13  |           | 19  |           | 16  |      |

## 6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

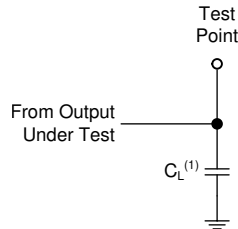
| PARAMETER |                                             | TEST CONDITIONS | TYP | UNIT |
|-----------|---------------------------------------------|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per flip-flop | No load         | 30  | pF   |

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

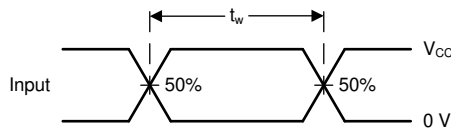
For clock inputs,  $f_{\max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

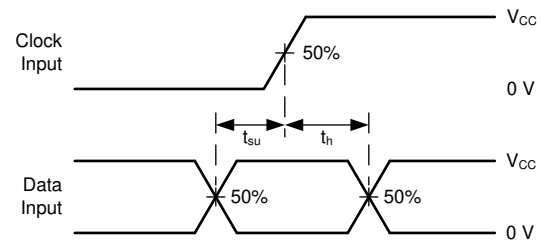


(1)  $C_L$  includes probe and test-fixture capacitance.

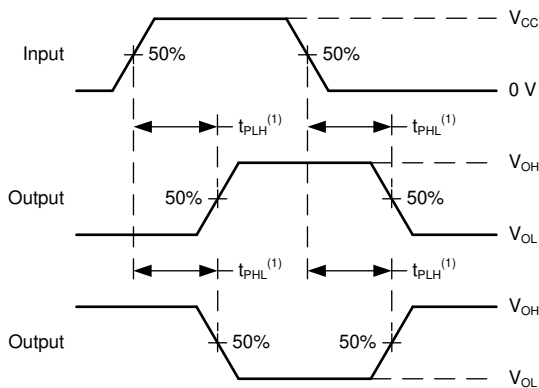
**Figure 7-1. Load Circuit for Push-Pull Outputs**



**Figure 7-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration**

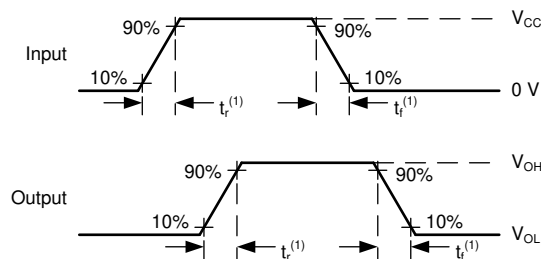


**Figure 7-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 7-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 7-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**

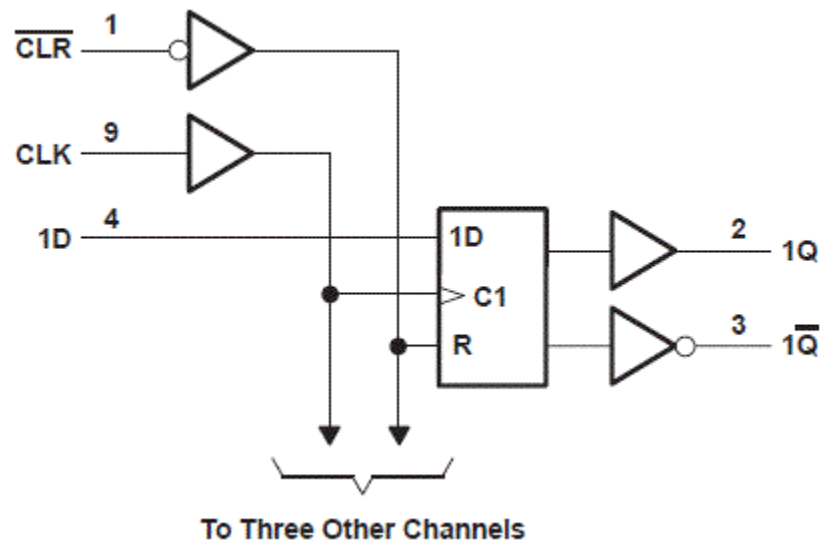
## 8 Detailed Description

### 8.1 Overview

These positive-edge-triggered D-type flip-flops have a direct clear ( $\overline{\text{CLR}}$ ) input. The 'HC175 devices feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

### 8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

### 8.3 Device Functional Modes

**Table 8-1. Function Table  
(each flip-flop)**

| INPUTS |            |   | OUTPUTS      |                         |
|--------|------------|---|--------------|-------------------------|
| CLR    | CLK        | D | Q            | $\overline{\text{Q}}$   |
| L      | X          | X | L            | H                       |
| H      | $\uparrow$ | H | H            | L                       |
| H      | $\uparrow$ | L | L            | H                       |
| H      | L          | X | $\text{Q}_0$ | $\overline{\text{Q}}_0$ |

## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 10 Layout

### 10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">84089012A</a>        | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84089012A<br>SNJ54HC<br>175FK |
| <a href="#">8408901EA</a>        | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8408901EA<br>SNJ54HC175J      |
| <a href="#">8408901FA</a>        | Active        | Production           | CFP (W)   16    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8408901FA<br>SNJ54HC175W      |
| <a href="#">JM38510/65308BEA</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>65308BEA          |
| JM38510/65308BEA.A               | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>65308BEA          |
| <a href="#">M38510/65308BEA</a>  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>65308BEA          |
| <a href="#">SN54HC175J</a>       | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC175J                    |
| SN54HC175J.A                     | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC175J                    |
| <a href="#">SN74HC175D</a>       | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC175                         |
| <a href="#">SN74HC175DBR</a>     | Active        | Production           | SSOP (DB)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175DBR.A                   | Active        | Production           | SSOP (DB)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| <a href="#">SN74HC175DR</a>      | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175DR.A                    | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175DRG4                    | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175DRG4.A                  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| <a href="#">SN74HC175N</a>       | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC175N                    |
| SN74HC175N.A                     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC175N                    |
| SN74HC175NE4                     | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC175N                    |
| <a href="#">SN74HC175NSR</a>     | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175NSR.A                   | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| <a href="#">SN74HC175PW</a>      | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC175                         |
| <a href="#">SN74HC175PWR</a>     | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175PWR.A                   | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |
| SN74HC175PWR.B                   | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | -           | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC175                         |

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">SNJ54HC175FK</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84089012A<br>SNJ54HC<br>175FK |
| SNJ54HC175FK.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84089012A<br>SNJ54HC<br>175FK |
| <a href="#">SNJ54HC175J</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8408901EA<br>SNJ54HC175J      |
| SNJ54HC175J.A                | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8408901EA<br>SNJ54HC175J      |
| <a href="#">SNJ54HC175W</a>  | Active        | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8408901FA<br>SNJ54HC175W      |
| SNJ54HC175W.A                | Active        | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8408901FA<br>SNJ54HC175W      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC175, SN74HC175 :**

- Catalog : [SN74HC175](#)
- Military : [SN54HC175](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC175DBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74HC175DR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC175DRG4 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC175NSR  | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74HC175PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

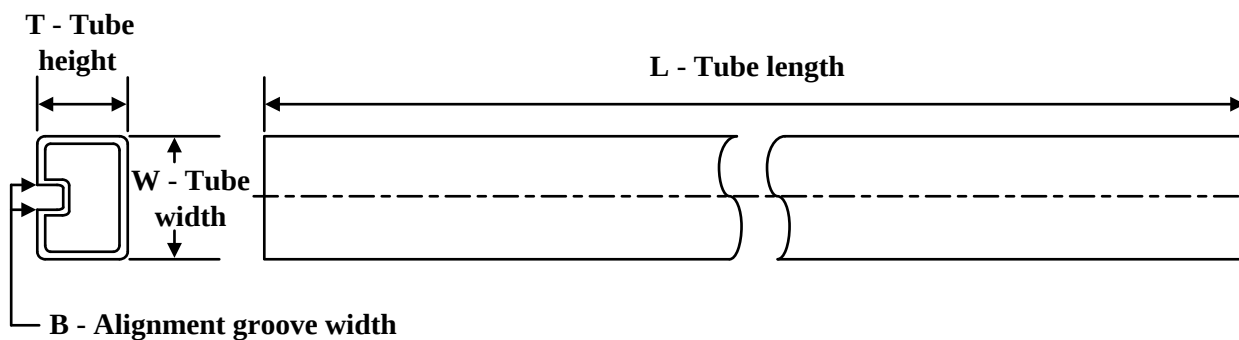
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC175DBR  | SSOP         | DB              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74HC175DR   | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74HC175DRG4 | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74HC175NSR  | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74HC175PWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 84089012A      | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 8408901FA      | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74HC175N     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC175N     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC175N.A   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC175N.A   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC175NE4   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC175NE4   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54HC175FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54HC175FK.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54HC175W    | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SNJ54HC175W.A  | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

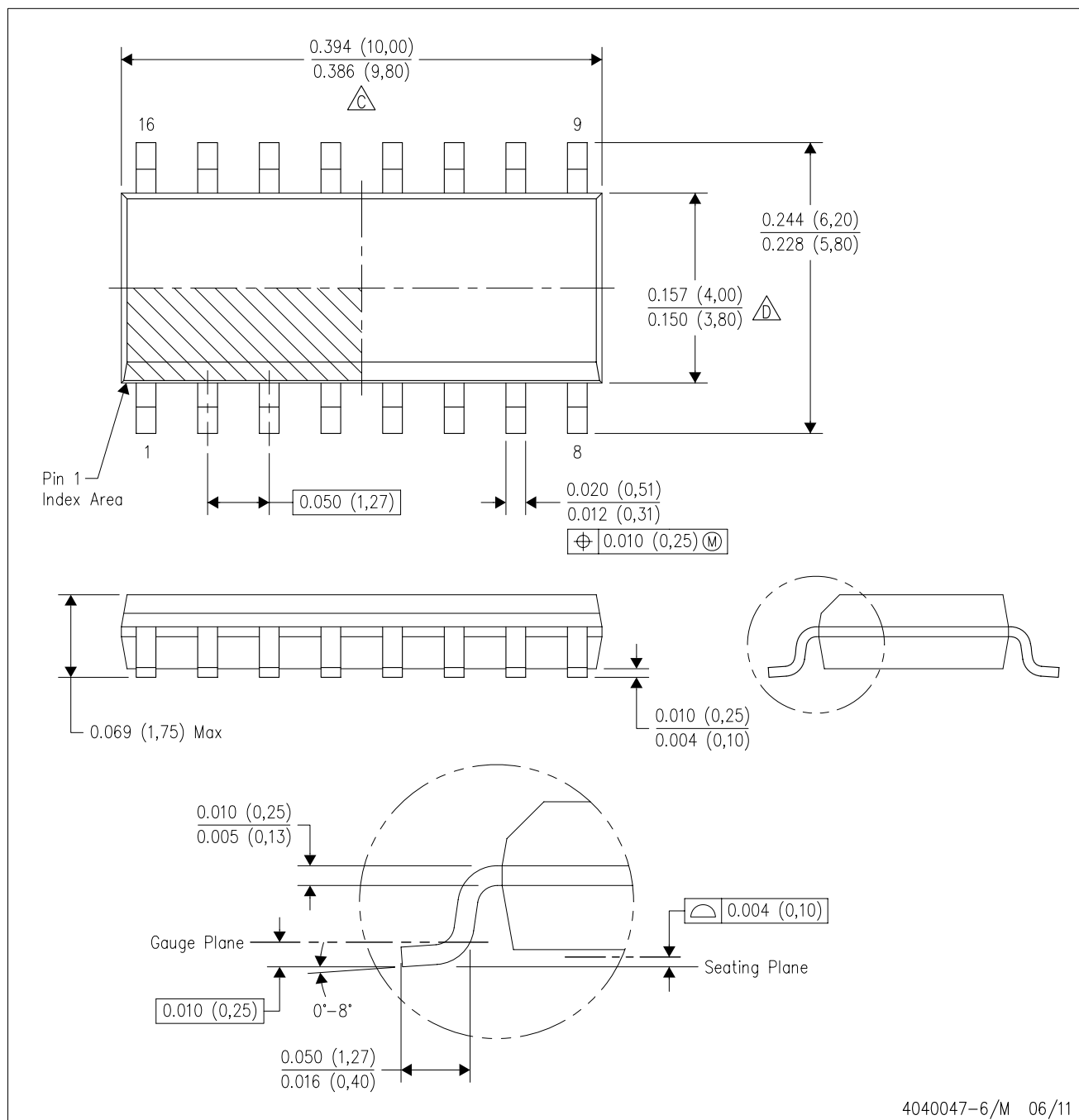
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

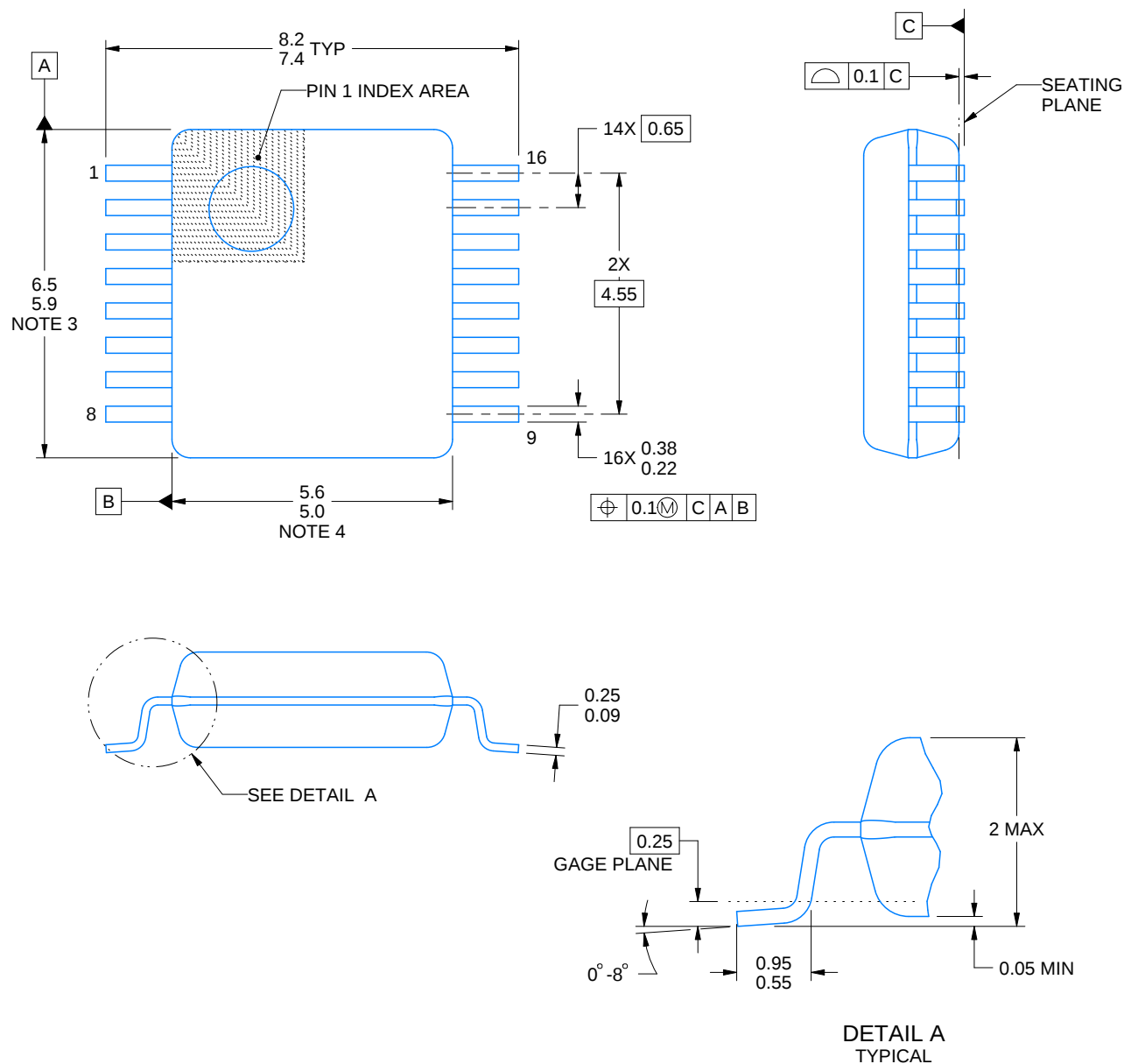
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220763/A 05/2022

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

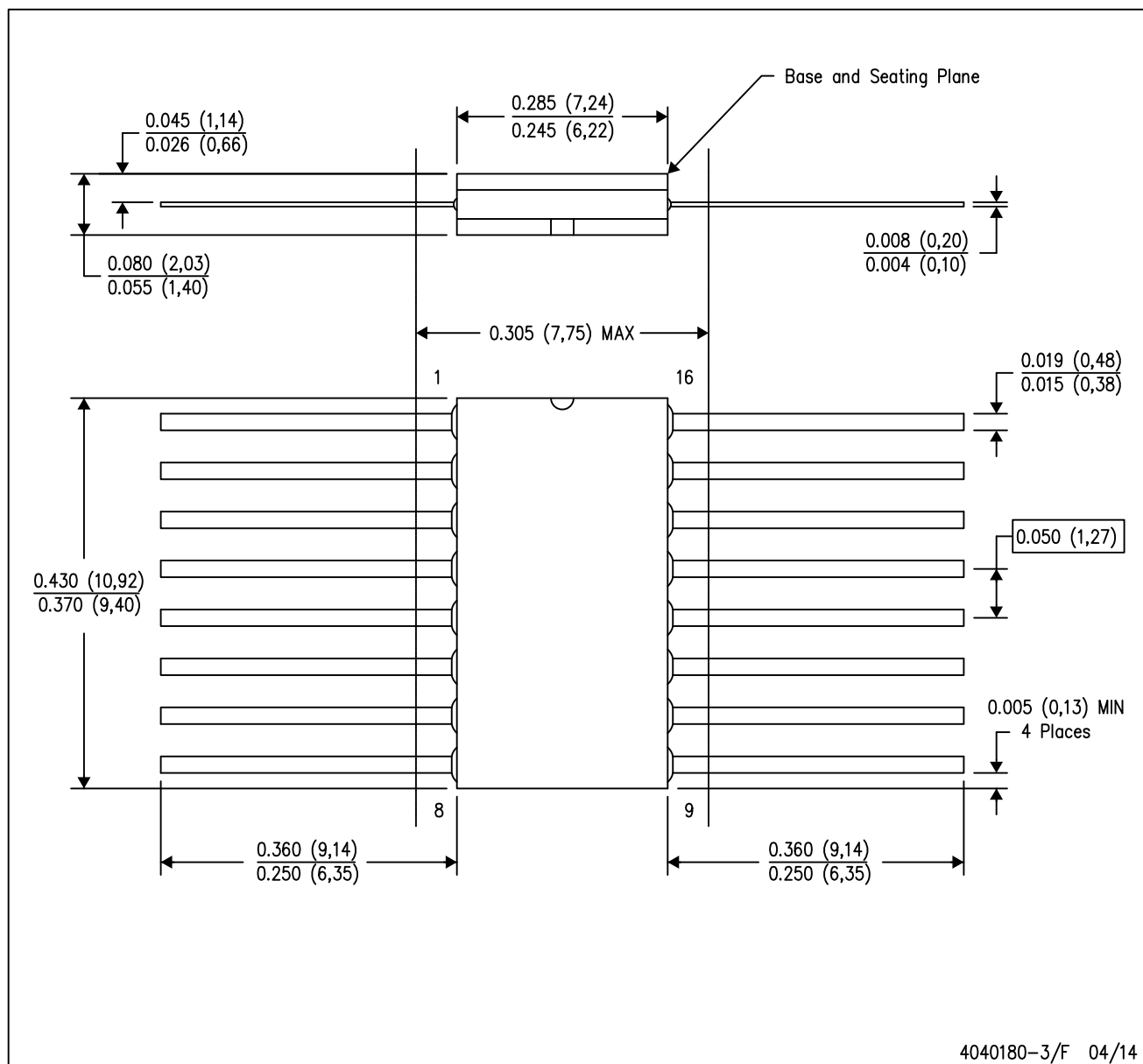
14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE

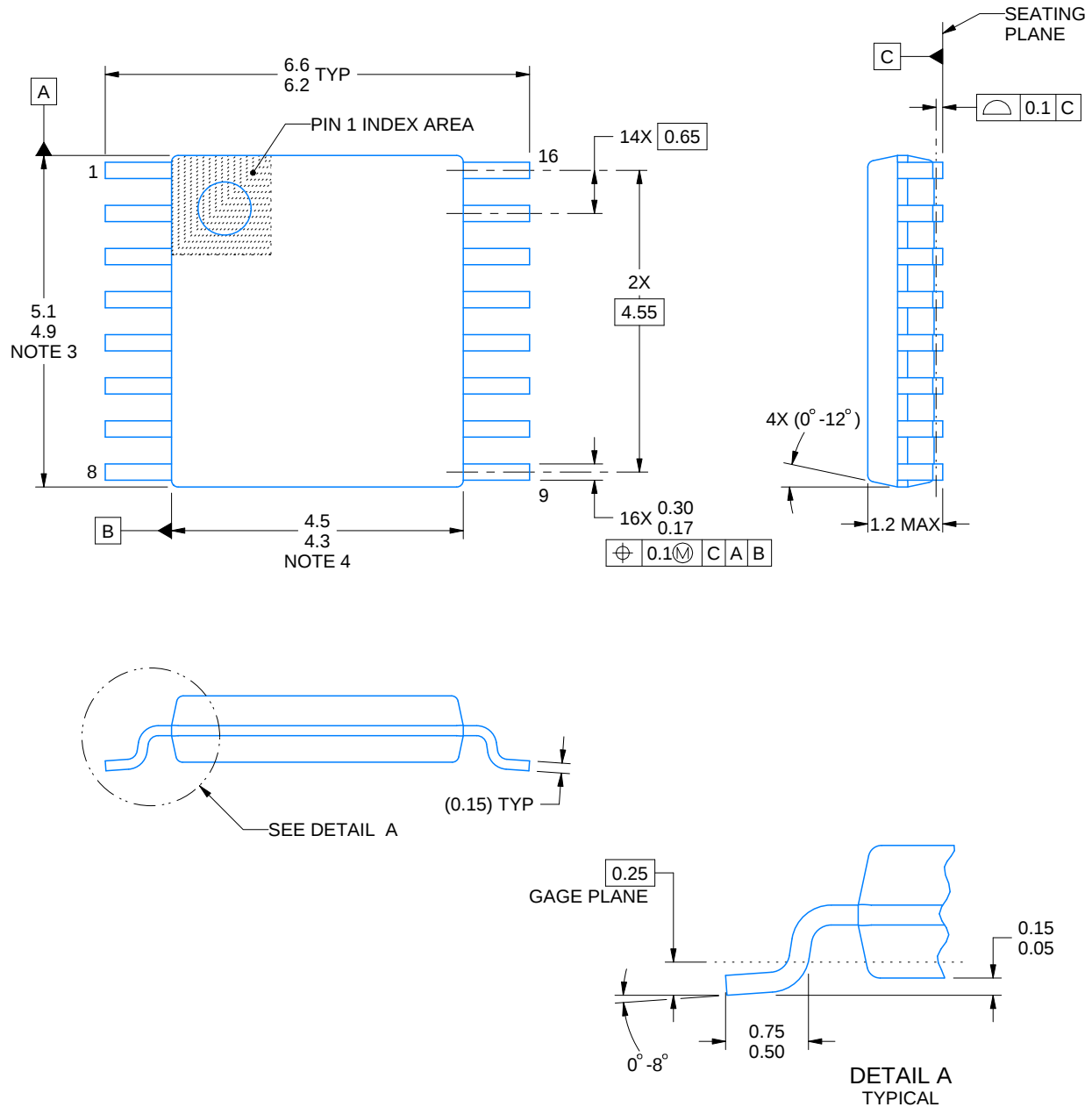


| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

## NOTES:

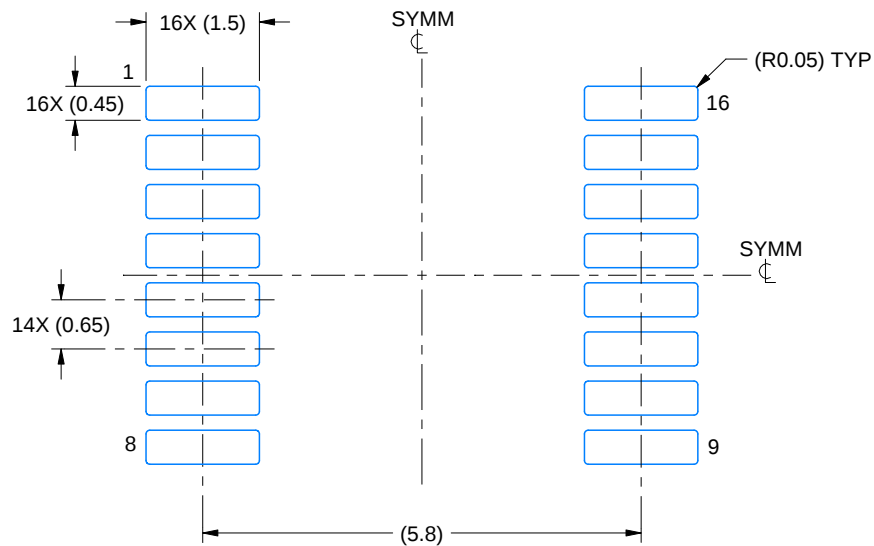
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

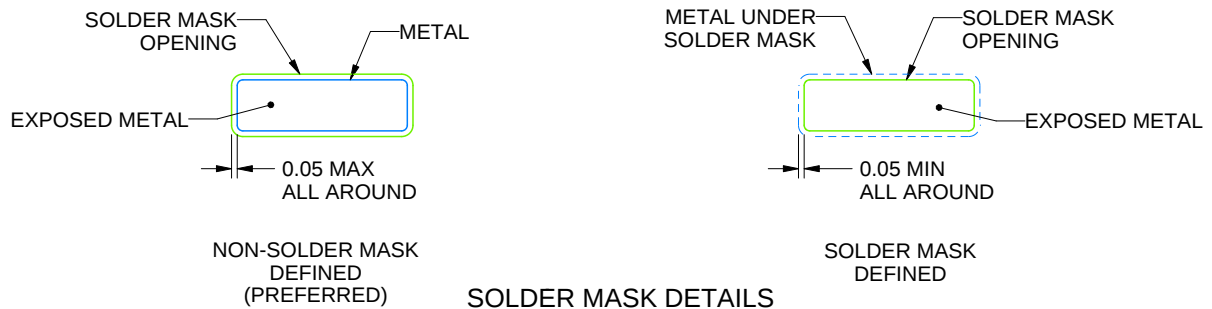
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated