FAIRCHILD SEMICONDUCTOR™

March 1999

NM93CS46 (MICROWIRE™ Bus Interface) 1K-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

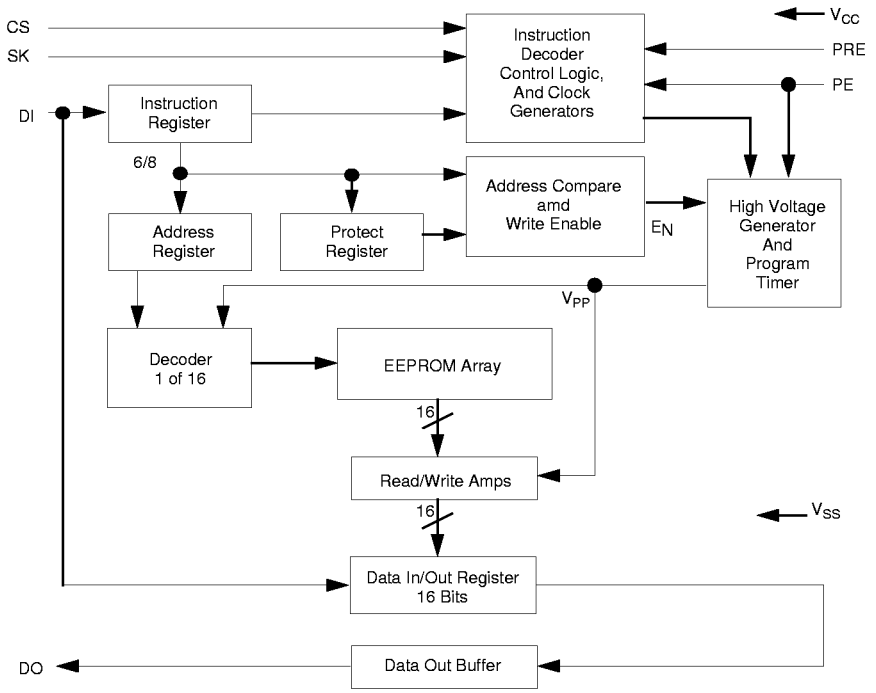
The NM93CS46 devices are 1024 bits of CMOS non-volatile electrically erasable memory divided into 64 16-bit registers. Selected registers can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification (all registers greater than, or equal to, the selected address are then protected from further change). Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using Fairchild Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CS46 is offered in both SO and TSSOP packages for small space considerations.

The EEPROM interfacing is MICROWIRE compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRENABLE, PRCLEAR, and PRDISABLE.

Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 200µA
  10µA standby current typical
  1µA standby current typical (L)
  0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 1,000,000 data changes
- 2.7V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Functional Diagram



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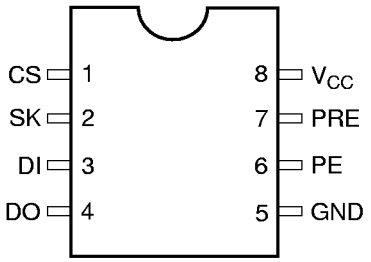
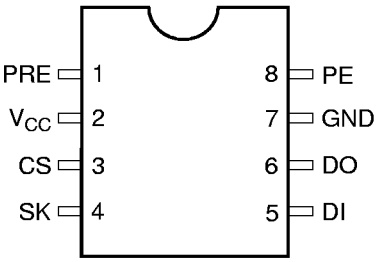
Connection Diagram

Dual-In-Line Package (N)
8–Pin SO (M8) and 8–Pin TSSOP (MT8)



DS500084-2

Rotated Die (93CS46T)



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Top View
Package Number N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

NM	93	CS	XX	T	LZ	E	XX	Letter	Description
							Package	N	8-pin DIP
								M8	8-pin SO
								MT8	8-pin TSSOP
						Temp. Range		None	0 to 70°C
								V	-40 to +125°C
								E	-40 to +85°C
					Voltage Operating Range			Blank	4.5V to 5.5V
								L	2.7V to 4.5V
								LZ	2.7V to 4.5V and <1µA Standby Current
				Blank				Blank	Normal Pin Out
				T				T	Rotated Pin Out
			Density					46	1024 bits
		C						C	CMOS
		CS						CS	Data protect and sequential read
	Interface							93	MICROWIRE
NM								**NM**	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS46	0°C to +70°C
NM93CS46E	-40°C to +85°C
NM93CS46V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±-1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = -400 µA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} - 0.2	0.2	V
f_{SK}	SK Clock Frequency		(Note 3)		1	MHz
t_{SKH}	SK High Time	NM93CS46 NM93CS46E/V	0°C to +70°C -40°C to +125°C	250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 4)	250		ns
t_{CSS}	CS Setup Time			100		ns
t_{PRES}	PRE Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{PES}	PE Setup Time			50		ns
t_{DIS}	DI Setup Time			100		ns
t_{CSH}	CS Hold Time			0		ns
t_{PEH}	PE Hold Time			250		ns
t_{PREH}	PRE Hold Time			50		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to “1”				500	ns
t_{PD0}	Output Delay to “0”				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE™		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CS46L/LZ	0°C to +70°C
NM93CS46LE/LZE	-40°C to +85°C
NM93CS46LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 4.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 4.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK=250 KHz		1	mA
I_{CCS}	Standby Current L LZ		CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			-0.1 0.8V_{CC}	0.15V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10µA I_{OH} = -10µA	 0.9V_{CC}	0.1V_{CC}	V
f_{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t_{SKH}	SK High Time			1		µs
t_{SKL}	SK Low Time			1		µs
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	0.2		µs
t_{CS}	Minimum CS Low Time		(Note 4)	1		µs
t_{CSS}	CS Setup Time			0.2		µs
t_{PRES}	PRE Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{PES}	PE Setup Time			50		ns
t_{DIS}	DI Setup Time			0.4		µs
t_{CSH}	CS Hold Time			0		ns
t_{PEH}	PE Hold Time			250		ns
t_{PREH}	PRE Hold Time			50		ns
t_{DIH}	DI Hold Time			0.4		µs
t_{PD1}	Output Delay to "1"				2	µs
t_{PD0}	Output Delay to "0"				2	µs
t_{SV}	CS to Status Valid				1	µs
t_{DF}	CS to DO in TRI-STATE™		CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH minimum} + t_{SKL minimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93CS46 EEPROM has 10 instructions as described below. All Data-In signals are clocked into the device on the low-to-high SK transition.

Read and Sequential Register Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **sequential register read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. This function is DISABLED if the Protect Register is in use to lock out a section of memory.

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: For all Protect Register Operations: If the PRE pin is not held at V_{IH}, all instructions will be applied to the EEPROM array, rather than the Protect Register.

Protect Register Read (PRREAD):

The PRREAD instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction the address stored in the memory Protect Register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the address string.

Protect Register Enable (PREN):

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The PRCLEAR instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRCLEAR instruction. Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will PREVENT the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming opcode.

Protect Register Write (PRWRITE):

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The PRDS instruction is a **ONE** TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

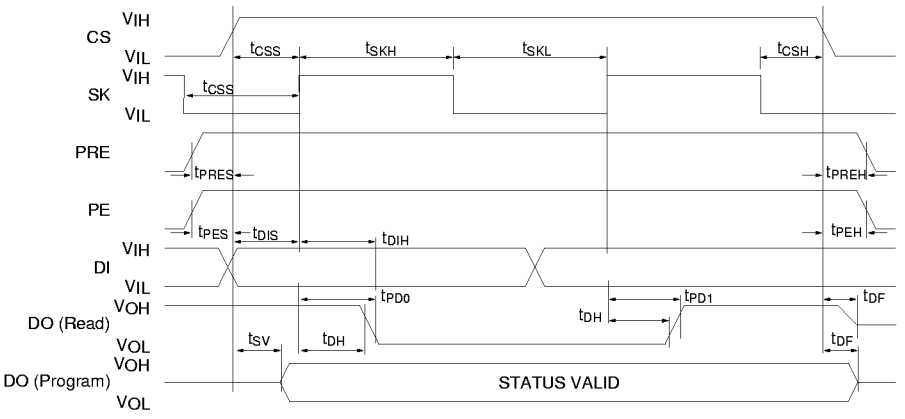
Functional Description (Continued)

Instruction Set for the NM93CS46

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Enable all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

Synchronous Data Timing



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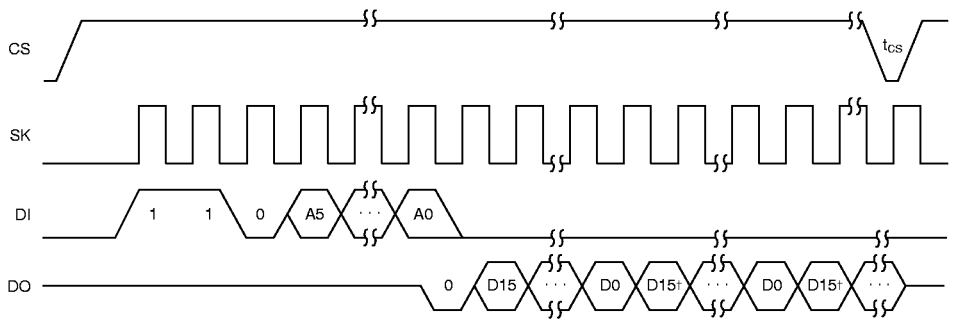
READ:
PRE = 0, PE = X



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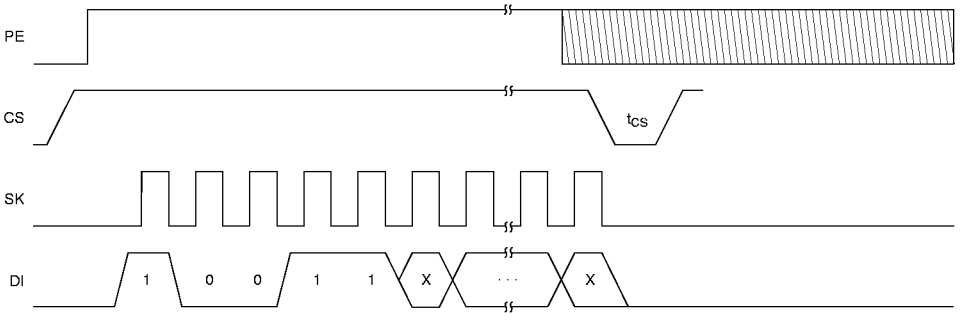
†The memory automatically cycles to the next register with continued clocking of SK.

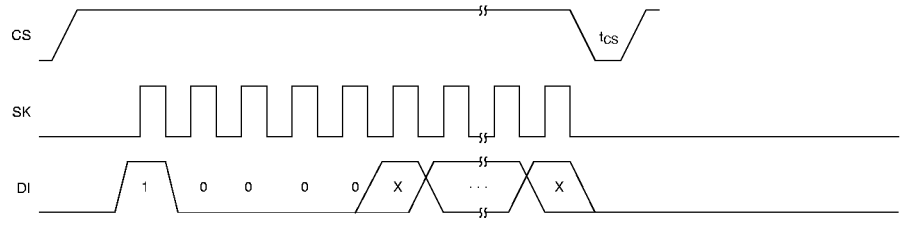
WEN:
PRE = 0, D0 = TRI-STATE



DS500084-6

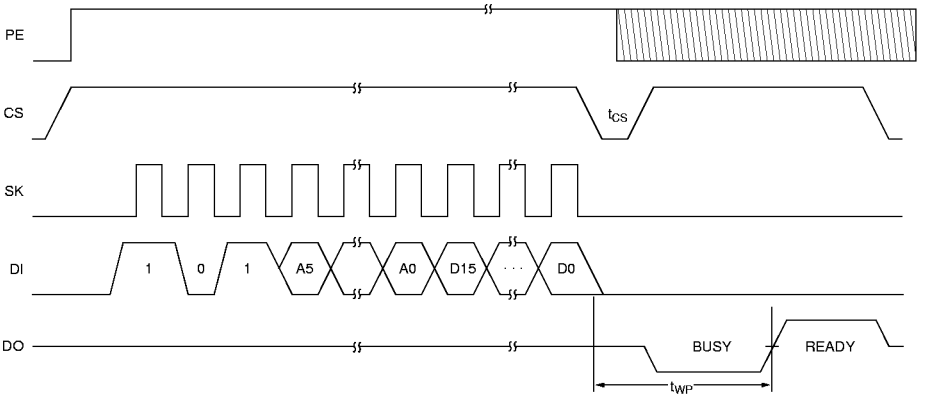
Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE



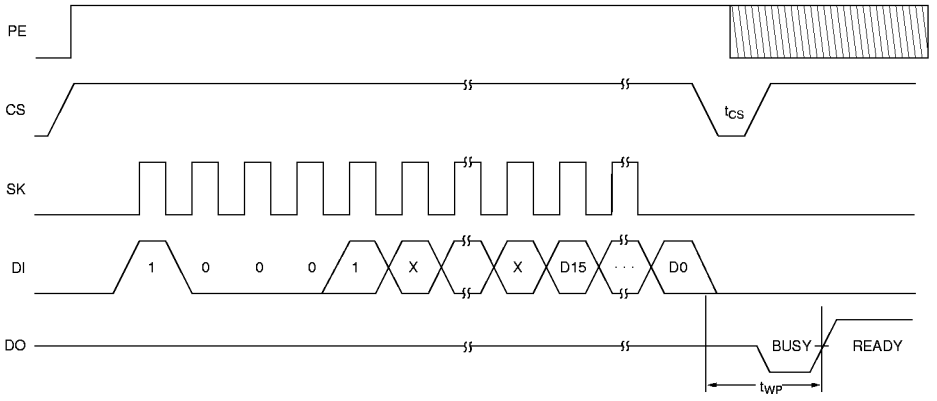
DS500084-7

WRITE:
PRE = 0



DS500084-8

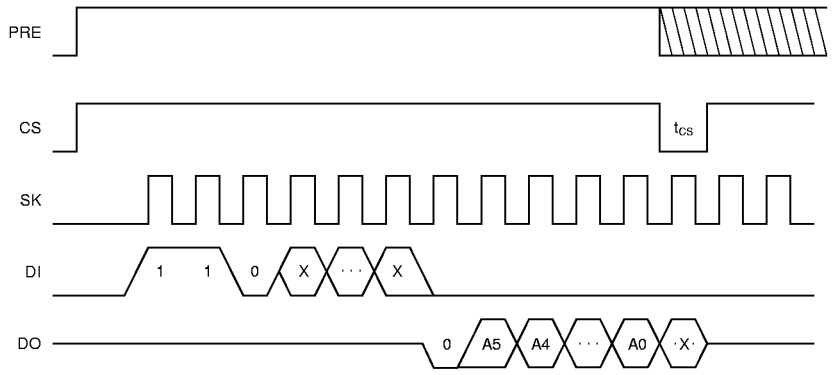
WRALL:
PRE = 0
(PROTECT REGISTER MUST BE CLEARED)



DS500084-9

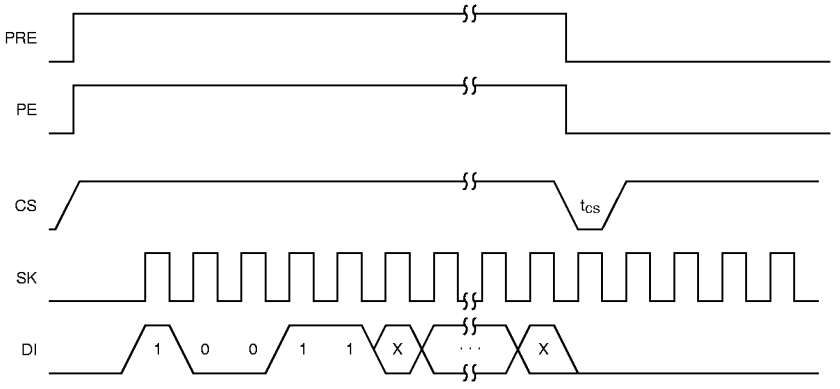
Timing Diagrams (Continued)

PRREAD:
PE = X



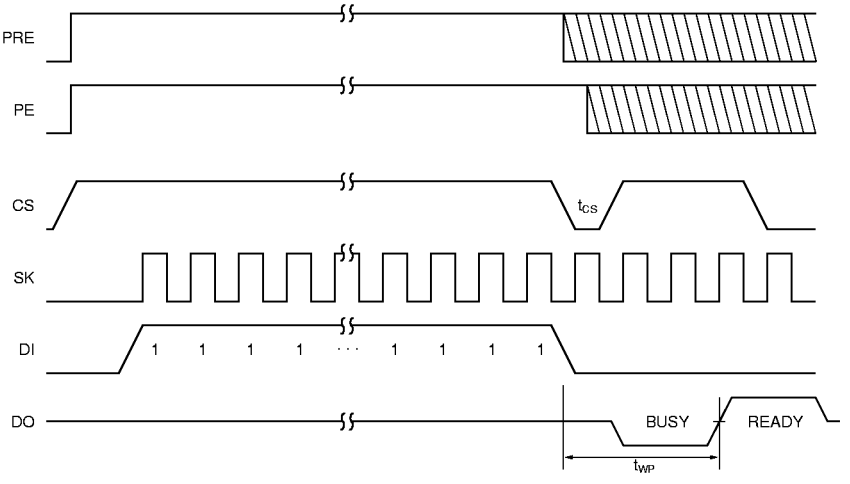
DS500084-10

PREN:
D0 = TRI-STATE
(A WEN CYCLE MUST PRECEDE A PREN CYCLE)



DS500084-11

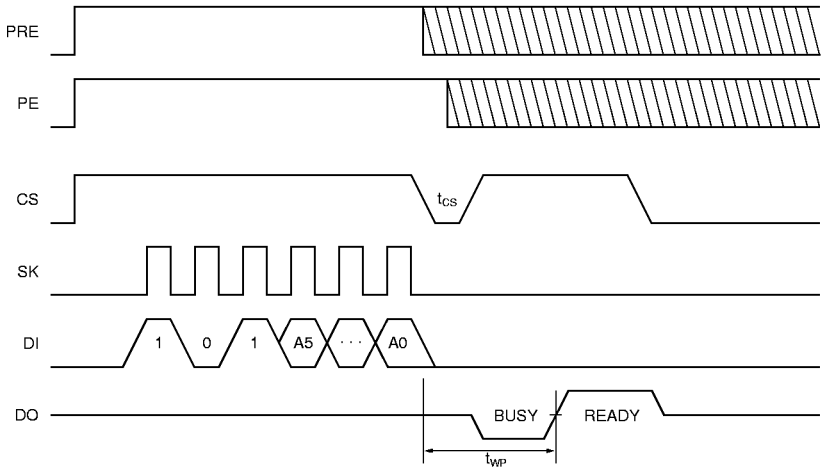
PRCLEAR:
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)



DS500084-12

Timing Diagrams (Continued)

PRWRITE:
(PREN CYCLES MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.)



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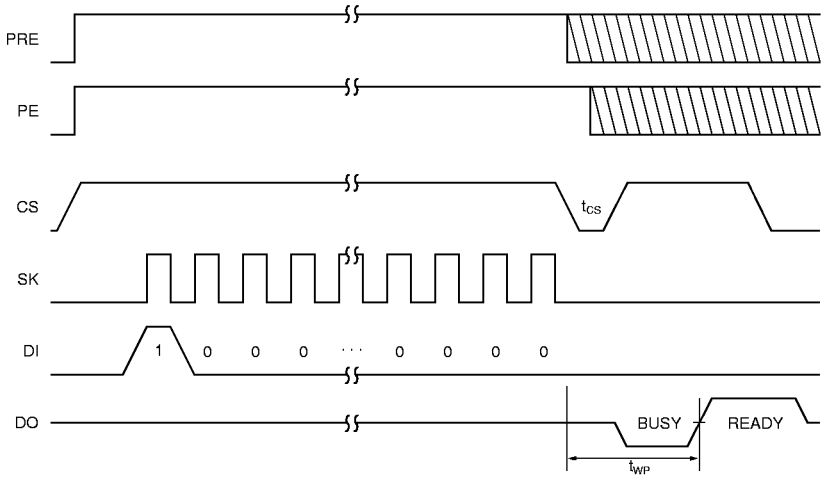
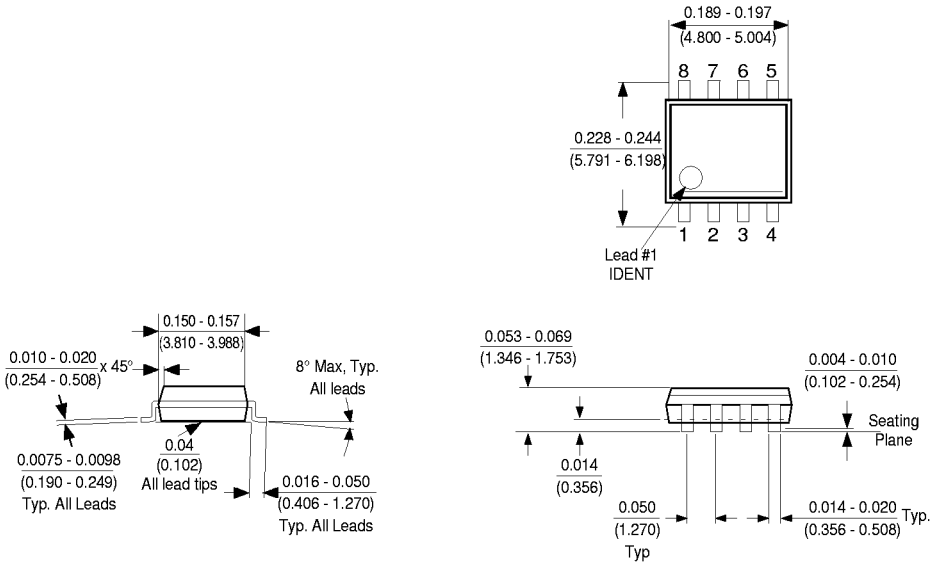
PRDS:
(*ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)



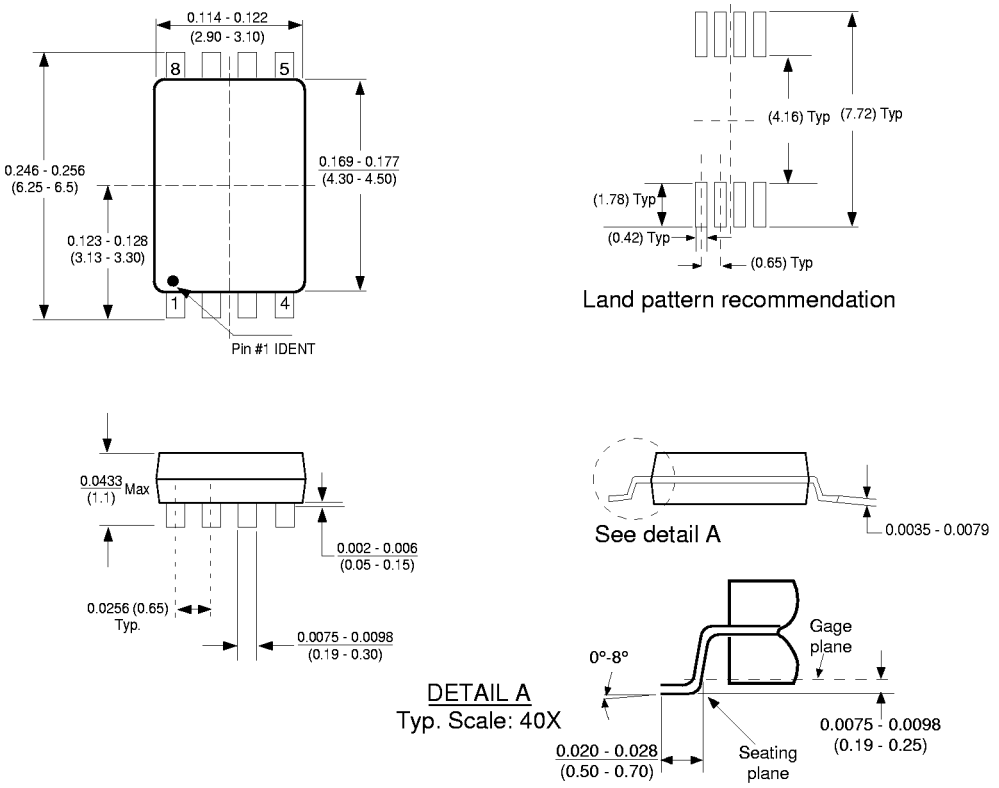
DS500084-14

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

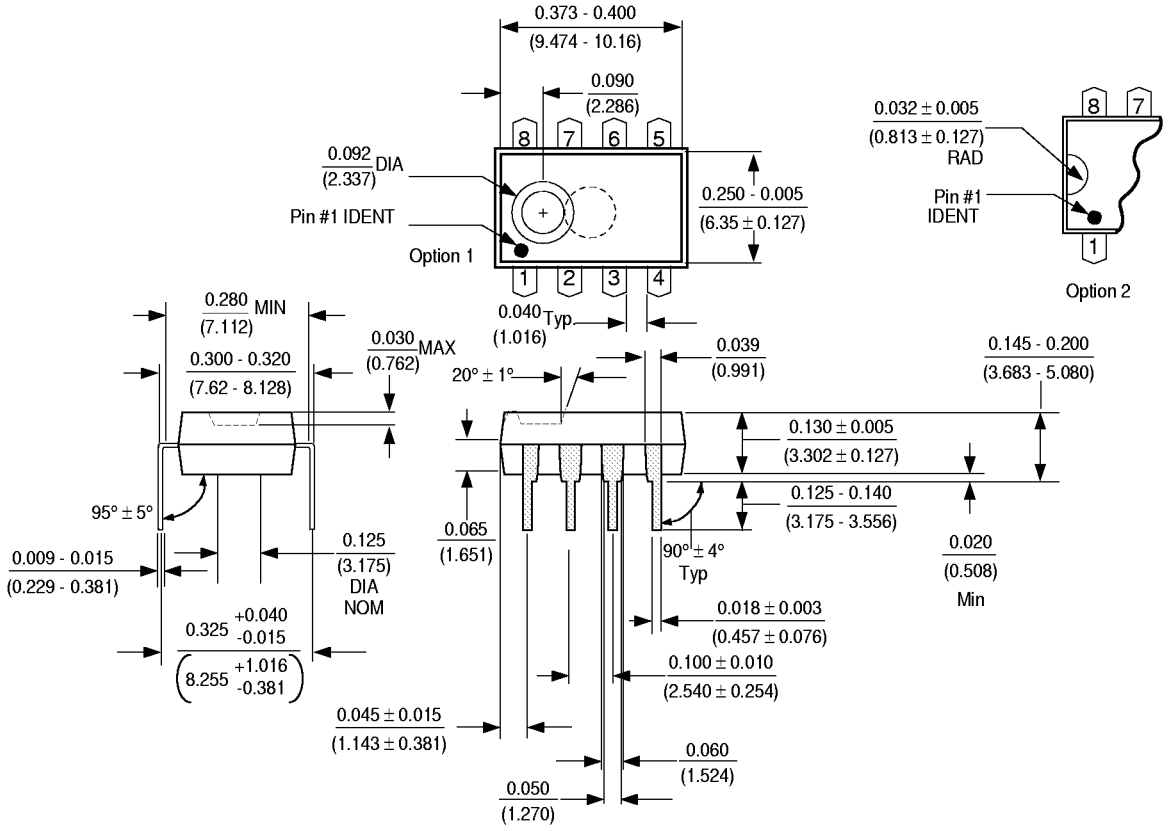


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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