



0.8 Ω , Low-Voltage, 4-Channel Analog Multiplexer

MAX4734

General Description

The MAX4734 is a low on-resistance, low-voltage, 4-channel CMOS analog multiplexer that operates from a single 1.6V to 3.6V supply. This device has fast switching speeds ($t_{ON} = 25\text{ns}$, $t_{OFF} = 20\text{ns}$ max), handles rail-to-rail analog signals, and consumes less than $4\mu\text{W}$ of quiescent power. The MAX4734 has break-before-make switching.

When powered from a 3V supply, the MAX4734 features low 0.8Ω (max) on-resistance (R_{ON}), with 0.2Ω (max) R_{ON} matching and 0.1Ω R_{ON} flatness. The digital logic input is 1.8V CMOS compatible when using a single 3V supply.

The MAX4734 is available in space-saving 12-pin thin QFN (3mm x 3mm) and 10-pin μMAX packages.

Features

- ◆ **Low R_{ON}**
 0.8Ω (max) (3V Supply)
 2Ω (max) (1.8V Supply)
- ◆ **0.1Ω (max) R_{ON} Flatness (3V Supply)**
- ◆ **1.6V to 3.6V Single-Supply Operation**
- ◆ **Available in Thin QFN (3mm x 3mm) Package**
- ◆ **High-Current Handling Capacity (150mA Continuous)**
- ◆ **1.8V CMOS-Logic Compatible (3V Supply)**
- ◆ **Fast Switching: $t_{ON} = 25\text{ns}$, $t_{OFF} = 20\text{ns}$**

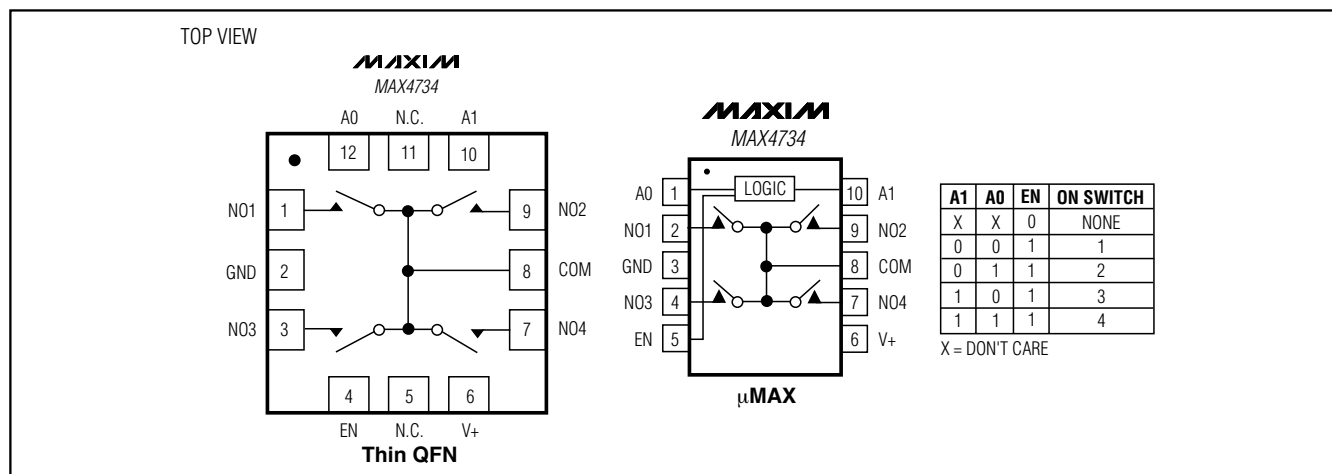
Applications

Power Routing
 Battery-Powered Systems
 Audio and Video Signal Routing
 Low-Voltage Data-Acquisition Systems
 Communications Circuits
 PCMCIA Cards
 Cellular Phones
 Modems
 Hard Drives

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4734EU	-40°C to +85°C	10 μMAX
MAX4734ETC	-40°C to +85°C	12 Thin QFN (3mm x 3mm)

Pin Configurations/Functional Diagrams/Truth Table



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ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)

V+, A₋, EN₋ -0.3V to +4V
 COM, NO₋ (Note 1) -0.3V to (V₊ + 0.3V)
 Continuous Current COM, NO₋ ± 150 mA
 Continuous Current (all other pins) ± 20 mA
 Peak Current COM, NO₋
 (pulsed at 1ms 10% duty cycle) ± 300 mA

Continuous Power Dissipation (T_A = +70°C)

10-Pin μ MAX (derate 5.6mW/°C above +70°C) 444mW
 12-Pin Thin QFN (derate 14.7mW/°C above +70°C) .. 1176mW
 Operating Temperature Range -40°C to +85°C
 Maximum Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Note 1: Signals on COM or NO₋ exceeding V₊ or GND are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single 3V Supply

(V₊ = 2.7V to 3.6V, V_{IH} = 1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V₊ = 3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM} , V _{NO-}			0		V ₊	V
On-Resistance (Note 4)	R _{ON}	V ₊ = 2.7V, I _{COM} = 100mA, V _{NO-} = 1.5V	+25°C		0.6	0.8	Ω
			T _{MIN} to T _{MAX}			1	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V ₊ = 2.7V, I _{COM} = 100mA, V _{NO-} = 1.5V	+25°C		0.1	0.2	Ω
			T _{MIN} to T _{MAX}			0.3	
On-Resistance Flatness (Note 6)	R _{FLAT(ON)}	V ₊ = 2.7V, I _{COM} = 100mA, V _{NO-} = 1V, 1.5V, 2V	+25°C		0.05	0.1	Ω
			T _{MIN} to T _{MAX}			0.2	
NO ₋ Off-Leakage Current (Note 7)	I _{NO-(OFF)}	V ₊ = 3.6V, V _{COM} = 0.3V, 3.3V, V _{NO-} = 3.3V, 0.3V	+25°C	-1	± 0.002	+1	nA
			T _{MIN} to T _{MAX}	-5		+5	
COM Off-Leakage Current (Note 7)	I _{COM(OFF)}	V ₊ = 3.6V, V _{COM} = 0.3V, 3.3V, V _{NO-} = 3.3V, 0.3V	+25°C	-1	± 0.002	+1	nA
			T _{MIN} to T _{MAX}	-5		+5	
COM On-Leakage Current (Note 7)	I _{COM(ON)}	V ₊ = 3.6V, V _{COM} = 3.3V, 0.3V, V _{NO-} = 3.3V, 0.3V, or floating	+25°C	-2	± 0.002	+2	nA
			T _{MIN} to T _{MAX}	-10		+10	

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ELECTRICAL CHARACTERISTICS—Single 3V Supply (continued)

(V₊ = 2.7V to 3.6V, V_{IH} = 1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V₊ = 3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} = 1.5V, R _L = 50 Ω , C _L = 35pF, Figure 1	+25°C		20	25	ns
			T _{MIN} to T _{MAX}			30	
Turn-Off Time	t _{OFF}	V _{NO_} = 1.5V, R _L = 50 Ω , C _L = 35pF, Figure 1	+25°C		15	20	ns
			T _{MIN} to T _{MAX}			25	
Break-Before-Make (Note 8)	t _{BBM}	V _{NO_} = 1.5V, R _L = 50 Ω , C _L = 35pF, Figure 2	+25°C		5		ns
			T _{MIN} to T _{MAX}	1			
Charge Injection	Q	V _{GEN} = 0, R _{GEN} = 0, C _L = 1.0nF, Figure 3	+25°C		60		pC
NO_ Off-Capacitance	C _{OFF}	f = 1MHz, Figure 4	+25°C		33		pF
COM Off-Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 4	+25°C		117		pF
COM On-Capacitance	C _{COM(ON)}	f = 1MHz, Figure 4	+25°C		171		pF
-3dB On-Channel Bandwidth	BW	Signal = 0, R _{IN} = R _{OUT} = 50 Ω , C _L = 5pF, Figure 5			90		MHz
Off-Isolation (Note 9)	V _{ISO}	f = 1MHz, V _{COM} = 1V _{P-P} , R _L = 50 Ω , C _L = 5pF, Figure 5	+25°C		-56		dB
Crosstalk (Note 10)	V _{CT}	f = 1MHz, V _{COM} = 1V _{P-P} , R _L = 50 Ω , C _L = 5pF, Figure 5	+25°C		-56		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V _{COM} = 2V _{P-P} , R _L = 32 Ω	+25°C		0.018		%
LOGIC INPUT (A₋, EN)							
Input Logic High	V _{IH}			1.4			V
Input Logic Low	V _{IL}					0.5	V
Input Leakage Current	I _{IN}	V _{EN} = 0 or 3.6V, V _{A_-} = 0 or 3.6V		-1	0.005	+1	μ A
POWER SUPPLY							
Power-Supply Range	V ₊			1.6		3.6	V
Positive Supply Current	I ₊	V ₊ = 3.6V, V _{EN} , A ₋ = 0 or V ₊ , all channels on or off			0.004	1	μ A

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ELECTRICAL CHARACTERISTICS—Single 1.8V Supply

($V_+ = 1.8V$, $V_{IH} = 1.0V$, $V_{IL} = 0.4V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified. Typical values are at $T_A = +25^\circ C$.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM} , V _{NO_}			0		V ₊	V
On-Resistance	R _{ON}	I _{COM_} = 10mA, V _{NO_} = 1V	+25°C	1.5	2	Ω	
			T _{MIN} to T _{MAX}		3		
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} = 1V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C	25	30	ns	
			T _{MIN} to T _{MAX}		35		
Turn-Off Time	t _{OFF}	V _{NO_} = 1V, R _L = 50Ω, C _L = 35pF, Figure 1	+25°C	18	25	ns	
			T _{MIN} to T _{MAX}		28		
Break-Before-Make (Note 8)	t _{BBM}	V _{NO_} = 1V, R _L = 50Ω, C _L = 35pF, Figure 2	+25°C	7		ns	
			T _{MIN} to T _{MAX}	1			
Charge Injection	Q	V _{GEN} = 0, R _{GEN} = 0, C _L = 1nF, Figure 3	+25°C	35		pC	
Off-Isolation (Note 9)	V _{ISO}	f = 1MHz, V _{NO_} = 1V _{P-P} , R _L = 50Ω, C _L = 5pF, Figure 5	+25°C	-56		dB	
Crosstalk (Note 10)	V _{CT}	f = 1MHz, V _{COM} = 1V _{P-P} , R _L = 50Ω, C _L = 5pF, Figure 5	+25°C	-56		dB	
LOGIC INPUT (A ₋ , EN)							
Input Logic High	V _{IH}			1		V	
Input Logic Low	V _{IL}				0.4	V	
Input Leakage Current	I _{IN}	V _{EN} = 0 or 3.6V, V _{A_-} = 0 or 3.6V			1	μA	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.

Note 3: $-40^\circ C$ specifications are guaranteed by design.

Note 4: R_{ON} and ΔR_{ON} matching specifications for thin QFN packaged parts are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Leakage parameters are 100% tested at hot temperature and guaranteed by correlation at room temperature.

Note 8: Guaranteed by design.

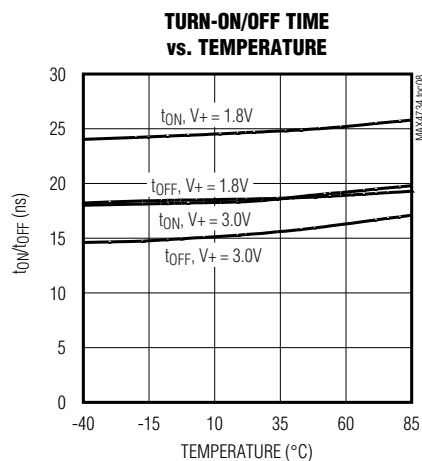
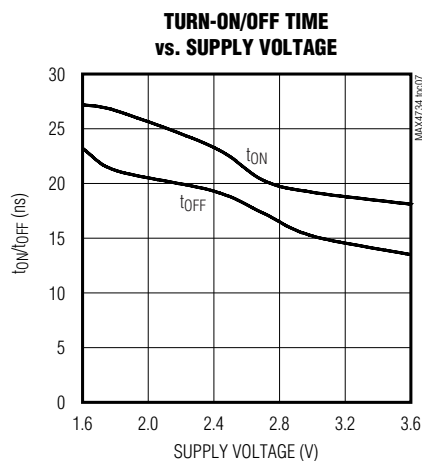
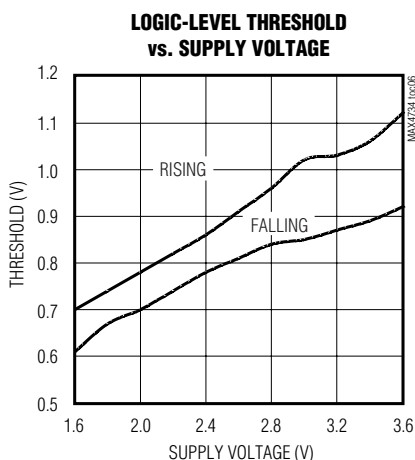
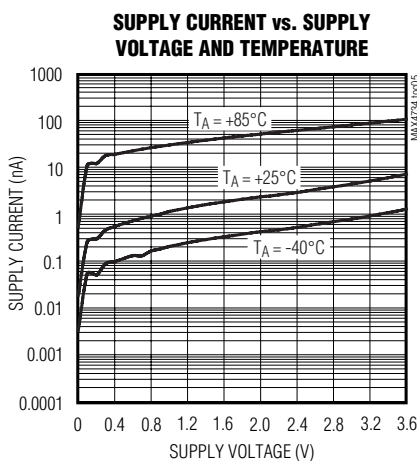
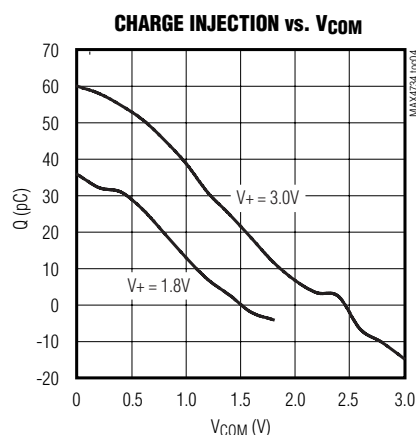
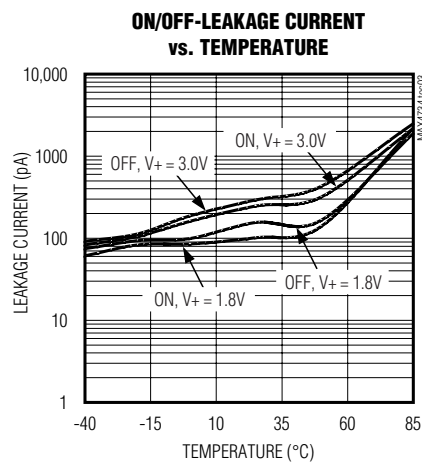
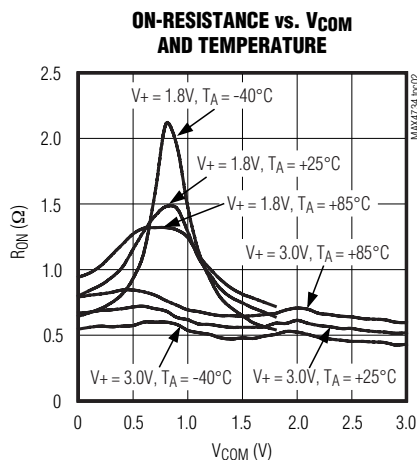
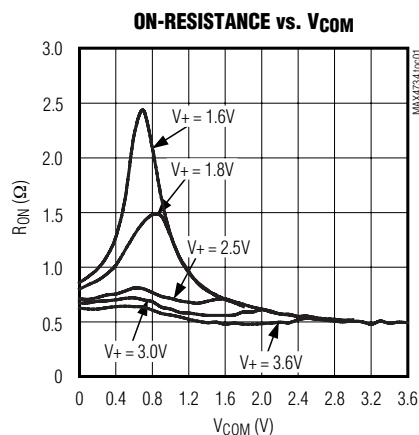
Note 9: Off-Isolation = $20\log_{10}(V_{COM}/V_{NO-})$, V_{COM} = output, V_{NO-} = input to off switch.

Note 10: Between two switches.

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Typical Operating Characteristics

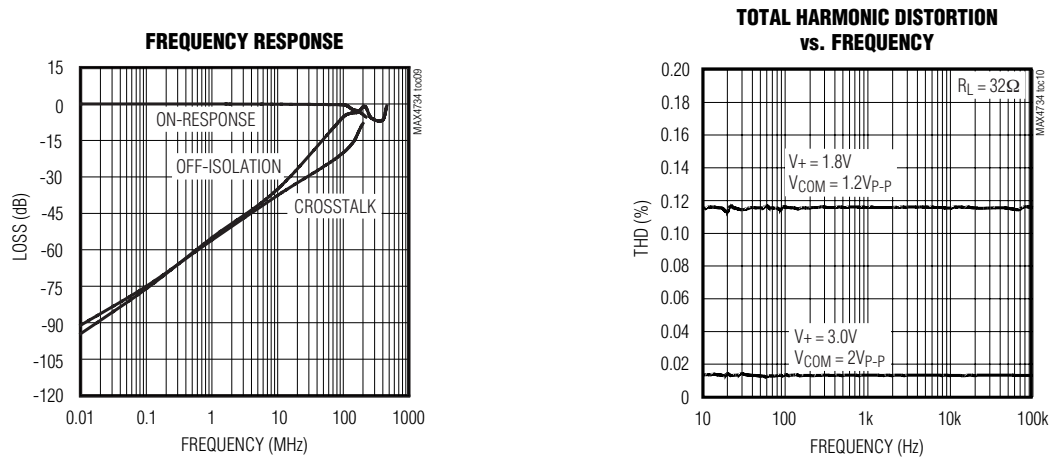
($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
μMAX	QFN		
1	12	A0	Address 0 Input
2	1	NO1	Analog Switch 1—Normally Open Terminal
3	2	GND	Ground
4	3	NO3	Analog Switch 3—Normally Open Terminal
5	4	EN	Enable Logic Input
6	6	V+	Positive-Supply Voltage Input
7	7	NO4	Analog Switch 4—Normally Open Terminal
8	8	COM	Analog Switch Common Terminal
9	9	NO2	Analog Switch 2—Normally Open Terminal
10	10	A1	Address 1 Input
—	5, 11	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Pad. Connect to Ground.

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Logic Inputs

The MAX4734 is a low 0.8Ω (max) (at $V_+ = 2.7V$) on-resistance, low-voltage, 4-channel CMOS analog multiplexer that operates from a 1.6V to 3.6V single supply. CMOS switch construction allows switching analog signals that range from GND to V_+ .

When powered from a 2.7V supply, the 0.8Ω (max) R_{ON} allows high continuous currents to be switched in a variety of applications.

Applications Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, followed by NO₂ or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V₊ supply to other components. A 0.1μF capacitor, connected from V₊ to GND, is adequate for most applications.

The MAX4734 logic inputs can be driven up to 3.6V regardless of the supply voltage. For example, with a 1.8V supply, A₋ and EN may be driven low to GND and high to 3.6V. Driving A₋ and EN rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be passed with very little change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_ and COM_ pins can be used as either inputs or outputs.

Lavout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

Test Circuits/Timing Diagrams

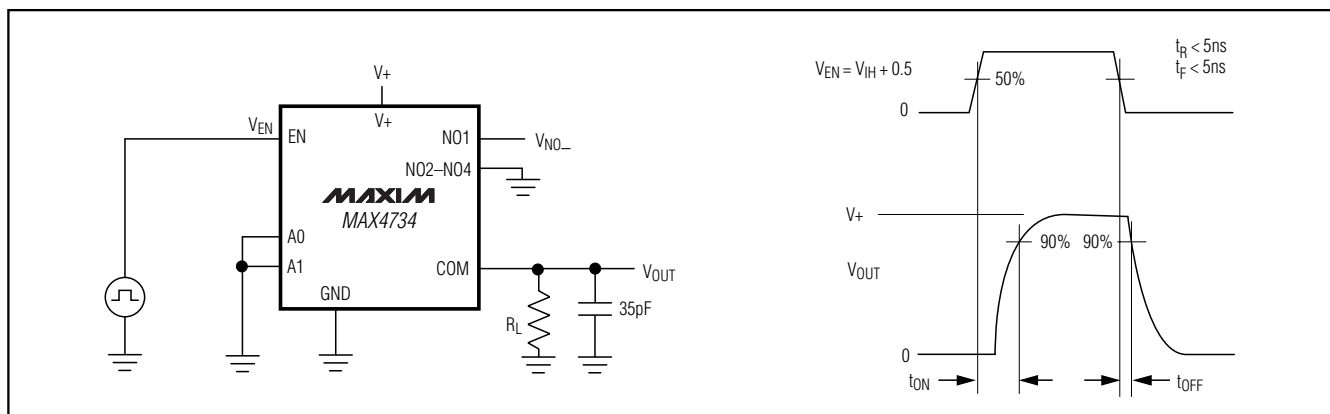
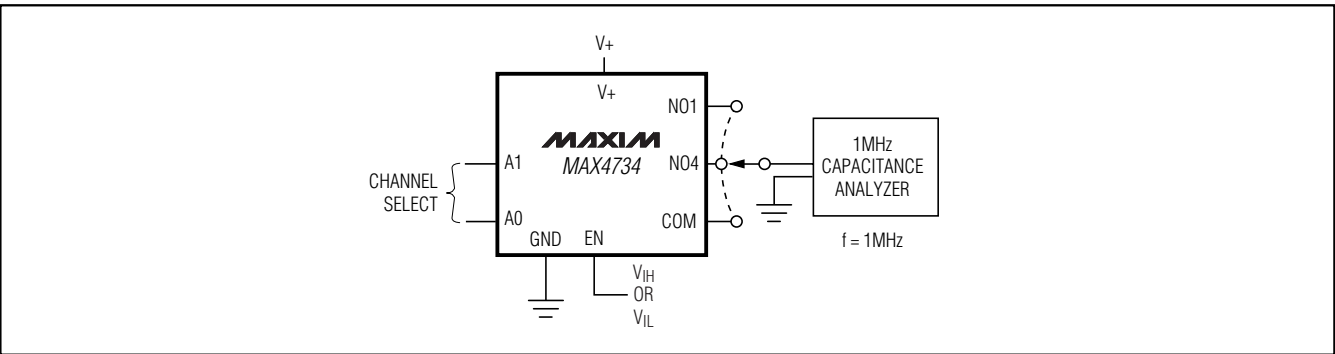
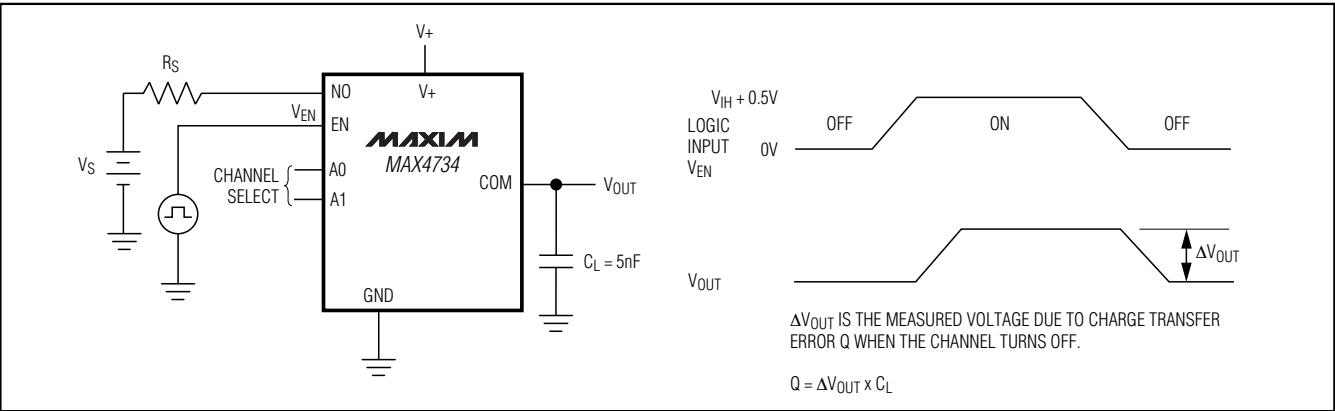
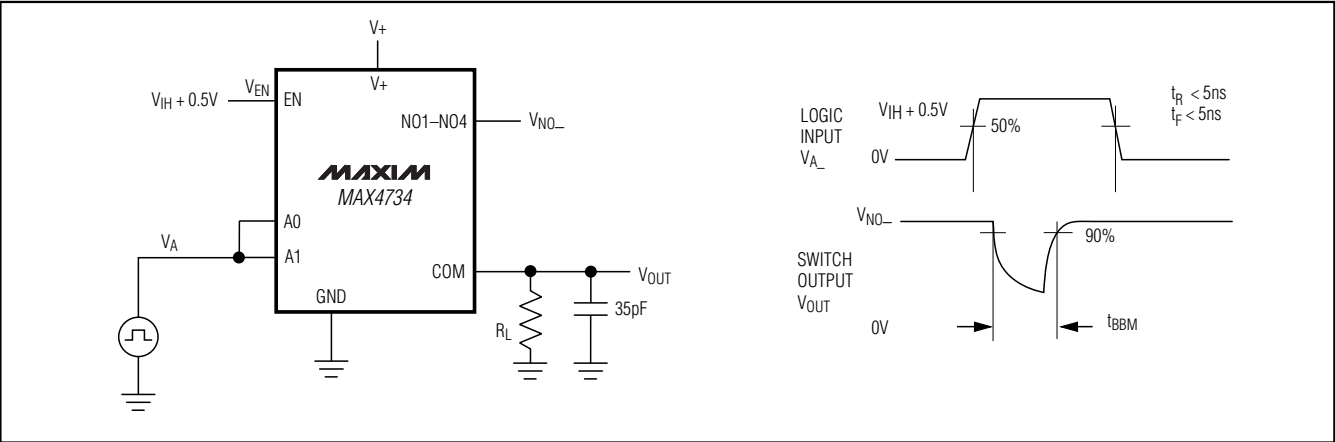


Figure 1. Switching Time

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Test Circuits/Timing Diagrams (continued)



0.8Ω, Low-Voltage, 4-Channel Analog Multiplexer

Test Circuits/Timing Diagrams (continued)

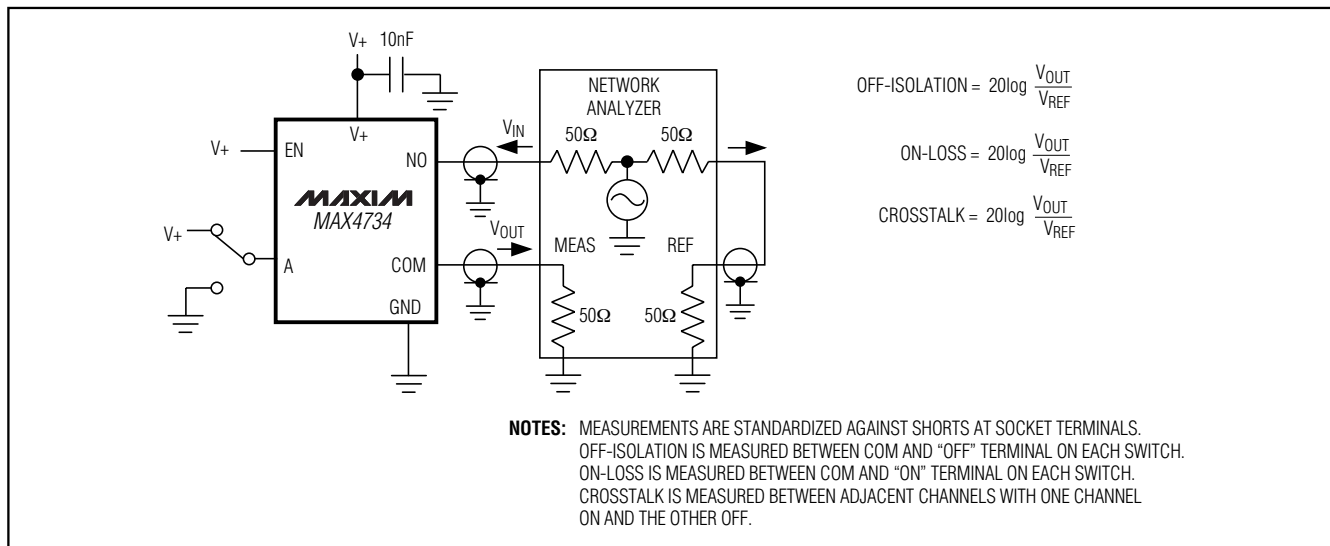


Figure 5. Off-Isolation/On-Channel/Crosstalk Bandwidth

Chip Information

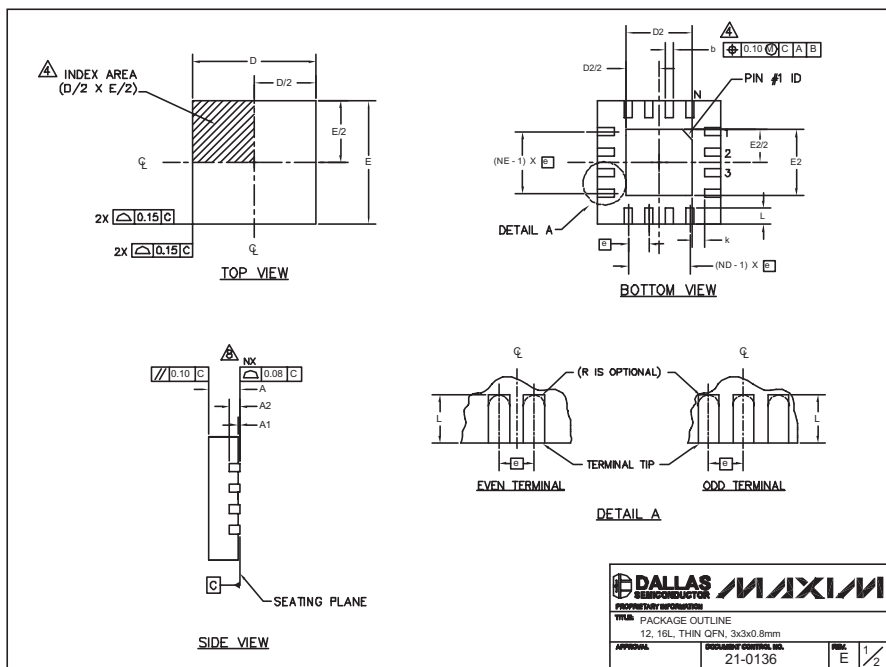
TRANSISTOR COUNT: 379

PROCESS: CMOS

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



PKG	12L 3x3				16L 3x3			
	REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80		0.70	0.75	0.80	
b	0.20	0.25	0.30		0.20	0.25	0.30	
D	2.90	3.00	3.10		2.90	3.00	3.10	
E	2.90	3.00	3.10		2.90	3.00	3.10	
e	0.50 BSC.				0.50 BSC.			
L	0.45	0.65	0.65		0.30	0.40	0.60	
N	12				16			
ND	3				4			
NE	3				4			
A1	0	0.02	0.05		0	0.02	0.05	
A2	0.20 REF				0.20 REF			
k	0.25	-	-		0.25	-	-	

PKG CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.05	1.10	1.25	0.05	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.05	1.10	1.25	0.05	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.05	1.10	1.25	0.05	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.05	1.10	1.25	0.05	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.05	0.80	0.85	0.05	0.80	0.85	0.225 x 45°	WEED-2	N/A
T1633-4	0.05	1.10	1.25	0.05	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

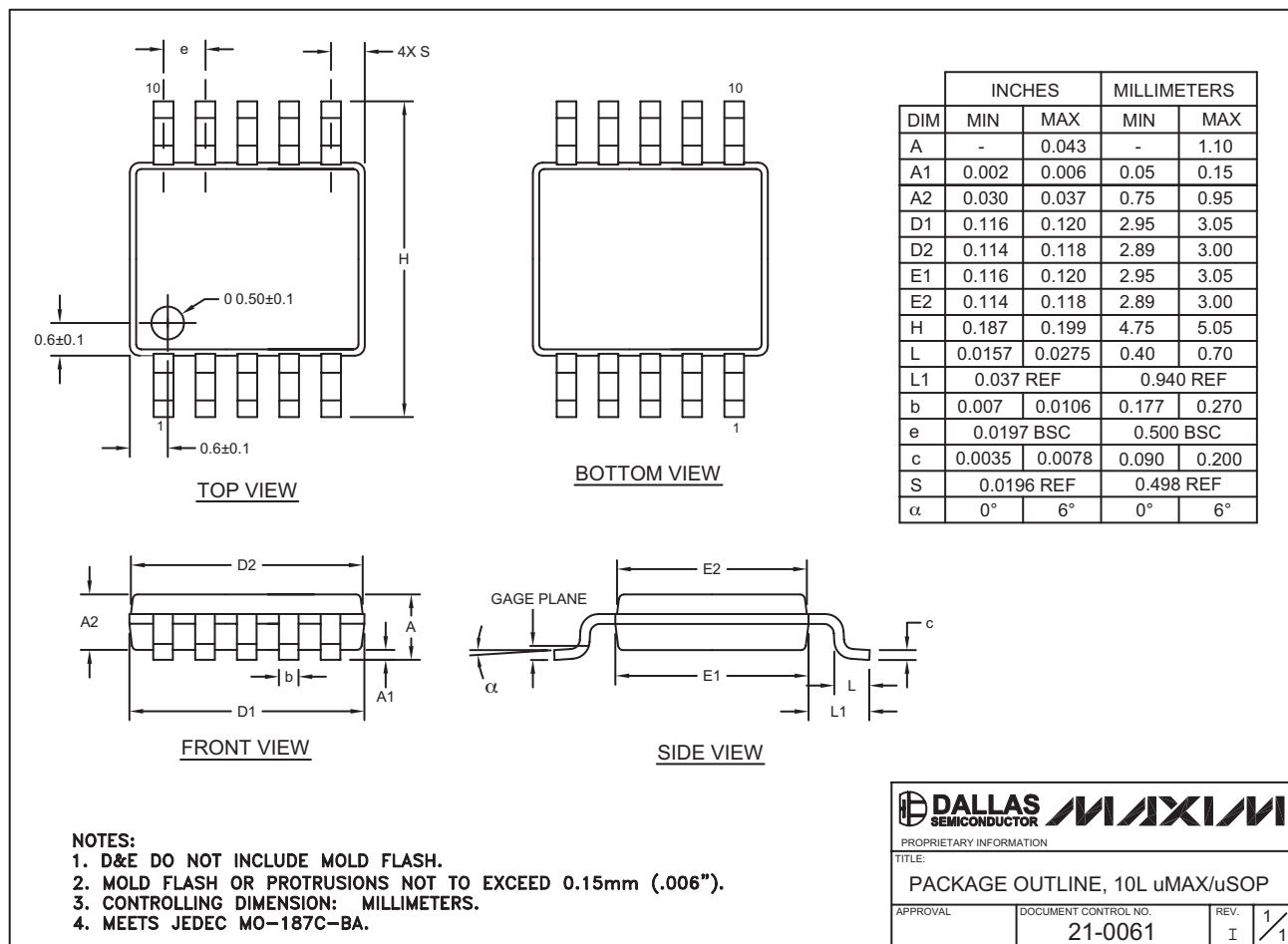
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE			
12, 16L, THIN QFN, 3x3x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	2
	21-0136	E	

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Package Information (continued)

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