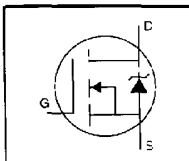


HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated



$$V_{DS} = 600V$$

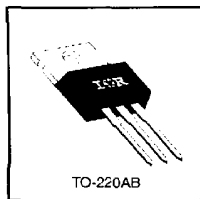
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 6.2A$$

Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power switching for switching applications.


Absolute Maximum Ratings

	Parameter	Max.	Units
$I_C @ T_C = 25^\circ C$	Continuous Drain Current, V _{GS} @ 10 V	6.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, V _{GS} @ 10 V	3.9	
I_{DW}	Pulsed Drain Current ①	25	
$P_D @ T_C = 25^\circ C$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS}	Single Pulse Avalanche Energy ②	530	mJ
I _{AS}	Avalanche Current ③	6.2	A
E _{AR}	Repetitive Avalanche Energy ③	13	mJ
dv/dt	Peak Diode Recovery dv/dt ④	3.0	V/ns
T _J	Operating Junction and Storage Temperature Range	-55 to +150	°C
T _{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	1.0	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
R _{θJA}	Junction-to-Ambient	—	—	62	

IRFBC40LC



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{DS(BR)}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$
$\Delta V_{DS(BR)}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.70	—	V/°C	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	$V_{GS}=10\text{V}$, $I_D=3.7\text{A}$ ①
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
g_{fs}	Forward Transconductance	3.7	—	—	S	$V_{DS}=100\text{V}$, $I_D=3.7\text{A}$ ①
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS}=-20\text{V}$
Q_g	Total Gate Charge	—	—	39	nC	$I_D=6.2\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	10	nC	$V_{DS}=360\text{V}$
Q_{gd}	Gate-to-Drain (Miller) Charge	—	—	9	nC	$V_{DS}=10\text{V}$ See Fig. 6 and 13 ③
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD}=30\text{V}$
t_r	Rise Time	—	20	—	ns	$I_D=6.2\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	27	—	ns	$R_G=9.1\Omega$
t_f	Fall Time	—	17	—	ns	$R_D=471\Omega$ See Figure 10 ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25 in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—	nH	
C_{iss}	Input Capacitance	—	1100	—	pF	$V_{GS}=0\text{V}$
C_{oss}	Output Capacitance	—	140	—	pF	$V_{DS}=25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	15	—	pF	$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	25	A	
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J=25^\circ\text{C}$, $I_S=6.2\text{A}$, $V_{GS}=0\text{V}$ ④
t_r	Reverse Recovery Time	—	440	680	ns	$T_J=25^\circ\text{C}$, $I_F=6.2\text{A}$
Q_{rr}	Reverse Recovery Charge	—	2.1	3.2	μC	$dI/dt=100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② $V_{DD}=50\text{V}$, starting $T_J=25^\circ\text{C}$, $L=25\text{mH}$, $R_G=25\Omega$, $I_{AS}=6.2\text{A}$ (See Figure 12)

③ $I_{SD}=6.2\text{A}$, $dI/dt=80\text{A}/\mu\text{s}$, $V_{DD}=V_{DS(BR)}$, $T_J=150^\circ\text{C}$

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$

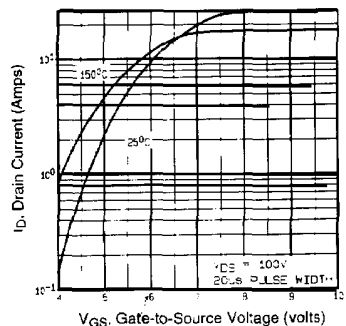
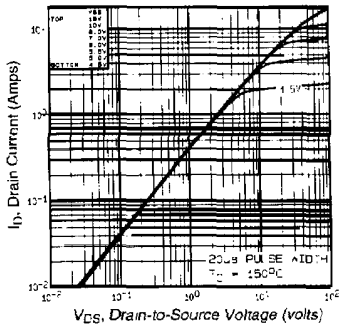
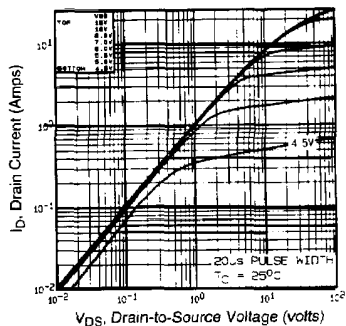


Fig 3. Typical Transfer Characteristics

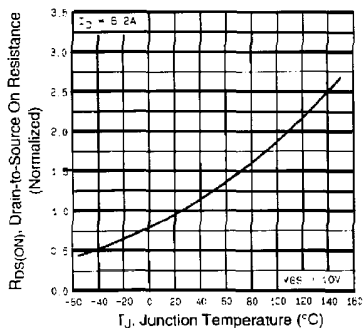


Fig 4. Normalized On-Resistance
Vs. Temperature

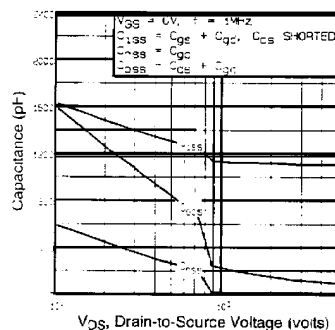


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

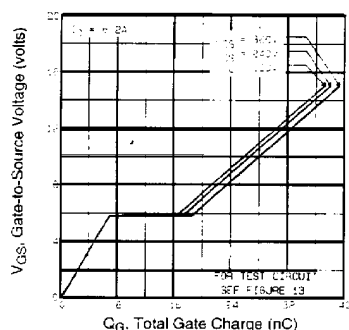


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

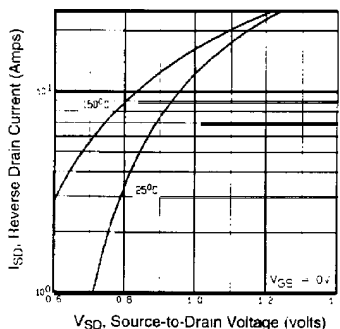


Fig 7. Typical Source-Drain Diode Forward Voltage

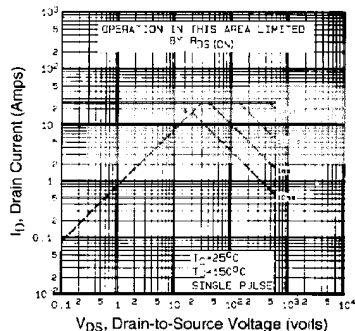


Fig 8. Maximum Safe Operating Area

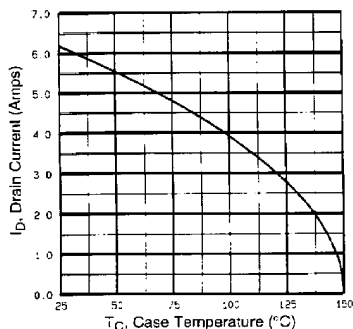


Fig 9. Maximum Drain Current Vs. Case Temperature

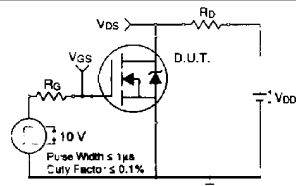


Fig 10a. Switching Time Test Circuit

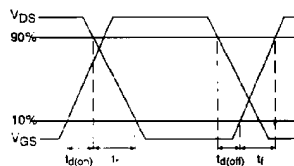


Fig 10b. Switching Time Waveforms

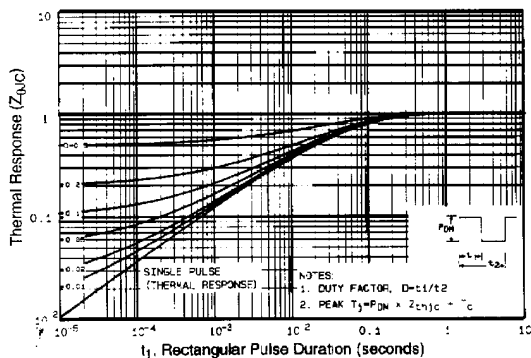


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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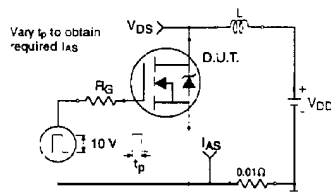


Fig 12a. Unclamped Inductive Test Circuit

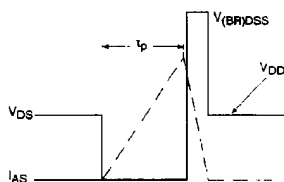


Fig 12b. Unclamped Inductive Waveforms

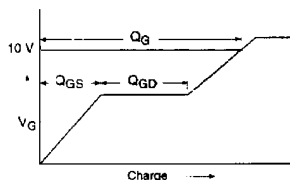


Fig 13a. Basic Gate Charge Waveform

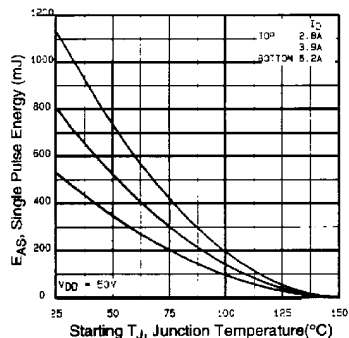


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

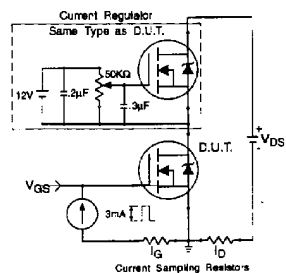


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

Appendix B: Package Outline Mechanical Drawing

Appendix C: Part Marking Information

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs

