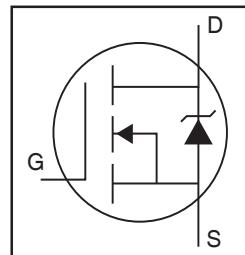


AUIRFS3306

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

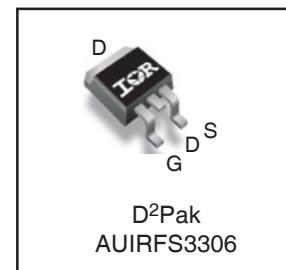


HEXFET® Power MOSFET

V_{DSS}	60V
$R_{DS(on)}$ typ.	3.3mΩ
max.	4.2mΩ
I_D (Silicon Limited)	160A ①
I_D (Package Limited)	120A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	160①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	110①	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ②	620	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	184	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	
E_{AR}	Repetitive Avalanche Energy ②	mJ	
dv/dt	Peak Diode Recovery ④	14	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
		300	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑥	—	40	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5\text{mA}$ ②
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	3.3	4.2	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$, $I_D = 75\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 150\mu\text{A}$
g_{fs}	Forward Transconductance	230	—	—	S	$V_{\text{DS}} = 50\text{V}$, $I_D = 75\text{A}$
R_G	Internal Gate Resistance	—	0.7	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 60\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 48\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -20\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	85	120	nC	$I_D = 75\text{A}$
Q_{gs}	Gate-to-Source Charge	—	20	—		$V_{\text{DS}} = 30\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	26	—		$V_{\text{GS}} = 10\text{V}$ ③
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{\text{gd}}$)	—	59	—		$I_D = 75\text{A}$, $V_{\text{DS}} = 0\text{V}$, $V_{\text{GS}} = 10\text{V}$
$t_{\text{d(on)}}$	Turn-On Delay Time	—	15	—	ns	$V_{\text{DD}} = 30\text{V}$
t_r	Rise Time	—	76	—		$I_D = 75\text{A}$
$t_{\text{d(off)}}$	Turn-Off Delay Time	—	40	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	77	—		$V_{\text{GS}} = 10\text{V}$ ③
C_{iss}	Input Capacitance	—	4520	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	500	—		$V_{\text{DS}} = 50\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	720	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 48V ⑦, See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related) ⑥	—	880	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 48V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	160 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
	Pulsed Source Current (Body Diode) ②	—	—	620	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_s = 75\text{A}$, $V_{\text{GS}} = 0\text{V}$ ③
	Reverse Recovery Time	—	31	—	ns	$T_J = 25^\circ\text{C}$
		—	35	—		$T_J = 125^\circ\text{C}$ $V_R = 51\text{V}$, $I_F = 75\text{A}$
Q_{rr}	Reverse Recovery Charge	—	34	—	nC	$T_J = 25^\circ\text{C}$
		—	45	—		$T_J = 125^\circ\text{C}$ $\text{di}/\text{dt} = 100\text{A}/\mu\text{s}$ ③
I_{RRM}	Reverse Recovery Current	—	1.9	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.04\text{mH}$
 $R_G = 25\Omega$, $I_{\text{AS}} = 96\text{A}$, $V_{\text{GS}} = 10\text{V}$. Part not recommended for use above this value.

- ④ $I_{\text{SD}} \leq 75\text{A}$, $\text{di}/\text{dt} \leq 1400\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .

Qualification Information[†]

		Automotive (per AEC-Q101) ^{††}	
Qualification Level		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D ² Pak	MSL1
ESD	Machine Model	Class M4 (+/- >800V) ^{†††} AEC-Q101-002	
	Human Body Model	Class H2 (+/- 3000V) ^{†††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- >2000V) ^{†††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

^{†††} Highest passing voltage.

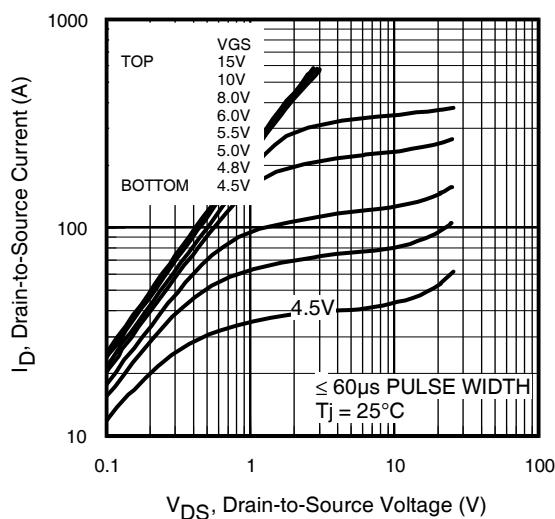


Fig 1. Typical Output Characteristics

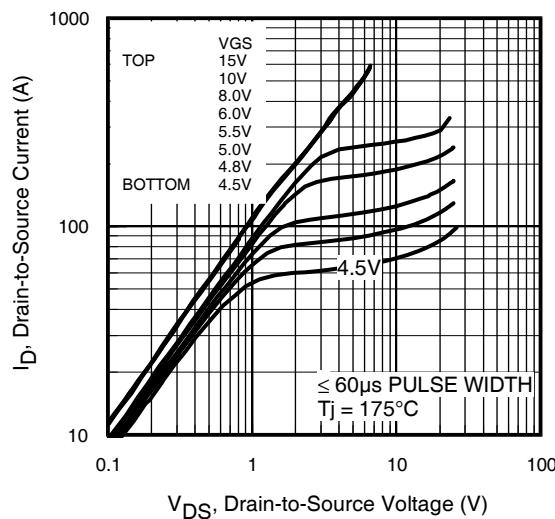


Fig 2. Typical Output Characteristics

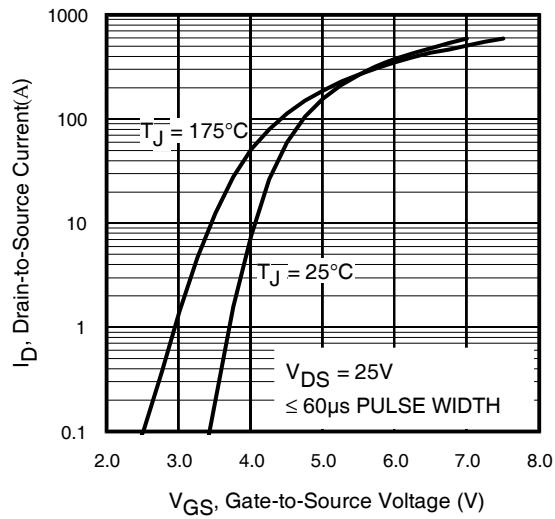


Fig 3. Typical Transfer Characteristics

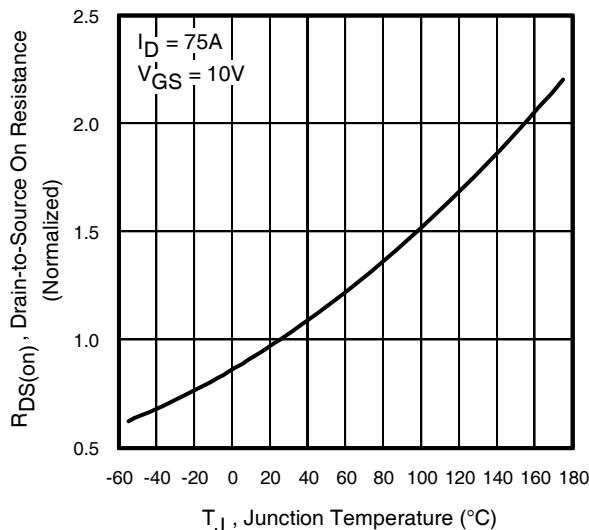


Fig 4. Normalized On-Resistance vs. Temperature

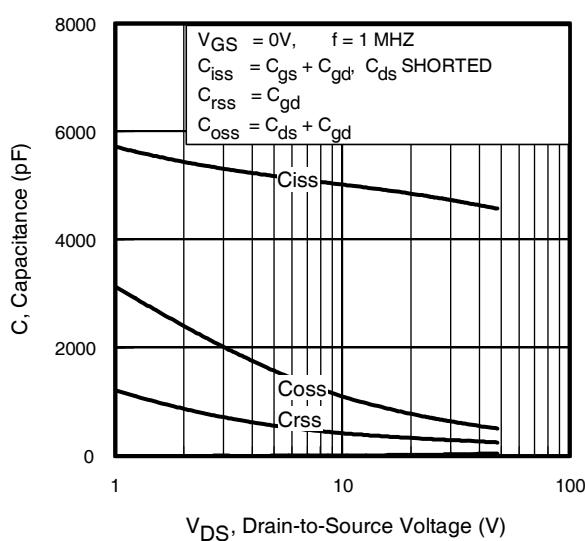


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

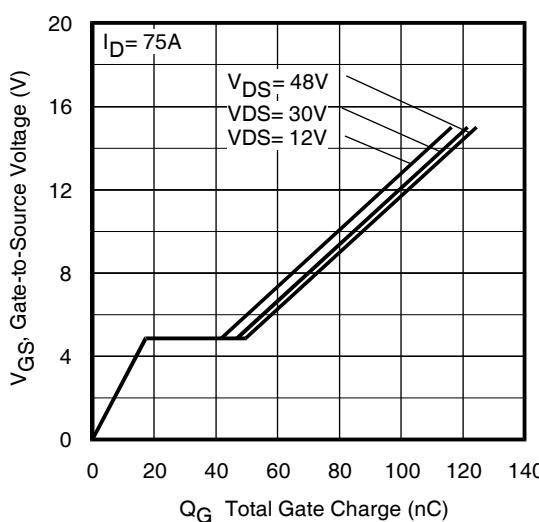


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

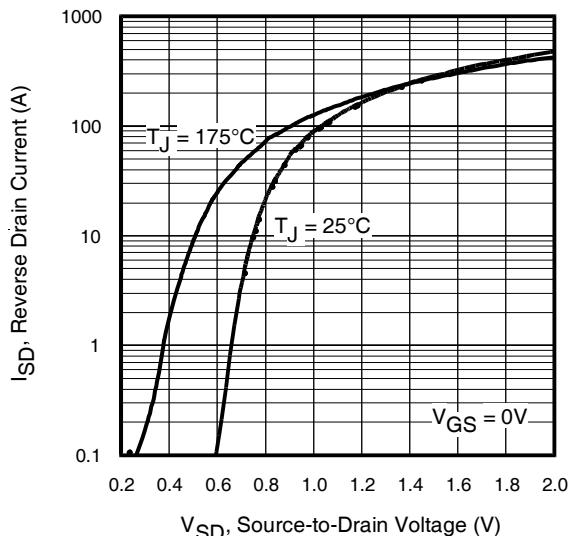


Fig 7. Typical Source-Drain Diode Forward Voltage

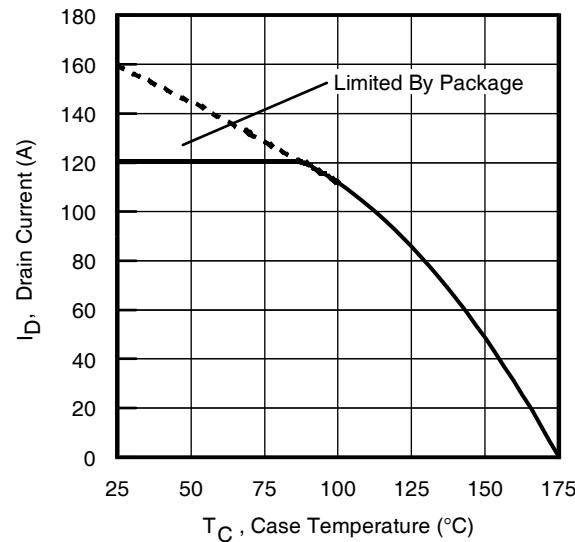


Fig 9. Maximum Drain Current vs. Case Temperature

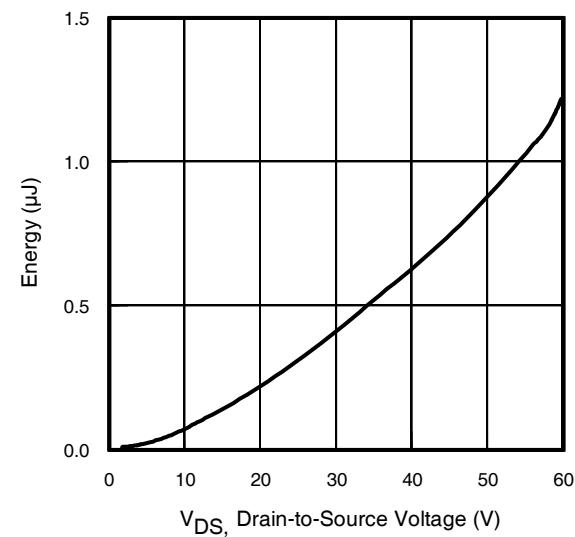


Fig 11. Typical C_{oss} Stored Energy

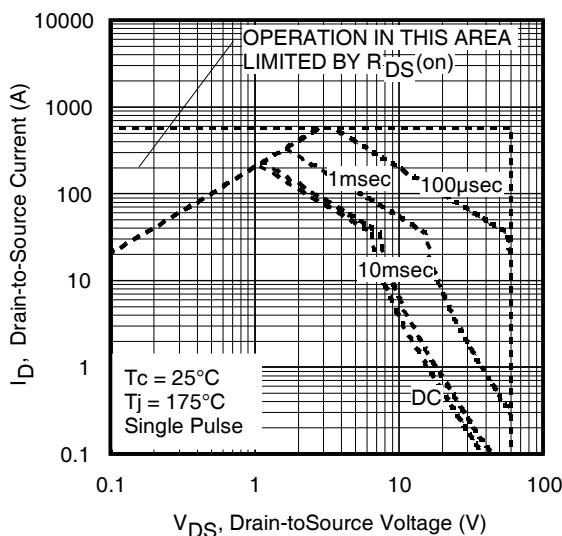


Fig 8. Maximum Safe Operating Area

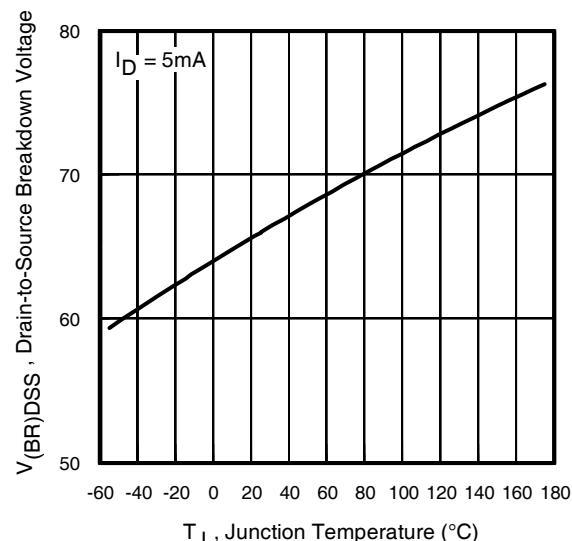


Fig 10. Drain-to-Source Breakdown Voltage

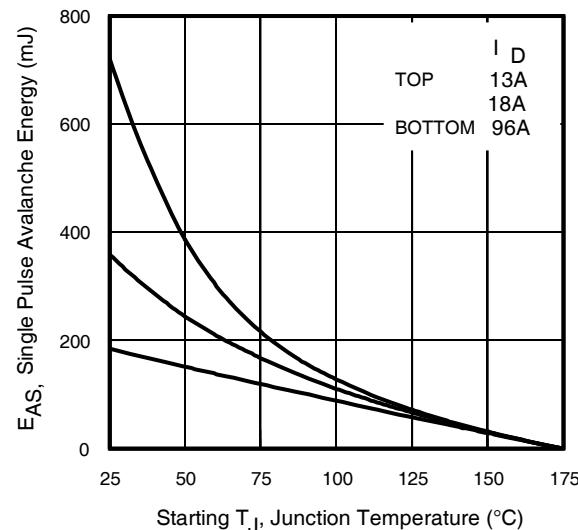


Fig 12. Maximum Avalanche Energy Vs. Drain Current

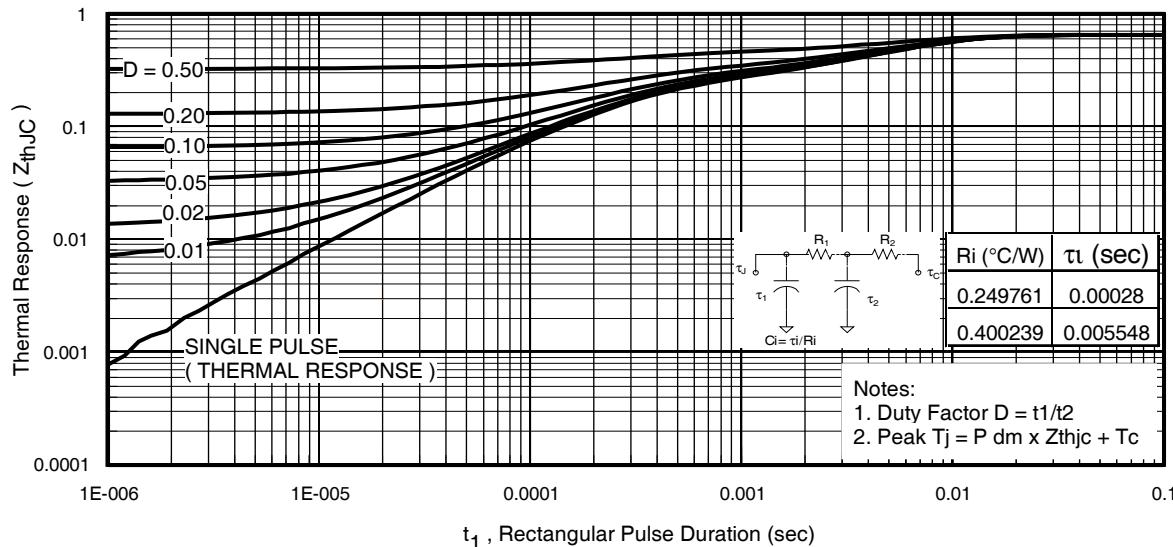


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

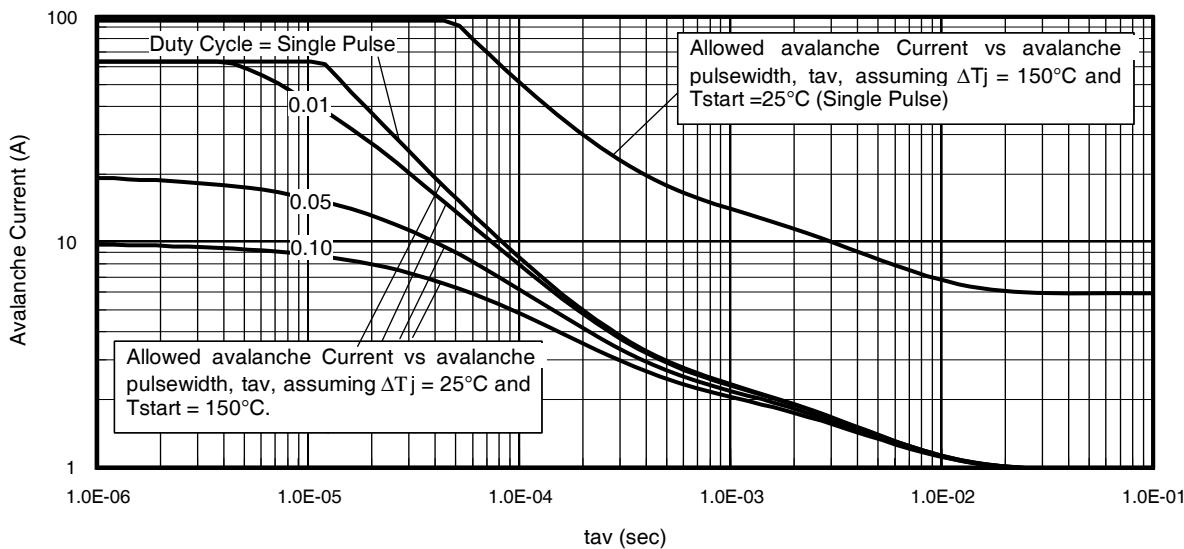
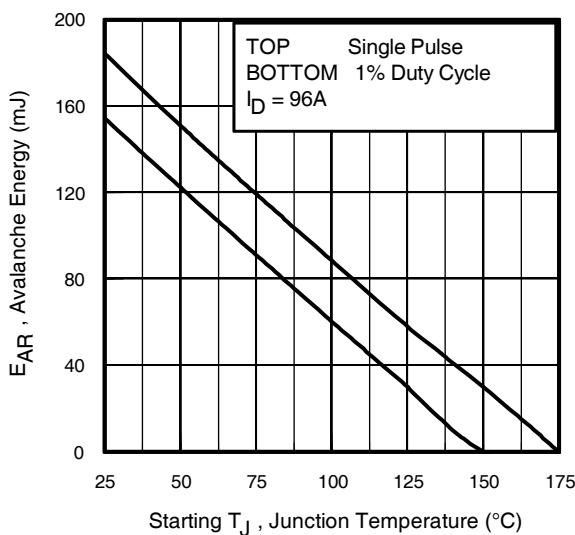


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
- t_{av} = Average time in avalanche.
- D = Duty cycle in avalanche = $t_{av} \cdot f$
- $Z_{th,JC}(D, t_{av})$ = Transient thermal resistance, see Figures 13

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{th,JC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

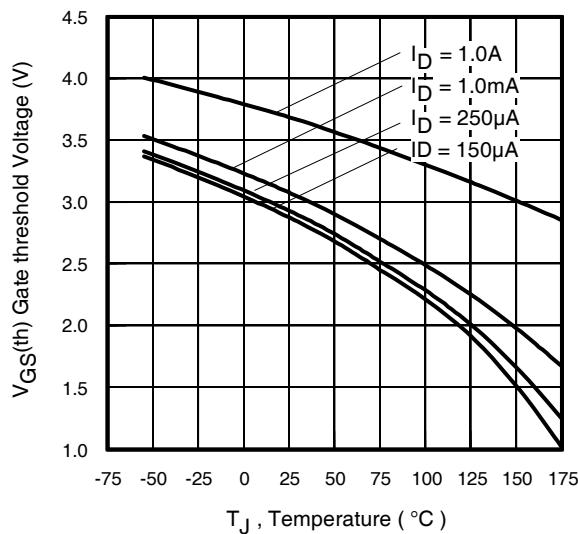


Fig. 16. Threshold Voltage Vs. Temperature

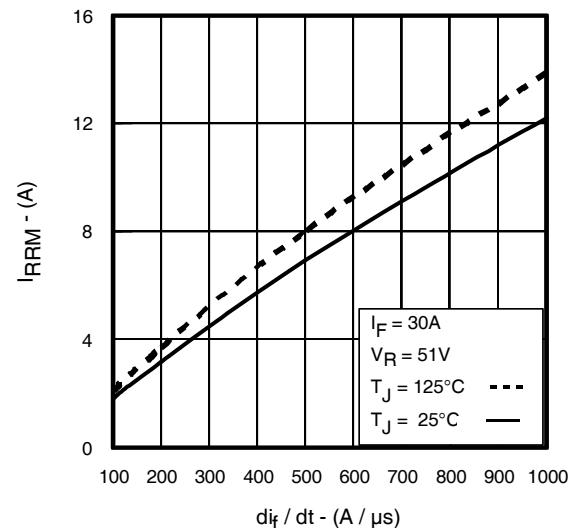


Fig. 17 - Typical Recovery Current vs. di_f/dt

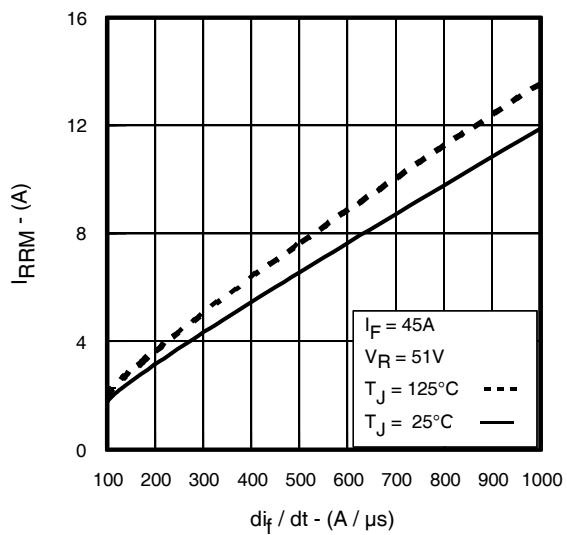


Fig. 18 - Typical Recovery Current vs. di_f/dt

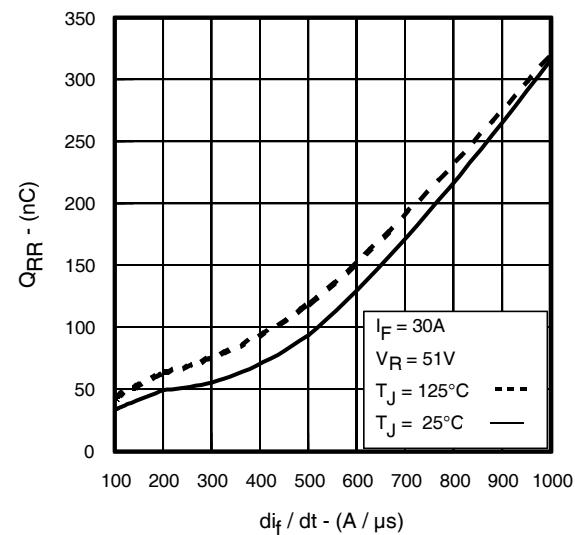


Fig. 19 - Typical Stored Charge vs. di_f/dt

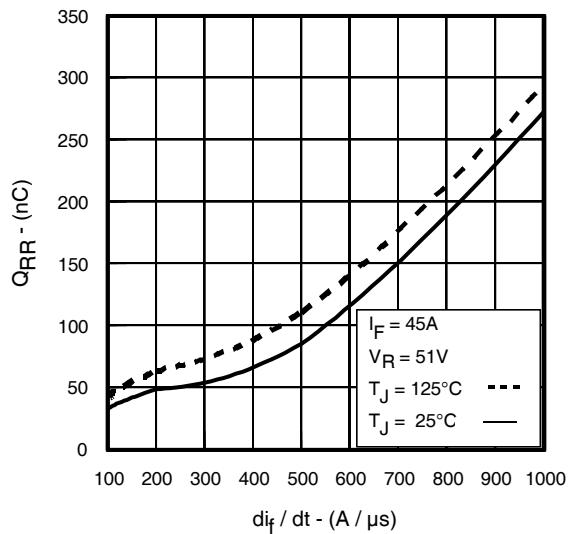


Fig. 20 - Typical Stored Charge vs. di_f/dt

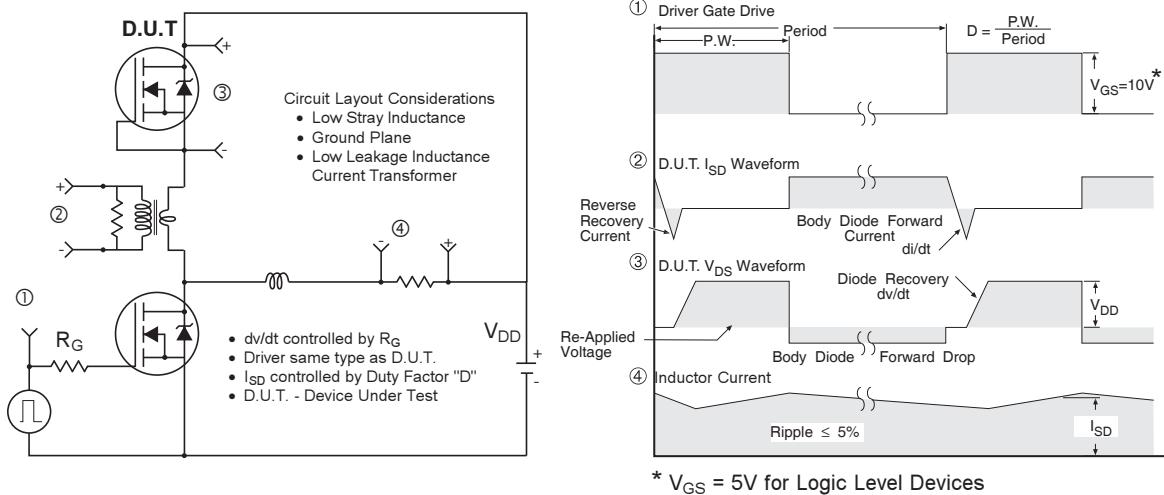


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

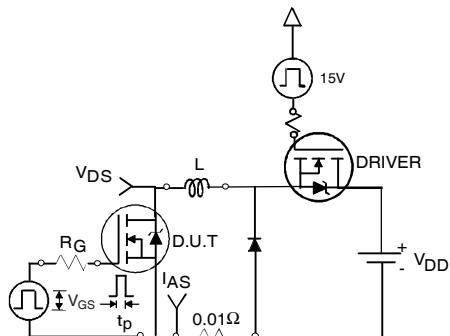


Fig 22a. Unclamped Inductive Test Circuit

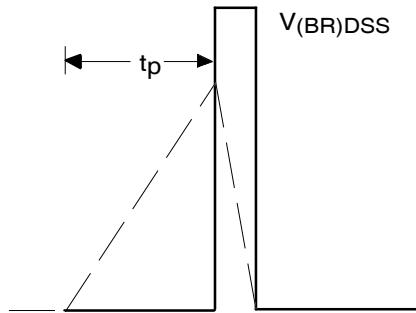


Fig 22b. Unclamped Inductive Waveforms

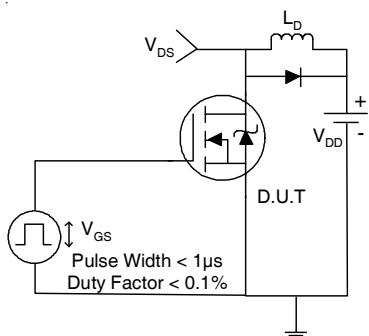


Fig 23a. Switching Time Test Circuit

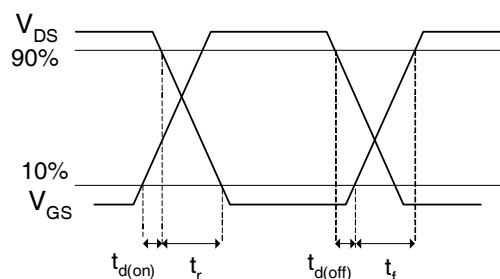


Fig 23b. Switching Time Waveforms

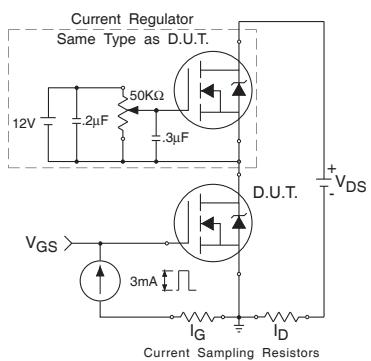


Fig 24a. Gate Charge Test Circuit

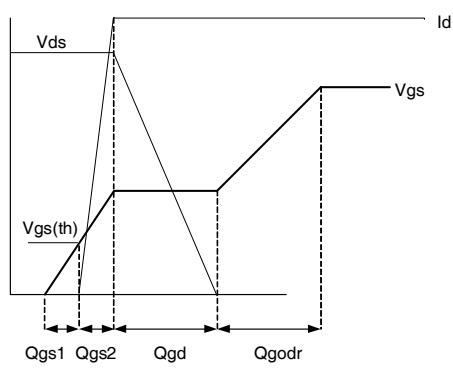
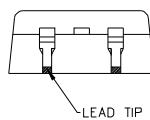
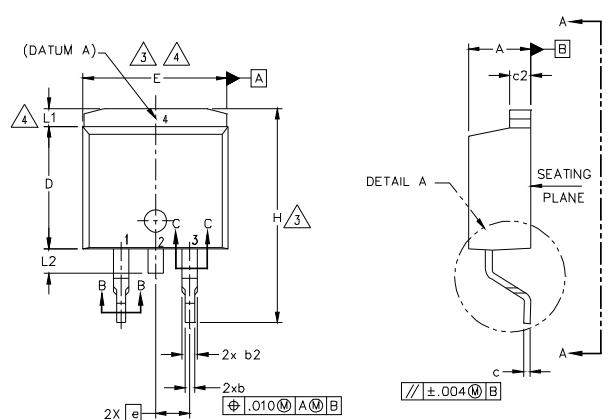


Fig 24b. Gate Charge Waveform

D²Pak Package Outline (Dimensions are shown in millimeters (inches))



S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	0.00	0.254	.000	.010		
b	0.51	0.99	.020	.039	5	
b1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068		
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	—	.270	—	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	—	.245	—	4	
e	2.54	BSC	.100	BSC		
H	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
L1	—	1.65	—	.066		
L2	1.27	1.78	—	.070		
L3	0.25	BSC	.010	BSC		
L4	4.78	5.28	.188	.208		

LEAD ASSIGNMENTS

DIODES

1. - ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4. - CATHODE
3. - ANODE

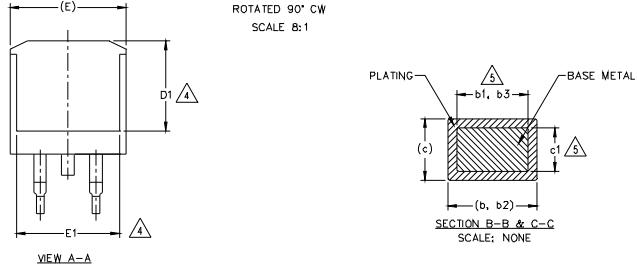
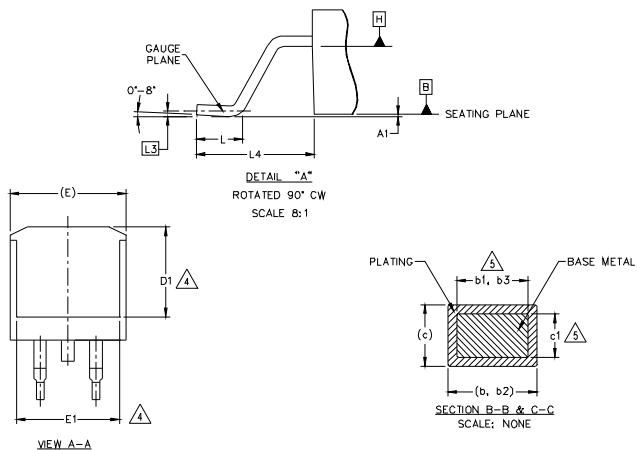
HEXFET

IGBTs, CoPACK

1. - GATE
2, 4. - DRAIN
3. - SOURCE

1. - GATE

2, 4. - COLLECTOR
3. - Emitter



D²Pak Part Marking Information

Part Number

AUFS3306

IR Logo

IR YWWA

Date Code

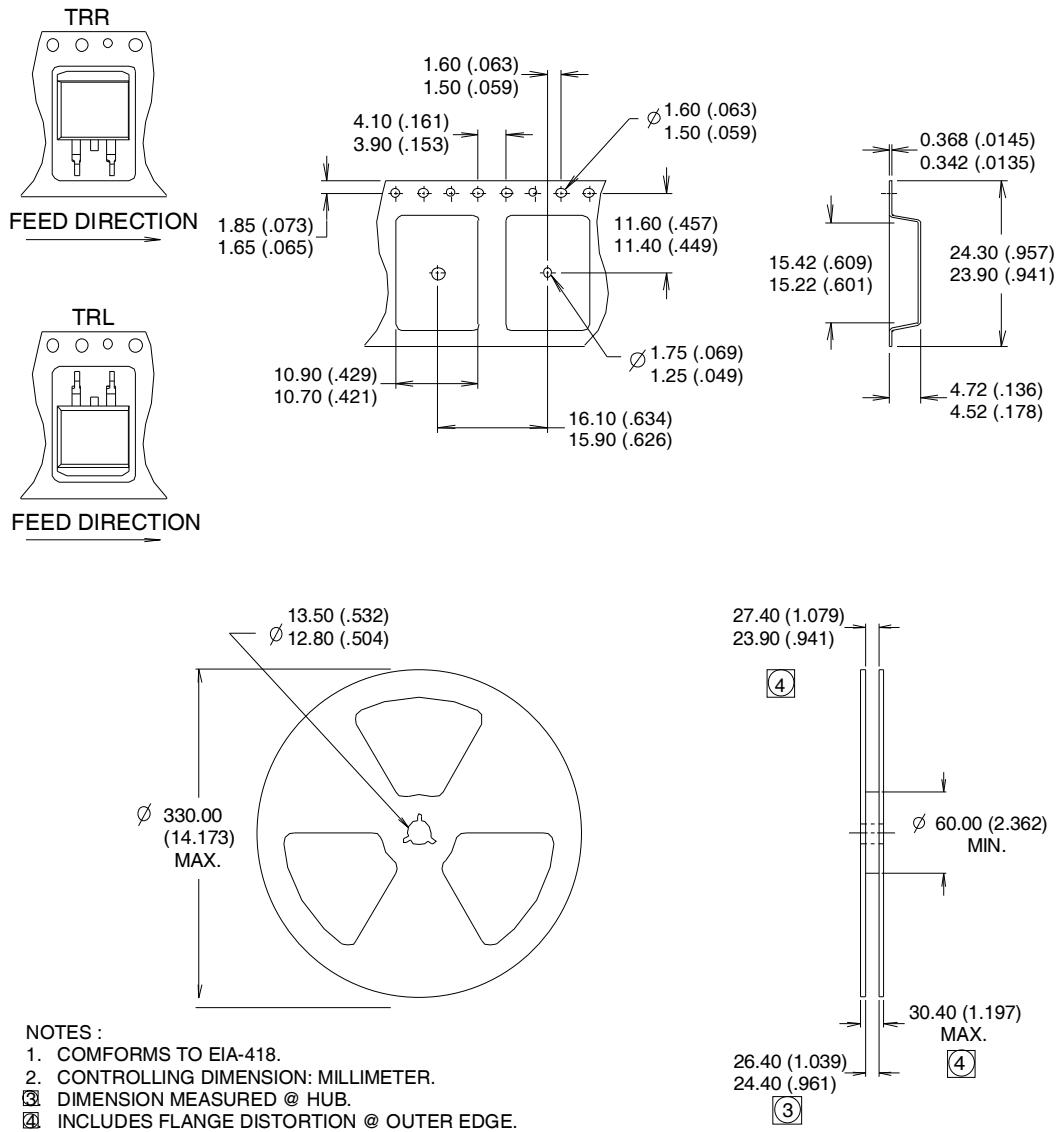
Y= Year

WW= Work Week

A= Automotive, Lead Free

Lot Code

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

D²Pak Tape & Reel Information

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFS3306	D2Pak	Tube	50	AUIRFS3306
		Tape and Reel Left	800	AUIRFS3306TRL
		Tape and Reel Right	800	AUIRFS3306TRR

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For technical support, please contact IR's Technical Assistance Center
<http://www.irf.com/technical-info/>

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