CY62187EV30, MoBL®

64 Mbit (4M x 16) Static RAM

Features

- Very High Speed
  - 55 ns
- Wide Voltage Range
  - 2.2V to 3.7V
- Ultra Low Standby Power
  - Typical Standby Current: 8 µA
  - Maximum Standby Current: 48 µA
- Ultra Low Active Power
  - Typical Active Current: 4.0 mA at f = 1 MHz
- Easy Memory Expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-Free 48-Ball FBGA Package

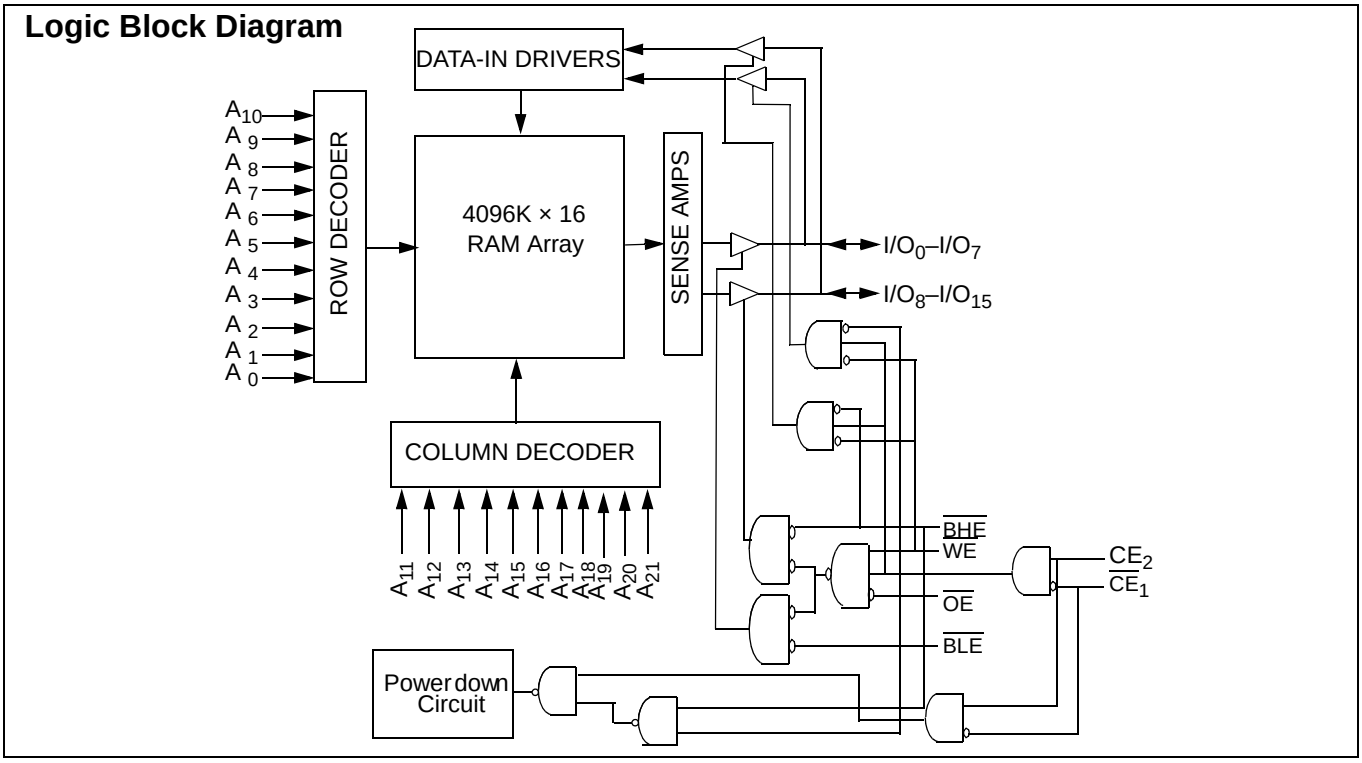
Functional Description

The CY62187EV30 is a high performance CMOS static RAM organized as 4M words by 16 bits[1]. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (IO_0 through IO_{15}) are placed in a high impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{21}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{21}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the Truth Table on page 9 for a complete description of read and write modes.

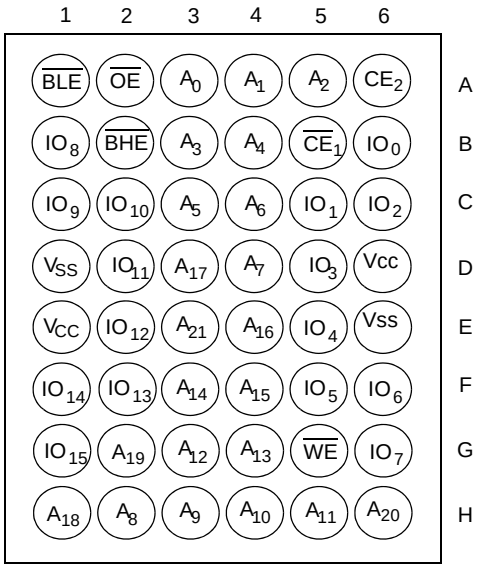
Logic Block Diagram



Note
1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configuration

Figure 1. 48-Ball VFBGA



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62187EV30LL	2.2	3.0	3.7	55	4.0	9	45	55	8	48

Note
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High Z State [3, 4]..... –0.3V to $V_{CC\ (max)}$ + 0.3V

DC Input Voltage [3, 4]..... –0.3V to $V_{CC\ (max)}$ + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62187EV30LL	Industrial	–40°C to +85°C	2.2V to 3.7V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ[2]	Max	
V_{OH}	Output HIGH Voltage	2.2V ≤ V_{CC} ≤ 2.7V	I_{OH} = –0.1 mA	2.0			V
		2.7V ≤ V_{CC} ≤ 3.7V	I_{OH} = –1.0 mA	2.4			V
V_{OL}	Output LOW Voltage	2.2V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.1 mA			0.4	V
		2.7V ≤ V_{CC} ≤ 3.7V	I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage	2.2V ≤ V_{CC} ≤ 2.7V		1.8		V_{CC} + 0.3V	V
		2.7V ≤ V_{CC} ≤ 3.7V		2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	2.2V≤ V_{CC} ≤ 2.7V		–0.3		0.6	V
		2.7V ≤ V_{CC} ≤ 3.7V		–0.3		0.7	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{Max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels		45	55	mA
		f = 1 MHz			7.5	9	mA
I_{SB2} [6]	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.7V			8	48	µA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	25	pF
C_{OUT}	Output Capacitance		35	pF

Notes

3. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Only chip enables ($\overline{CE_1}$ and CE_2) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	59.06	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		14.08	°C/W

Figure 2. AC Test Loads and Waveforms

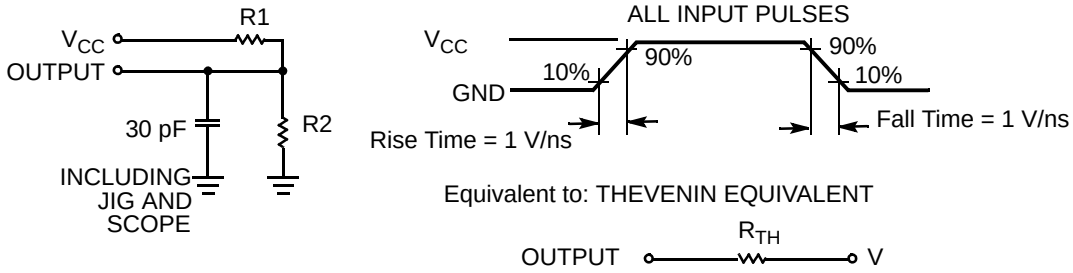


Table 1. AC Test Loads

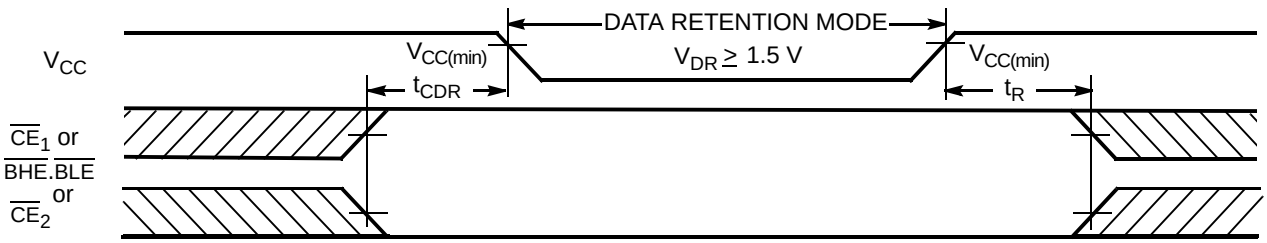
Parameter		2.2V to 3.7V	Unit
R1		1103	Ω
R2		1554	Ω
R_{TH}		645	Ω
V_{TH}	2.2V < V_{CC} ≤ 3V	V_{CC}/2	V
	3V < V_{CC} ≤ 3.7V	1.5	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[2]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR} [6]	Data Retention Current	V_{CC}= 1.5V, $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			48	µA
t_{CDR} [7]	Chip Deselect to Data Retention Time		0			ns
t_R [8]	Operation Recovery Time		t_{RC}			ns

Figure 3. Data Retention Waveform [9]



Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
9. BHE.BLE is the AND of both BHE and BLE. Chip is deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics

Over the Operating Range [10]

Parameter	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid		55	ns
t_{OHA}	Data Hold from Address Change	6		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[11]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[11, 12]		20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power Down		55	ns
t_{DBE}	BLE/$\overline{BHE}$ LOW to Data Valid		55	ns
t_{LZBE}	BLE/$\overline{BHE}$ LOW to Low Z [11]	10		ns
t_{HZBE}	BLE/$\overline{BHE}$ HIGH to HIGH Z [11, 12]		20	ns
Write Cycle[13]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	45		ns
t_{AW}	Address Setup to Write End	45		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		ns
t_{BW}	BLE/$\overline{BHE}$ LOW to Write End	45		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	10		ns

Notes

10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns, timing reference levels of V_{TH}, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads on page 4.
11. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
13. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled)[14, 15]

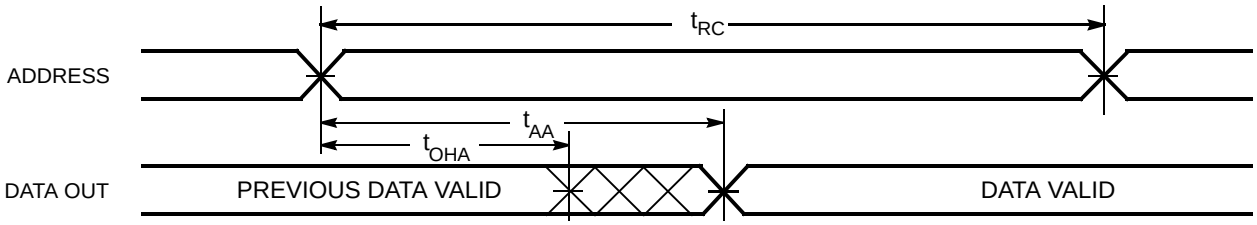
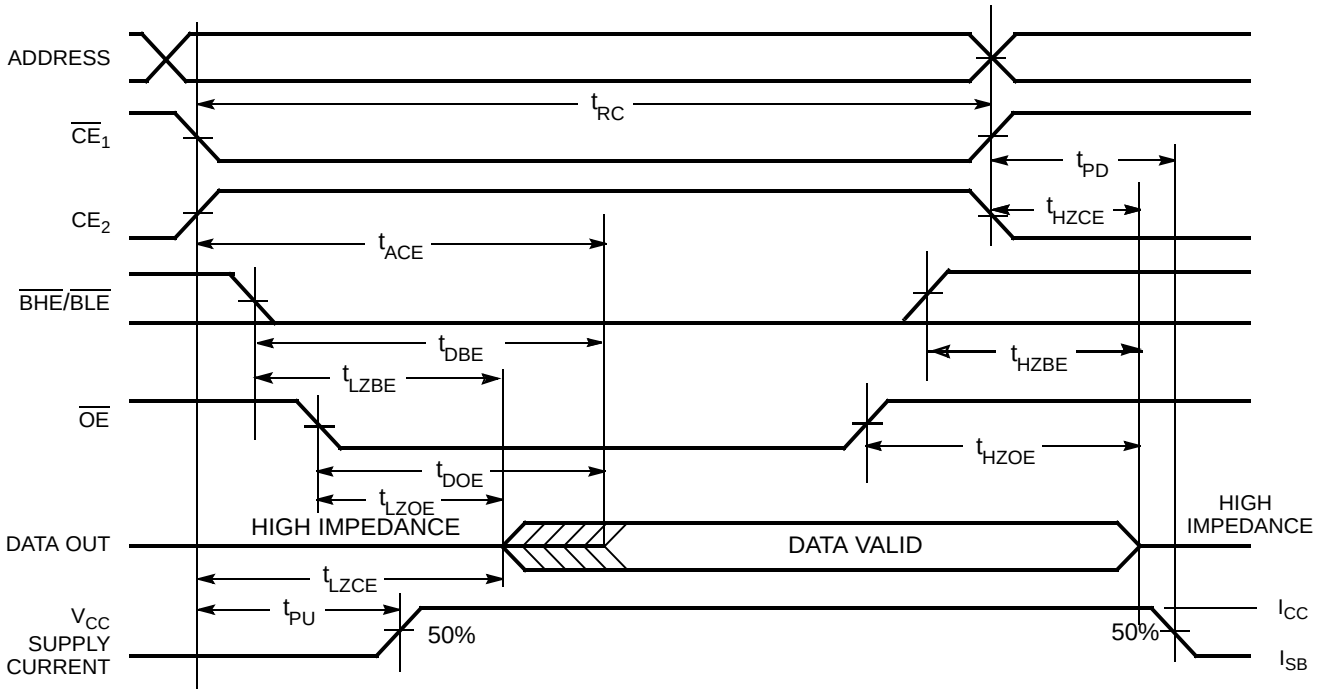


Figure 5. Read Cycle 2 ($\overline{OE}$ Controlled)[15, 16]



Notes
14. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 ($\overline{WE}$ Controlled) [13, 17, 18, 19]

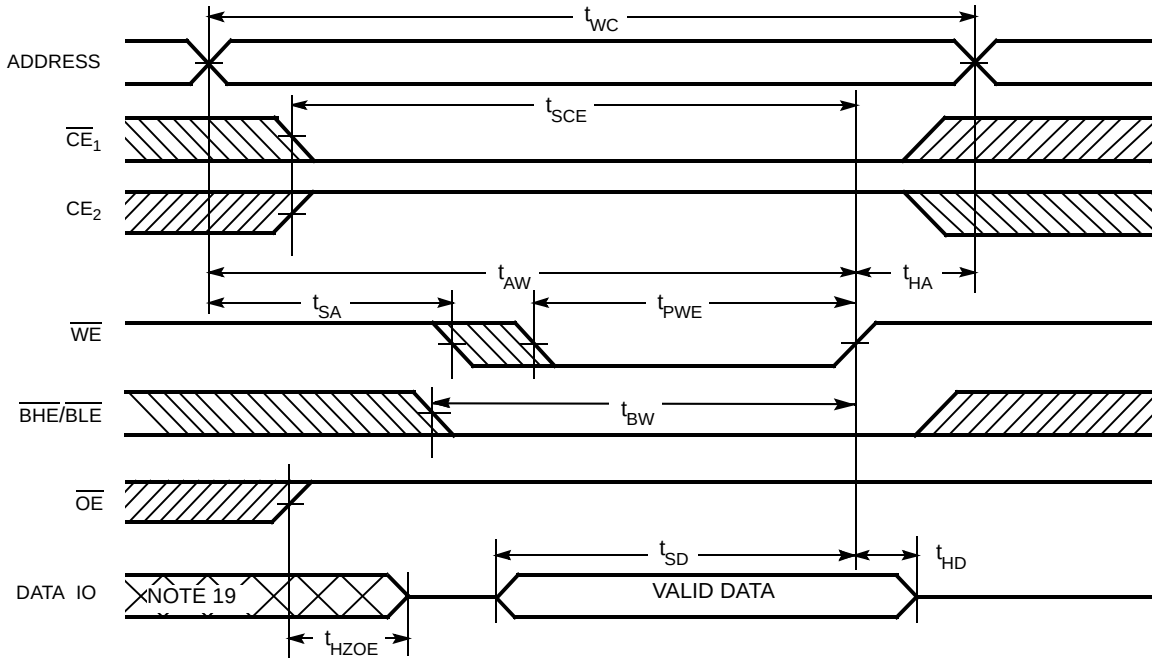
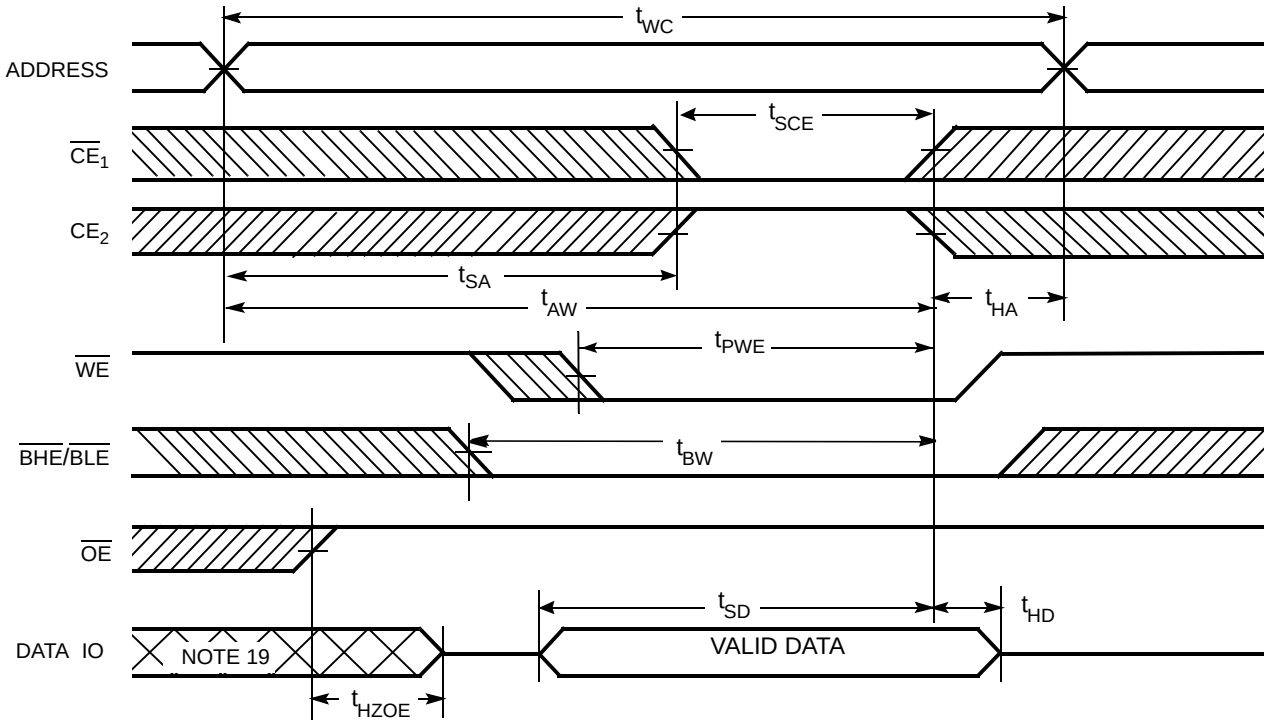


Figure 7. Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled) [13, 17, 18, 19]



Notes
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
19. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[18, 19]

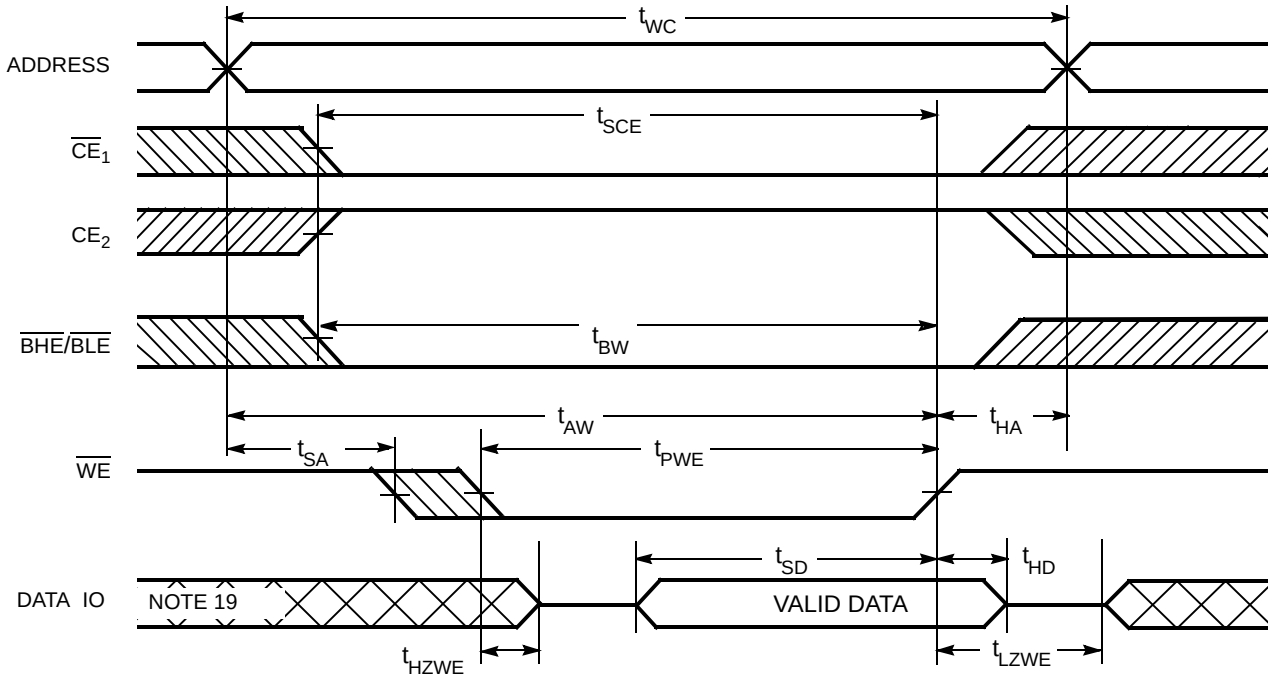
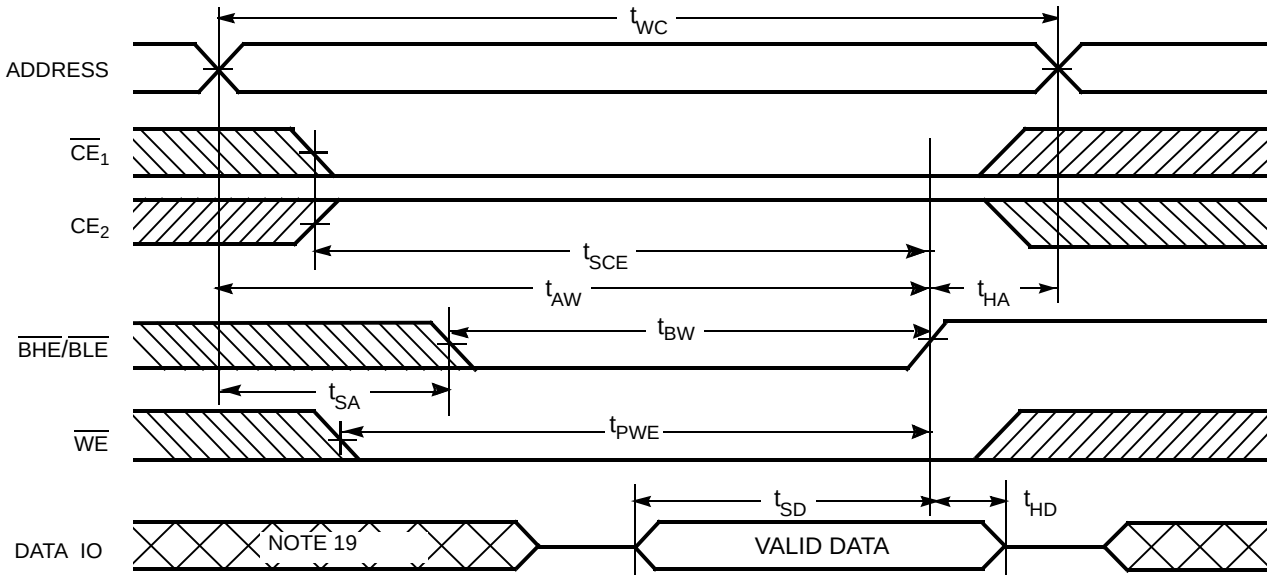


Figure 9. Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[18,19]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X[20]	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X[20]	L	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X[20]	X[20]	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (IO_0–IO_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (IO_8–IO_{15}): Data Out (IO_0–IO_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (IO_8–IO_{15}); High Z (IO_0–IO_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (IO_0–IO_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (IO_8–IO_{15}); Data In (IO_0–IO_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (IO_8–IO_{15}); High Z (IO_0–IO_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

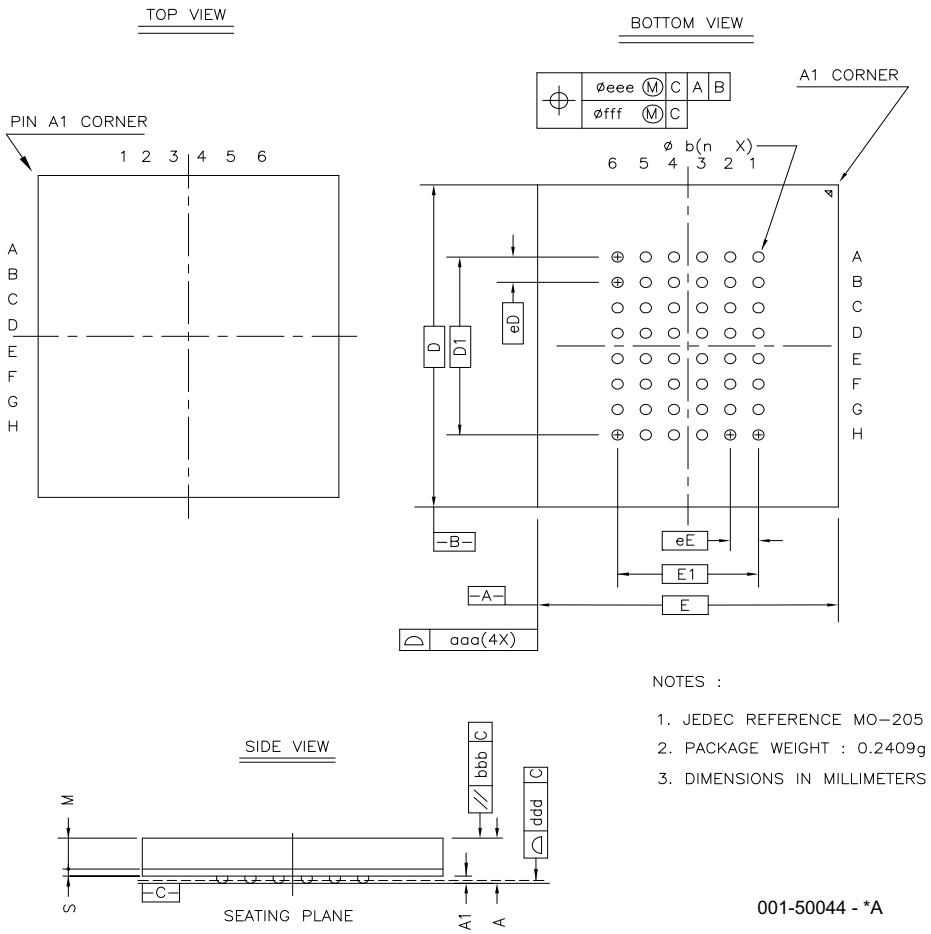
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62187EV30LL-55BAXI	001-50044	48-Ball Fine Pitch Ball Grid Array (8 x 9.5 x 1.4 mm) Pb-Free	Industrial

Note
20. The ‘X’ (Don’t care) state for the chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Package Diagrams

Figure 10. 48-Ball FBGA (8 x 9.5 x 1.4 mm)



		Symbol	Common Dimensions
Package :			FBGA
Body Size:	X	E	8.00
	Y	D	9.50
Ball Pitch :	X	eE	0.75
	Y	eD	0.75
Total Thickness :		A	1.45 +/− 0.05
Mold Thickness :		M	0.910 Ref.
Substrate Thickness :		S	0.21 Ref.
Ball Diameter :			0.30
Stand Off :		A1	0.16−0.26
Ball Width :		b	0.27−0.37
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	48
Edge Ball Center to Center :	X	E1	3.750
	Y	D1	5.250

NOTES :

1. JEDEC REFERENCE MO−205
2. PACKAGE WEIGHT : 0.2409g
3. DIMENSIONS IN MILLIMETERS

001-50044 - *A

Document History Page

Document Title: CY62187EV30 MoBL® 64 Mbit (4M x 16) Static RAM Document Number: 001-48998				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2595932	VKN/PYRS	10/24/08	New Datasheet
*A	2644442	VKN/PYRS	01/23/09	Updated the Package diagram on page 10
*B	2672650	VKN/PYRS	03/12/09	Extended the V_{CC} range to 3.7V Added 55 ns speed bin and it's related information Changed $I_{CC\ (typ)}$ from 2.5 mA to 3.5 mA at f = 1 MHz Changed $I_{CC\ (max)}$ from 4 mA to 6 mA at f = 1 MHz For 70 ns speed, changed $I_{CC\ (typ)}$ form 33 mA to 28 mA at f = f_{MAX} For 70 ns speed, changed $I_{CC\ (max)}$ from 40 mA to 45 mA at f = f_{MAX} For 70 ns speed, changed t_{PWE} from 45 to 50 ns, t_{SD} from 30 to 35 ns Modified footnote #6 Changed 48-Ball FBGA package dimensions from 8 x 9.5 x 1.6 mm to 8 x 9.5 x 1.4 mm and updated package diagram on page 10
*C	2737164	VKN/AESA	07/13/09	Converted from preliminary to final Changed $I_{CC(typ)}$ from 3.5 mA to 4 mA at f = 1 MHz Changed $I_{CC(typ)}$ from 35 mA to 45 mA and from 28 mA to 35 mA for the speeds 50 ns and 70 ns respectively at f = f_{max} Included V_{CC} range in the test condition of the "Electrical Characteristics" table for the specs V_{OH}, V_{OL}, V_{IH}, V_{IL} Changed $V_{IL(max)}$ from 0.8V to 0.7V for V_{CC} = 2.7V to 3.7V Changed C_{IN} spec from 20 pF to 25 pF and C_{OUT} spec from 20 pF to 35 pF Included thermal specs for 48-FBGA Included V_{CC} range for V_{TH} spec in the AC test load table Changed t_{LZBE} spec from 5 ns to 10 ns Added footnote #20 related to chip enable
*D	2765892	VKN	09/18/09	Removed 70 ns speed For 55 ns speed, at f = 1 MHz, changed $I_{CC\ (max)}$ spec from 6 mA to 9 mA Changed $I_{CC(typ)}$ from 4 mA to 7.5 mA at f = 1 MHz

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