

OPA627
OPA637

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: $4.5\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
- FAST SETTLING TIME:
OPA627—550ns to 0.01%
OPA637—450ns to 0.01%
- LOW V_{OS} : 100 μV max
- LOW DRIFT: 0.8 $\mu\text{V}/^\circ\text{C}$ max
- LOW I_B : 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

DESCRIPTION

The OPA627 and OPA637 *Difet* operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage— $\pm 4.5\text{V}$ to $\pm 18\text{V}$. Laser-trimmed *Difet* input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

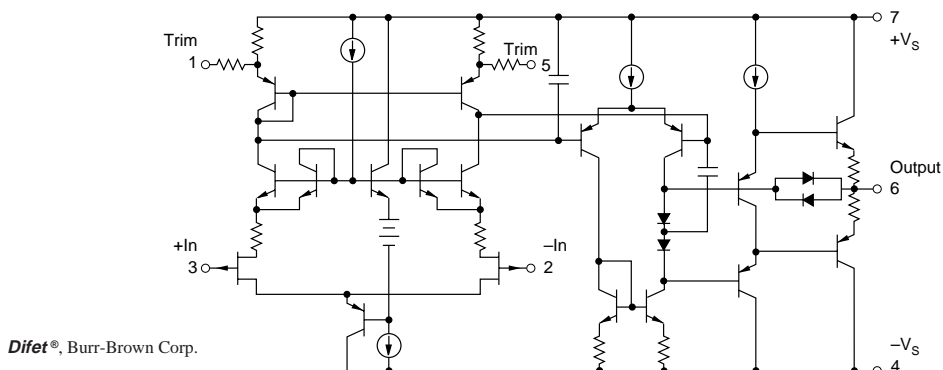
APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



Difet®, Burr-Brown Corp.

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^{\circ}\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA627BM, BP, SM OPA637BM, BP, SM			OPA627AM, AP, AU OPA637AM, AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE ⁽¹⁾ Input Offset Voltage AP, BP, AU Grades Average Drift AP, BP, AU Grades Power Supply Rejection	$V_S = \pm 4.5$ to $\pm 18\text{V}$		40 100 0.4 0.8 120	100 250 0.8 2	100	130 280 1.2 2.5 116	250 500 2	μV μV $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/^{\circ}\text{C}$ dB
INPUT BIAS CURRENT ⁽²⁾ Input Bias Current Over Specified Temperature SM Grade Over Common-Mode Voltage Input Offset Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$ $V_{CM} = \pm 10\text{V}$ $V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		1 1 50 1 0.5 1 50	5 1 50 5 1 50		2 2 2 1 10 2	10 2	pA nA nA pA pA nA nA
NOISE Input Voltage Noise Noise Density: $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Voltage Noise, BW = 0.1Hz to 10Hz Input Bias Current Noise Noise Density, $f = 100\text{Hz}$ Current Noise, BW = 0.1Hz to 10Hz			15 8 5.2 4.5 0.6	40 20 8 6 1.6		20 10 5.6 4.8 0.8		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ $\text{fA}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 8$ $10^{13} \parallel 7$			* *		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	$V_{CM} = \pm 10.5\text{V}$	± 11 ± 10.5 106	± 11.5 ± 11 116		* * 100	* * 110		V V dB
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature SM Grade	$V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$	112 106 100	120 117 114		106 100	116 110		dB dB dB
FREQUENCY RESPONSE Slew Rate: OPA627 OPA637 Settling Time: OPA627 0.01% 0.1% OPA637 0.01% 0.1% Gain-Bandwidth Product: OPA627 OPA637 Total Harmonic Distortion + Noise	$G = -1$, 10V Step $G = -4$, 10V Step $G = -1$, 10V Step $G = -1$, 10V Step $G = -4$, 10V Step $G = -4$, 10V Step $G = 1$ $G = 10$ $G = +1$, $f = 1\text{kHz}$	40 100	55 135 550 450 450 300 16 80 0.00003		* * * * * * * * *	* * * * * * * * *		V/ μs V/ μs ns ns ns ns MHz MHz %
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 15 ± 7	± 18 ± 7.5	* *	* *	* *	V V mA
OUTPUT Voltage Output Over Specified Temperature Current Output Short-Circuit Current Output Impedance, Open-Loop	$R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$ 1MHz	± 11.5 ± 11 ± 35	± 12.3 ± 11.5 ± 45 $+70/-55$ 55	± 100	* * * *	* * * *	* *	V mA mA Ω
TEMPERATURE RANGE Specification: AP, BP, AM, BM, AU SM Storage: AM, BM, SM AP, BP, AU θ_{JA} : AM, BM, SM AP, BP AU		-25 -55 -60 -40	200 100 160	+85 +125 +150 +125	* * * *	* * * *	* * *	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$

* Specifications same as "B" grade.

NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at $T_J = +25^{\circ}\text{C}$. See Typical Performance Curves for warmed-up performance.

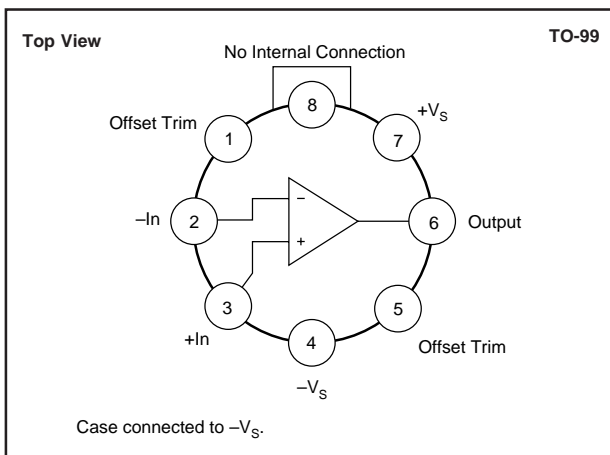
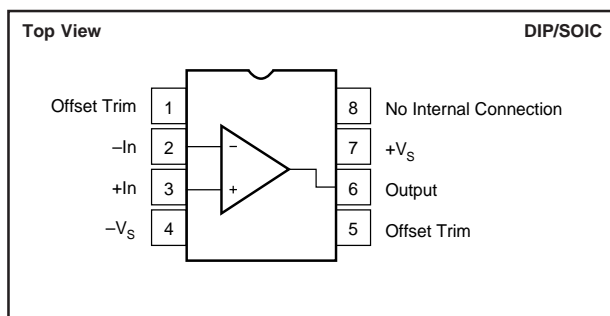
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BURR-BROWN®



OPA627, 637

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	±18V
Input Voltage Range	+V _S + 2V to -V _S - 2V
Differential Input Range	Total V _S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	-55°C to +125°C
P, U Package	-40°C to +125°C
Storage Temperature	
M Package	-65°C to +150°C
P, U Package	-40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
SOIC (soldering, 3s)	+260°C

NOTE: (1) Stresses above these ratings may cause permanent damage.

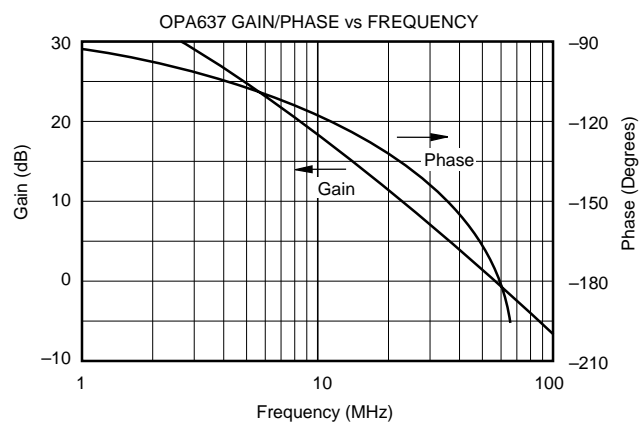
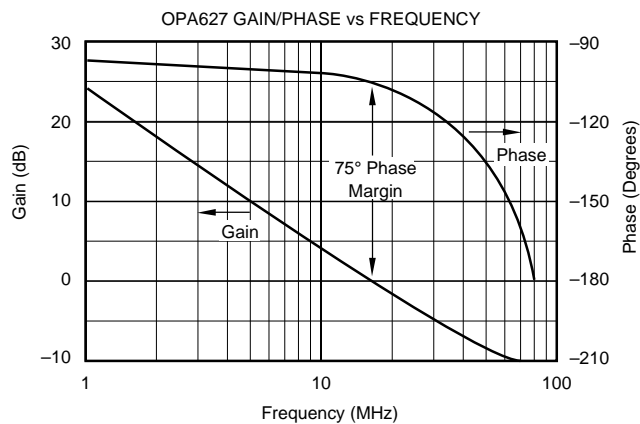
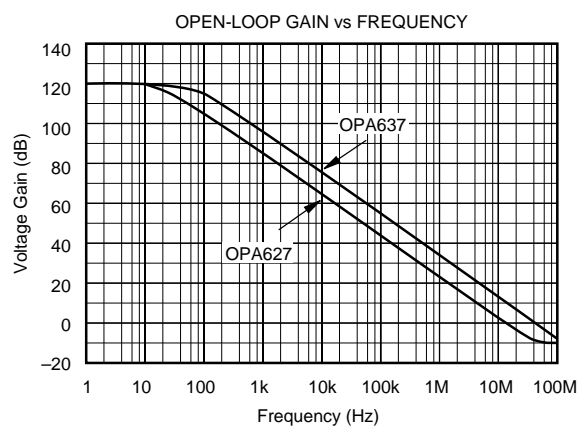
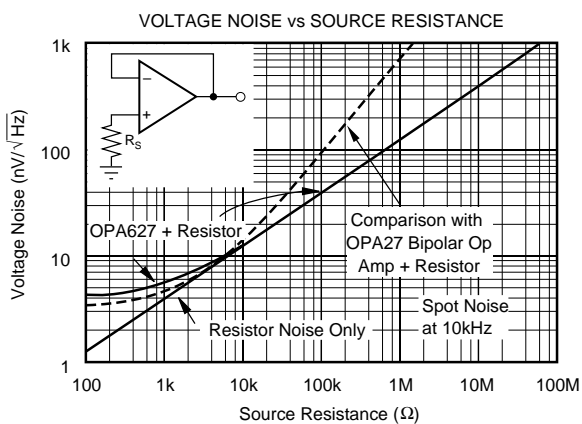
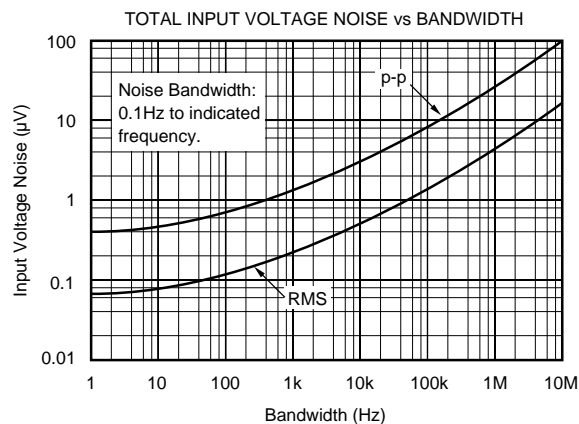
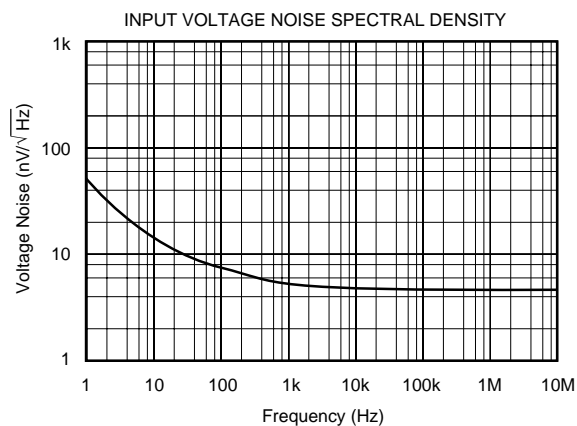
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
OPA627AP	Plastic DIP	006	-25°C to +85°C
OPA627BP	Plastic DIP	006	-25°C to +85°C
OPA627AU	SOIC	182	-25°C to +85°C
OPA627AM	TO-99 Metal	001	-25°C to +85°C
OPA627BM	TO-99 Metal	001	-25°C to +85°C
OPA627SM	TO-99 Metal	001	-55°C to +125°C
OPA637AP	Plastic DIP	006	-25°C to +85°C
OPA637BP	Plastic DIP	006	-25°C to +85°C
OPA637AU	SOIC	182	-25°C to +85°C
OPA637AM	TO-99 Metal	001	-25°C to +85°C
OPA637BM	TO-99 Metal	001	-25°C to +85°C
OPA637SM	TO-99 Metal	001	-55°C to +125°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

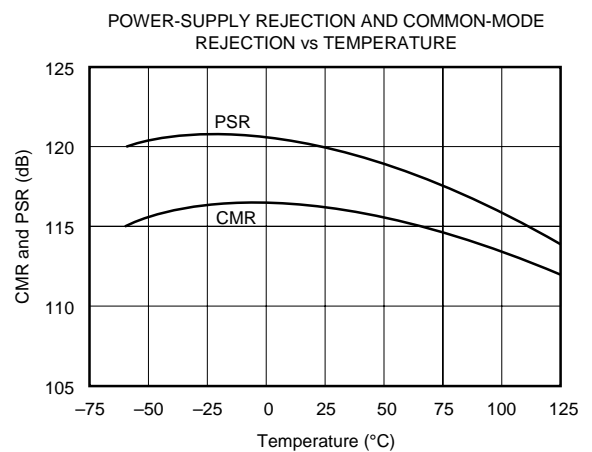
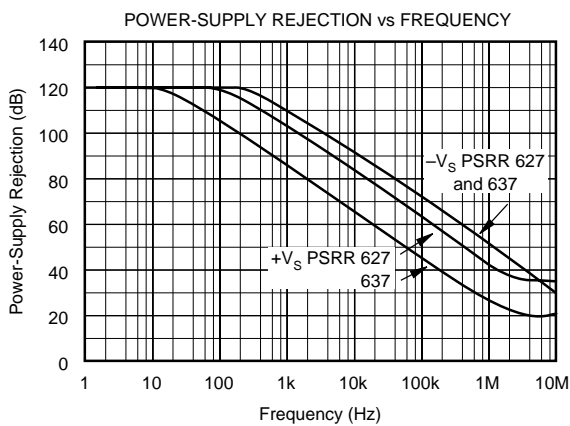
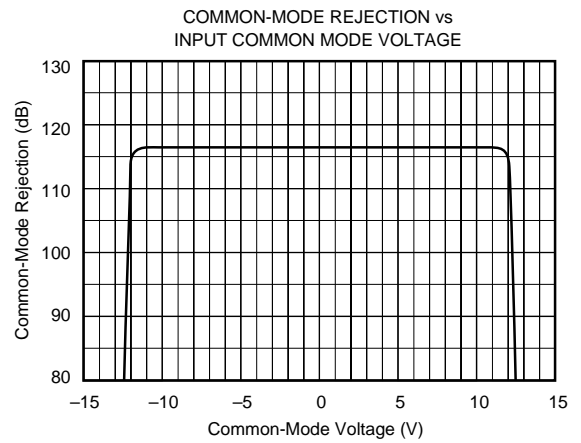
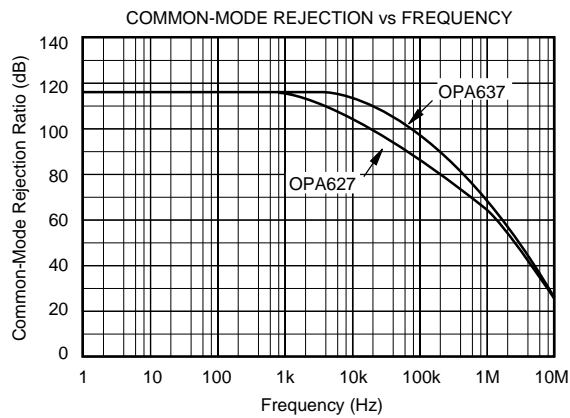
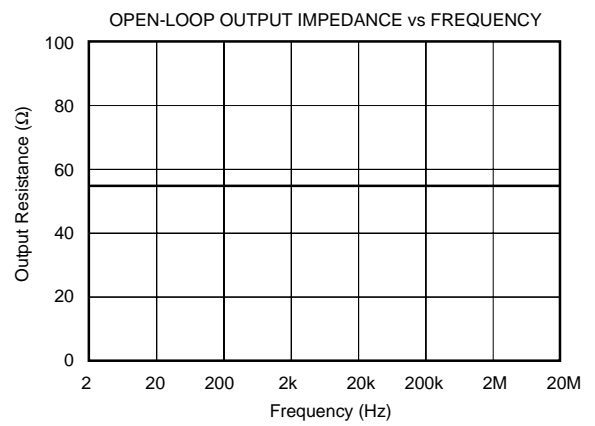
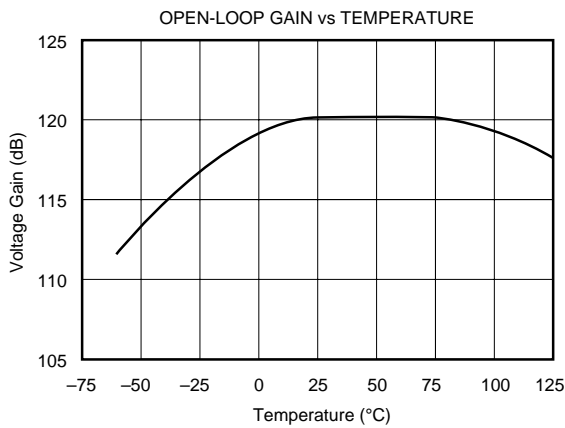
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.



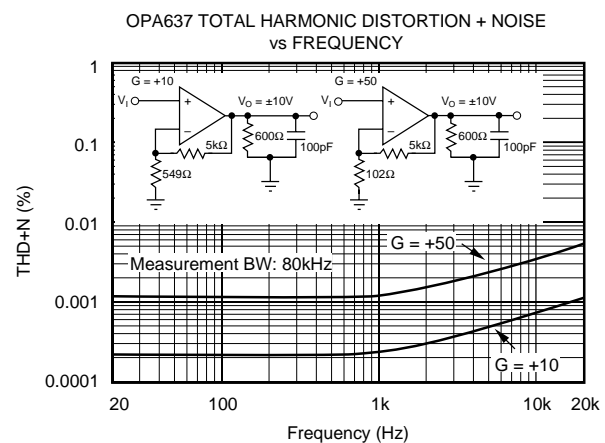
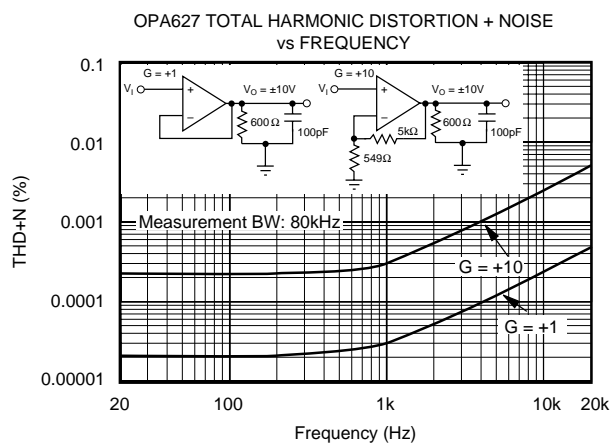
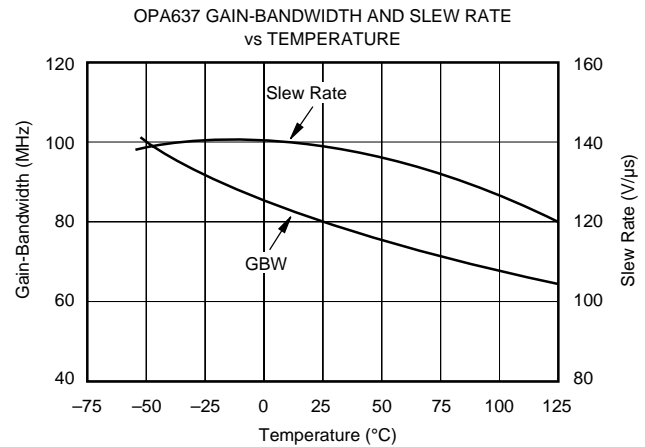
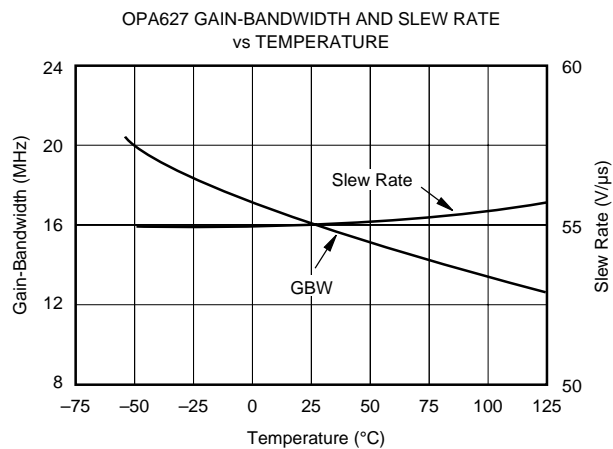
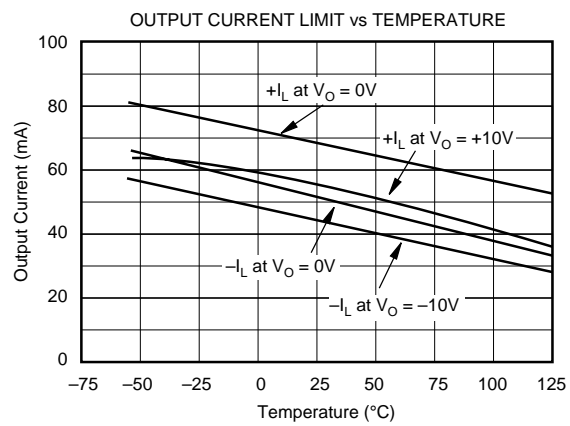
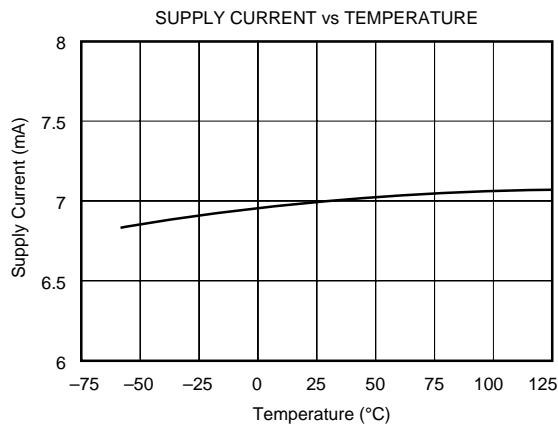
TYPICAL PERFORMANCE CURVES (CONT)

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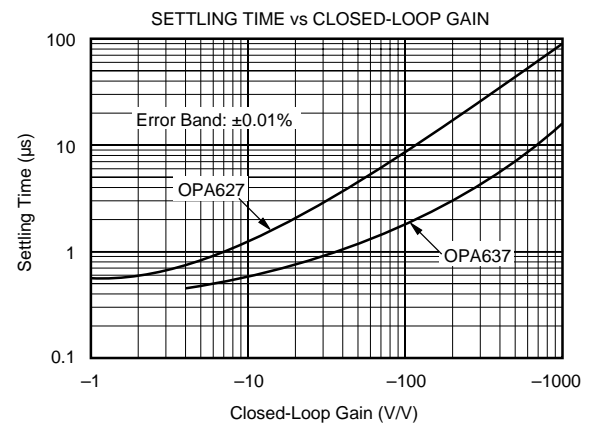
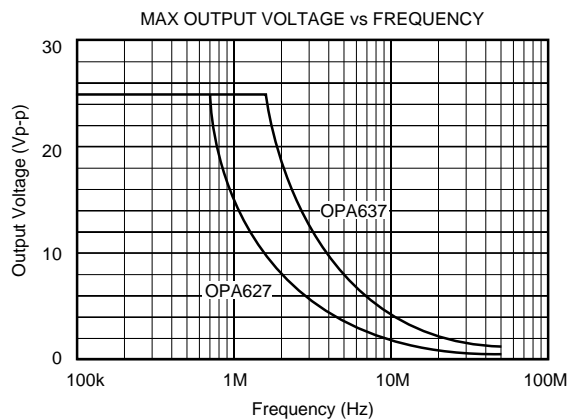
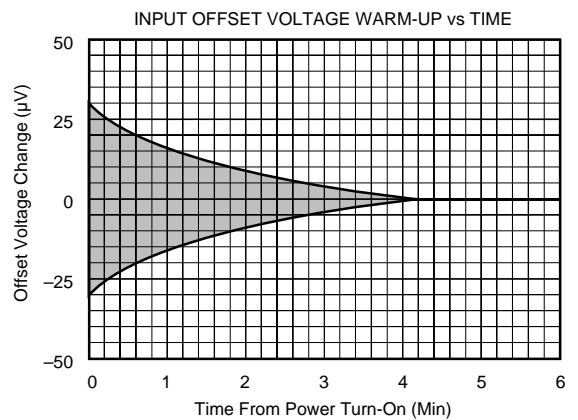
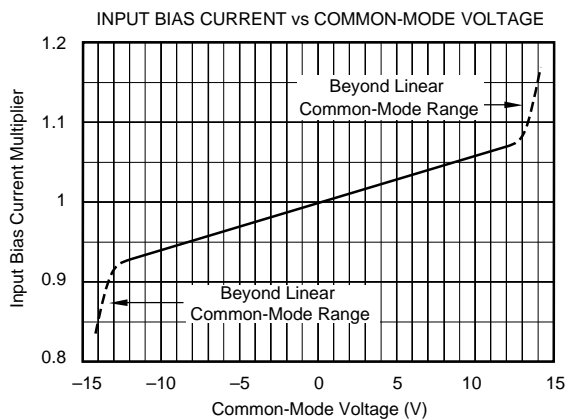
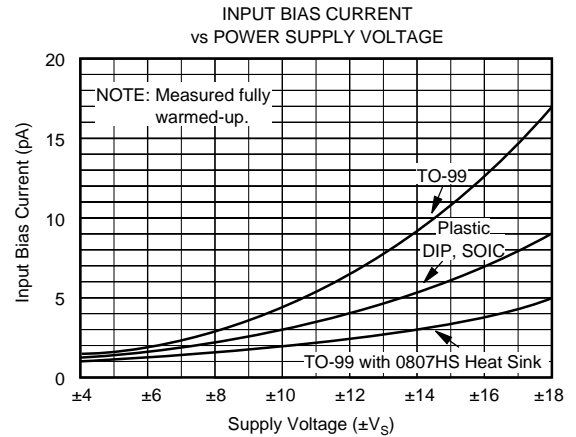
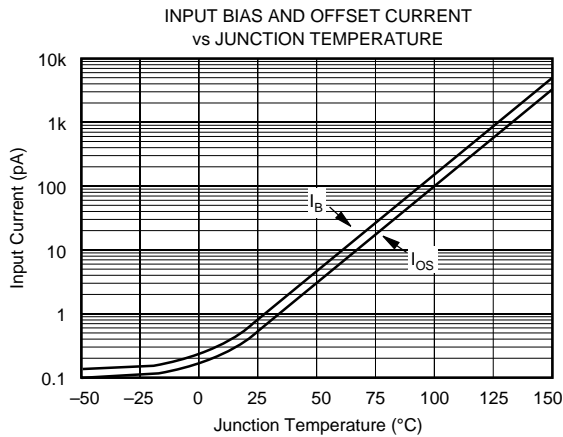
TYPICAL PERFORMANCE CURVES (CONT)

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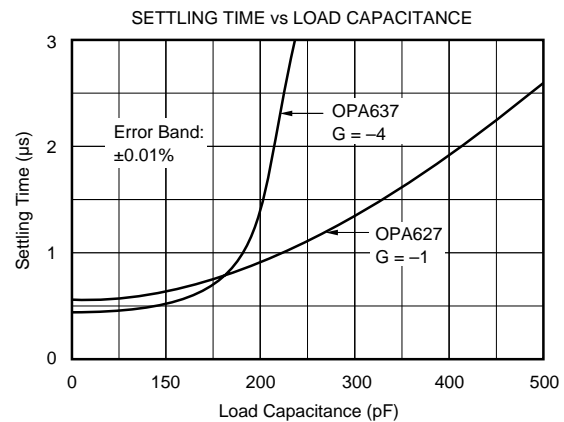
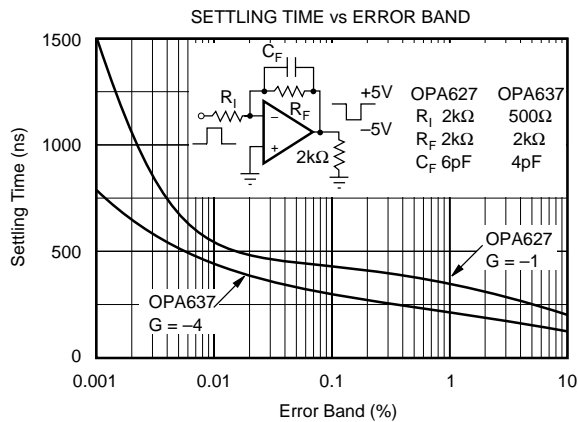
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

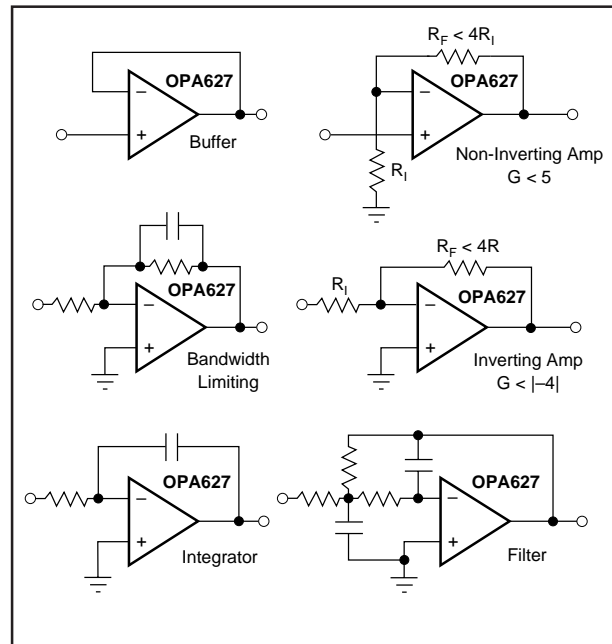


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately $4\mu\text{V}/^\circ\text{C}$ for 1mV of change in the offset voltage due to an offset adjustment (as shown on Figure 3).

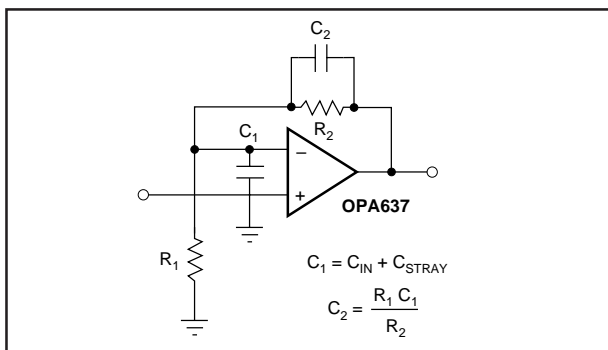


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a $2\text{k}\Omega$ source resistance, the op

amp contributes little additional noise. Below $1\text{k}\Omega$, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case (TO-99 metal package only) is internally connected to the negative power supply as it is with most common op amps. Pin 8 of the plastic DIP, SOIC, and TO-99 packages has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases $0.1\mu\text{F}$ ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as $1\mu\text{F}$ solid tantalum capacitors may improve dynamic performance in these applications.

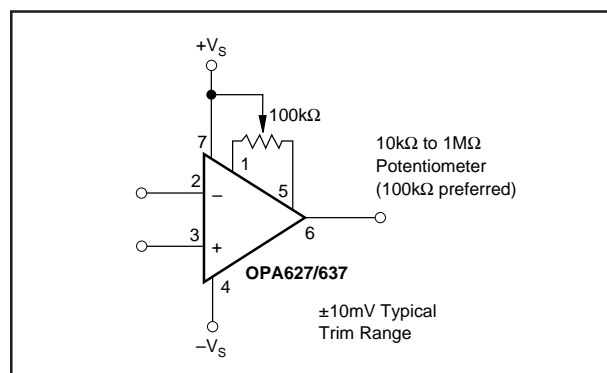


FIGURE 3. Optional Offset Voltage Trim Circuit.

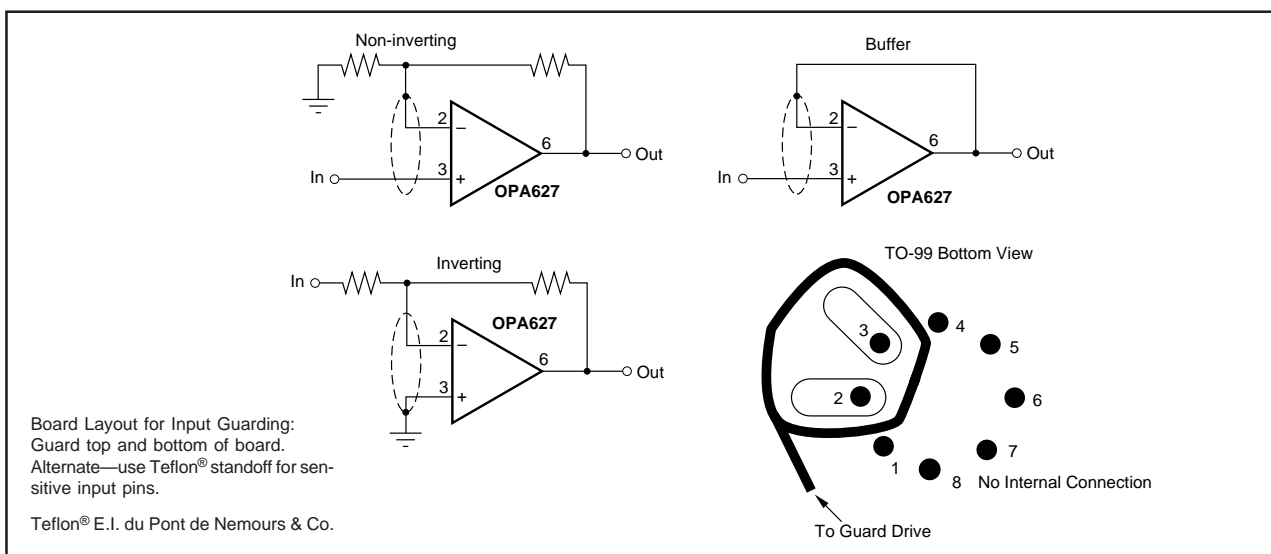


FIGURE 4. Connection of Input Guard for Lowest I_B .

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using $\pm 5V$ power supplies reduces power dissipation to one-third of that at $\pm 15V$. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at $\pm 15V$.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board “guard” pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case (TO-99 metal package only) is internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below $-12V$, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery

takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6 μ s. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

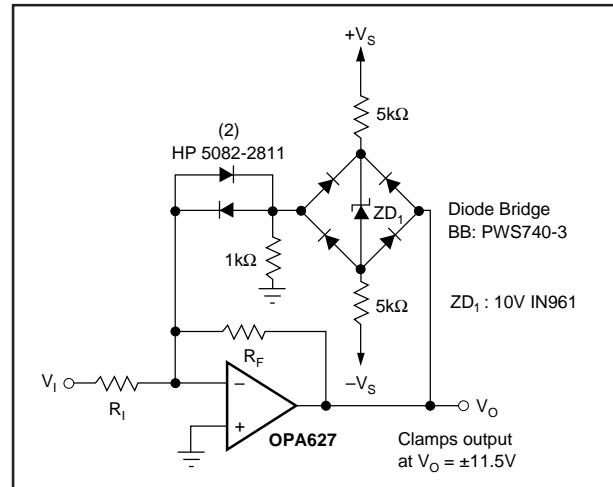


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

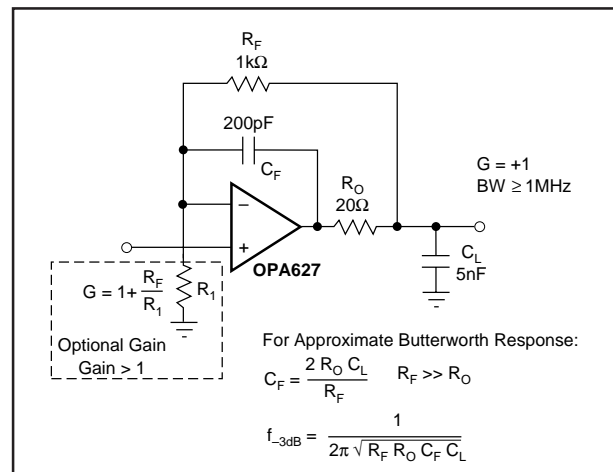


FIGURE 6. Driving Large Capacitive Loads.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_S + 2V$ and $-V_S - 2V$. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S , to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a $1k\Omega$ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately $25nA$ —more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at $1pA$ and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed $2V$ beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

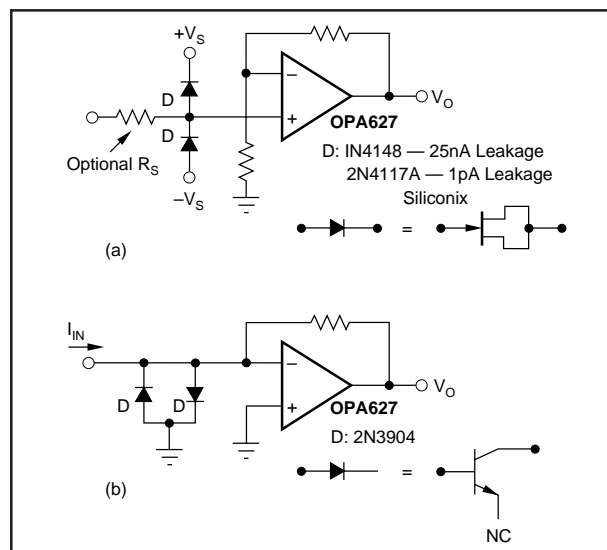


FIGURE 7. Input Protection Circuits.

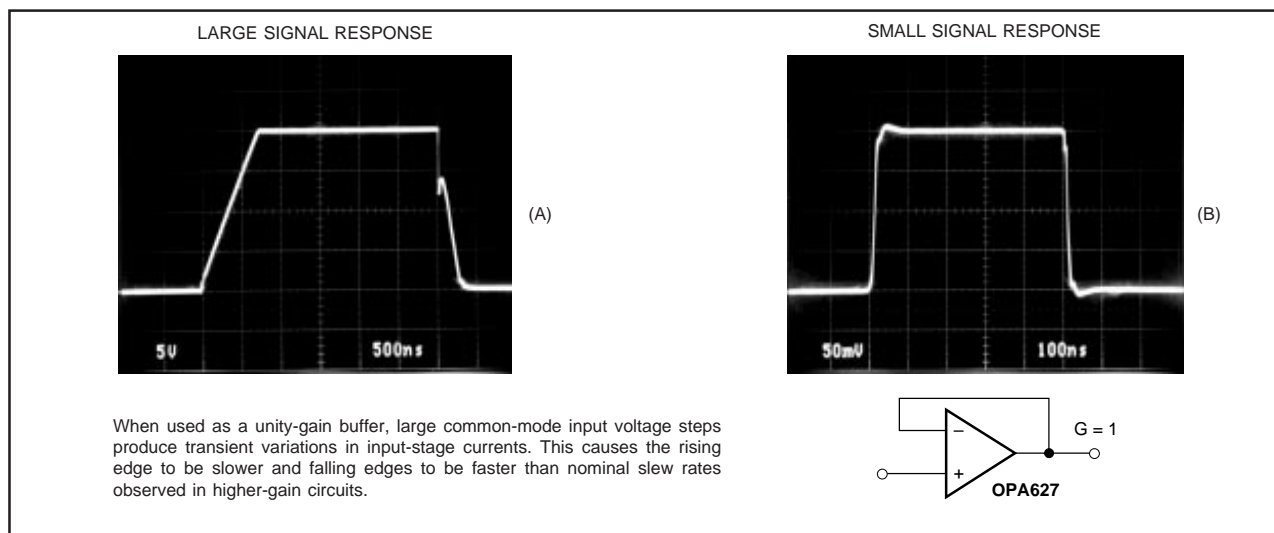


FIGURE 8. OPA627 Dynamic Performance, $G = +1$.

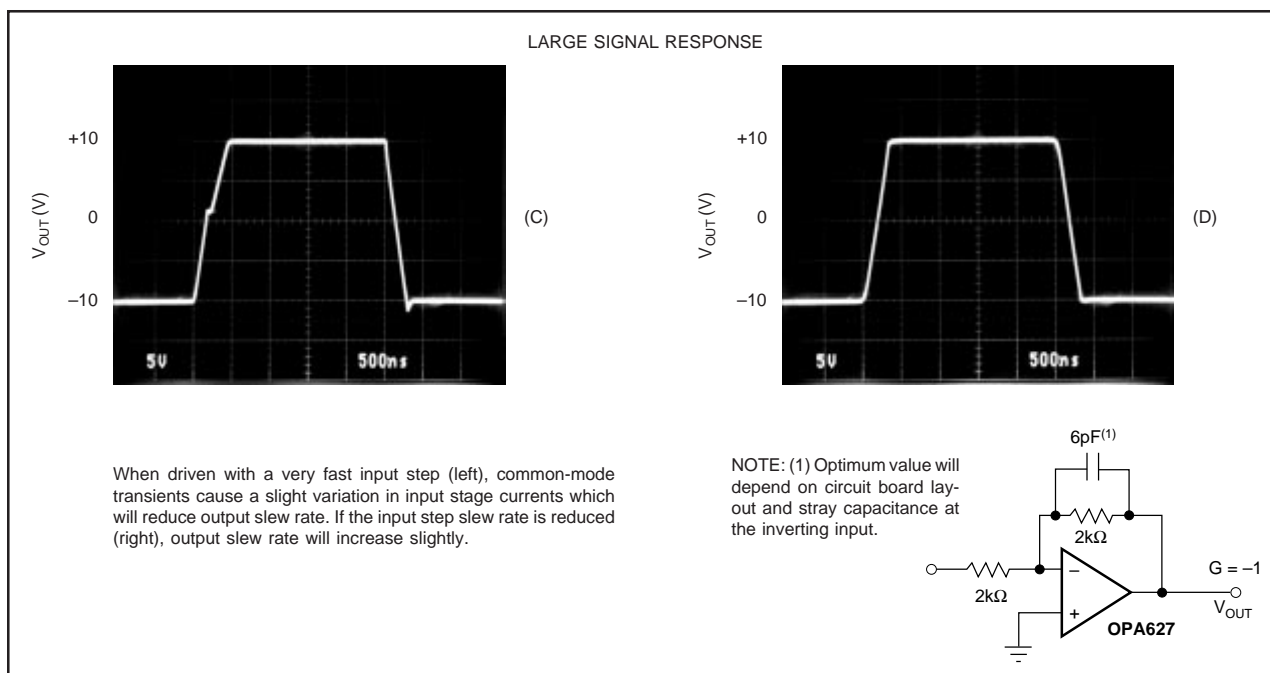


FIGURE 9. OPA627 Dynamic Performance, $G = -1$.

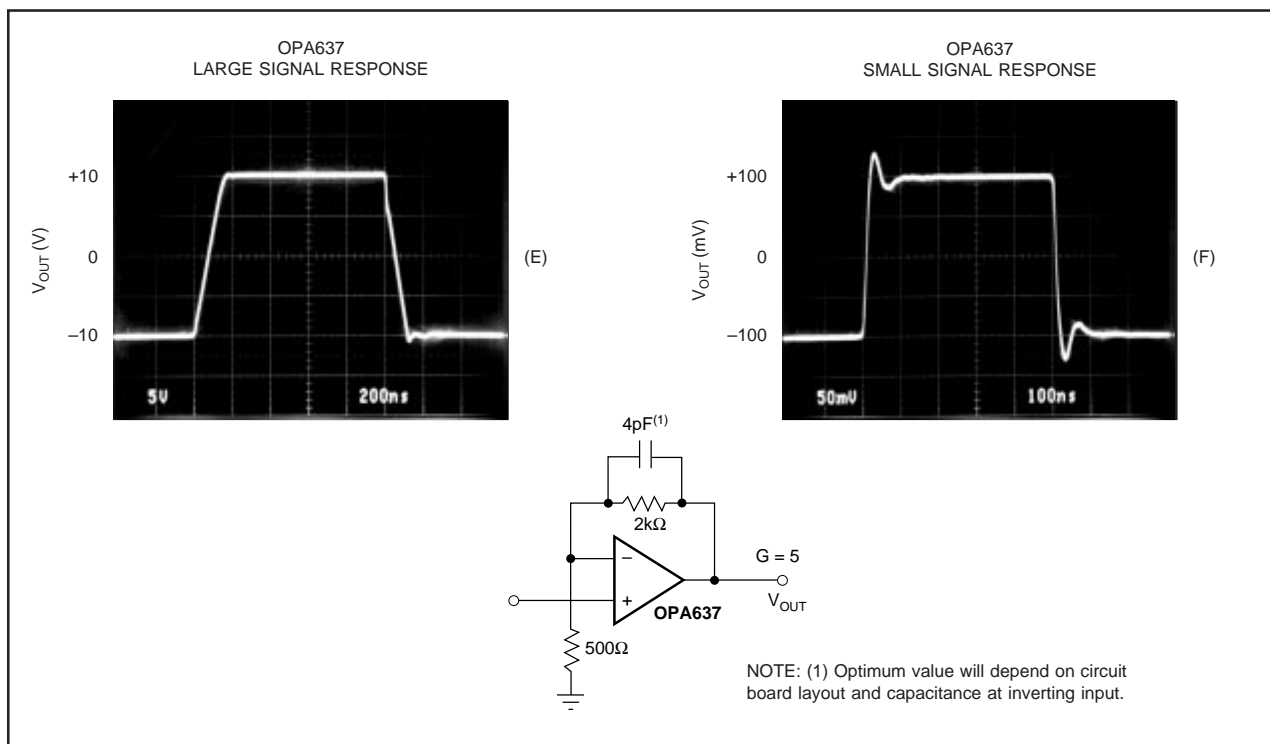


FIGURE 10. OPA637 Dynamic Response, $G = 5$.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA627AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA627AM	
OPA627AP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA627AP	Samples
OPA627APG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA627AP	Samples
OPA627AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU	Samples
OPA627BM	NRND	TO-99	LMC	8	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA627BM	
OPA627BP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA627BP	Samples
OPA627BPG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA627BP	Samples
OPA627SM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA627SM	
OPA637AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA637AM	
OPA637AM2	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI			
OPA637AP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA637AP	Samples
OPA637APG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA637AP	Samples
OPA637AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU	Samples
OPA637AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU	Samples
OPA637AUE4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA637AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU	Samples
OPA637BM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA637BM	
OPA637BM1	OBSOLETE	TO-99	LMC	8		TBD	Call TI	Call TI			
OPA637BP	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA637BP	Samples
OPA637BPG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI		OPA637BP	Samples
OPA637SM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA637SM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA627AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA637AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

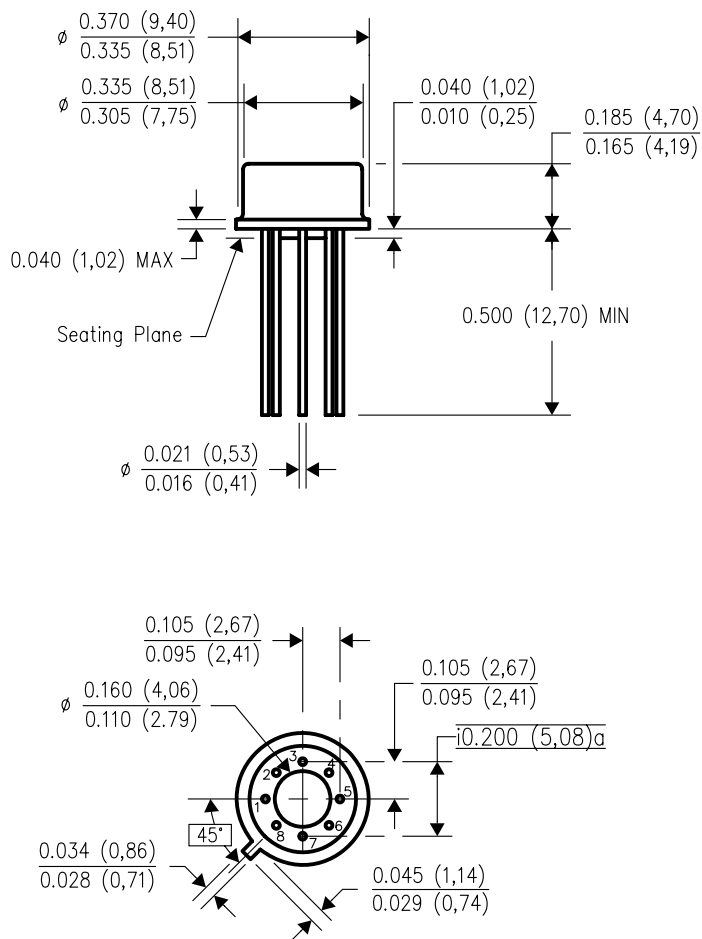


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA627AU/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA637AU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

LMC (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



4202483/B 09/07

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 - Pin numbers shown for reference only. Numbers may not be marked on package.
 - Falls within JEDEC MO-002/T0-99.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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