MSBA8100 Product Brief

Multi-Standard Baseband Accelerator

The MSBA8100 device is an accelerator for Fourier transforms and channel decoding. It is designed to bolster the rapidly changing and expanding wireless markets, such as 3G-LTE, WiMAX and 3GPP-R6.

The MSBA8100 device is the perfect companion for the MSC8144 multicore DSP, and can accelerate tasks such as Turbo decoding, Viterbi decoding, Fast Fourier Transform (FFT), Inverse Fast Fourier Transform (IFFT), Discrete Fourier Transform (DFT), and Inverse Discrete Fourier Transform (IDFT).

Contents

1 Features

The MSBA8100 device targets high-bandwidth highly computational DSP applications and is optimized for 3G-LTE, WiMAX and 3GPP-R6 applications.

1.1 Block Diagram

The MSBA8100 device is an integrated device that contains a multi-accelerator platform engine (MAPLE-B) for Turbo decoding, Viterbi decoding, FFT, IFFT, DFT, and IDFT acceleration; 512 Kbyte of M2 memory; a DDR memory controller; two serial RapidIO® interfaces and a PCI controller.

A block diagram of the MSBA8100 is shown in Figure 1.
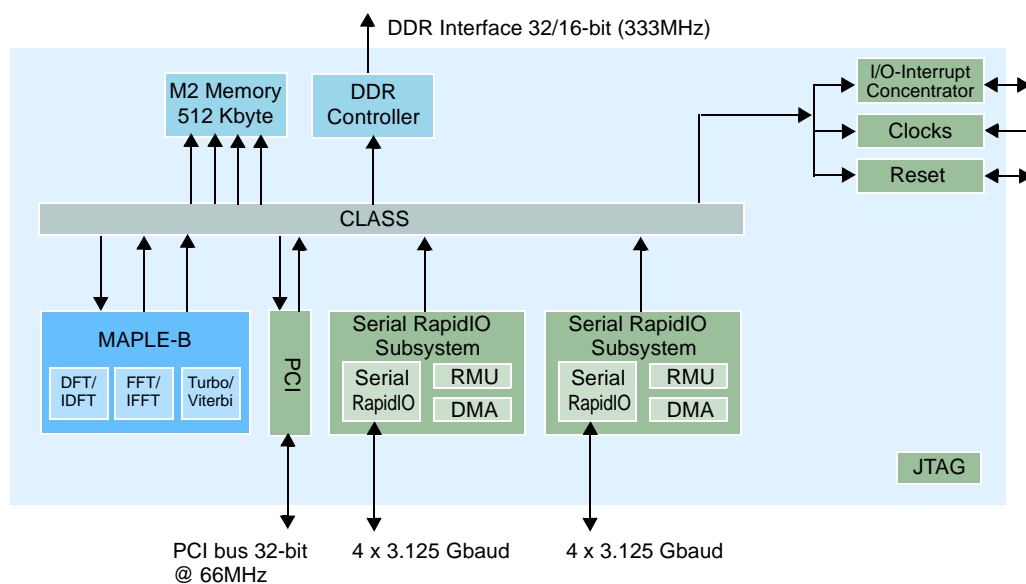
Note: The arrow direction indicates master or slave.

Figure 1. MSBA8100 Block Diagram

1.2 Critical Performance Metrics

- The MAPLE-B contains a highly flexible and programmable Turbo and Viterbi decoder supporting various configurable decoding parameters (for example, polynomials, rate). The MAPLE-B can perform up to 150 Mbps (6 iterations) of Turbo decoding or up to 85 Mbps of K = 9 with zero tail biting of Viterbi decoding, while supporting various standards such as: 3G-LTE, WiMAX and 3GPP-R6.
- The MAPLE-B also supports:
  — FFT/IFFT for sizes 128, 256, 512, 1024, or 2048 points at up to 200 Million samples per second
  — DFT/IDFT for sizes up to 1536 points at up to 130 Million samples per second
- Power supplies:
  — Logic power: 1 V nominal
  — I/O power: 1.8 V, 2.5 V, and 3.3 V nominal
- Flip Chip-Plastic Ball Grid Array (FC-PBGA), 1 mm pitch, 29 mm × 29 mm

1.3 Device Level Features

The MSBA8100 device delivers best-in-class performance and integration, embeds the MAPLE-B accelerator for Turbo and Viterbi channel decoding and for DFT/IDFT and FFT/IFFT algorithms acceleration. The MSBA8100 device also includes large internal memory and supports a variety of advanced interface types, including two RapidIO interfaces for data and control planes interfacing DSPs such as the MSC8144, switches and other ASICs or FPGAs, a PCI controller for easy configuration of the device and other control plane transactions, and a DDR controllers for high-speed, industry-standard memory interface. The MSBA8100 device offers tremendous processing power while maintaining a competitive price and power.

1.4 Module Level Features

- Multi Accelerator Platform Engine for Baseband (MAPLE-B)
  — Programmable System Interface
    – Software friendly buffer descriptor based handshake and task assignment.
    – Support for high priority and low priority tasks via multiple descriptor rings.
    – Processing elements management and scheduling.
    – Two master buses for data transfers from/to the system memory at total throughput up to 50 Gbps.
    – One slave bus for accessing MAPLE-B internal memories and registers.
    – Multi-Core Aware.
    – Interrupt or RapidIO Doorbell generation and/or status bit indication on job or multiple jobs completion.
    – System memory utilized only for input/output data, all the internal calculations are performed using MAPLE-B memories.
  — Turbo Decoding
    – Scalable architecture with 1, 2 or 4 Radix 4 dual-recursion engines.
    – Supports Wimax OFDMA turbo decoding as specified in **IEEE®** 802.16™-2004 standard and corrigendum **IEEE** P802.16-2004/Cor2/D2 standard, section 8.4.9.2.3.

- – Supports 3G-LTE (Evolved UTRA) turbo decoding as specified in 3GPP TS 36.212, section 5.1.2.2.
- – Supports 3GPP-R6 turbo decoding as specified in 3GPP TS 25.212, section 4.2.3.2.
- – Programmable Number of Iterations
- – Multiple stop conditions, including built in CRC check and A-Posteriori Quality Indication.
- – Programmable de-puncturing schemes including support for rate-dematching in 3G-LTE.
- – Binary and Duo-Binary turbo codes.
- – Support for trellis termination bits and tail biting.
- – Decoding techniques using: Max Log Map or Linear Log Map (MAX*) including extrinsic factorization.
- – 8-bit soft symbol inputs with Hard or Soft decision outputs.
  — Viterbi Decoding
  - – Supports WiMAX OFDMA channel decoding as specified in **IEEE** 802.16-2004 and corrigendum **IEEE** P802.16-2004/Cor2/D2, section 8.4.9.2.1.
  - – Supports 3G-LTE (Evolved UTRA) channel decoding as specified in 3GPP TS 36.212, section 5.1.2.1.
  - – Supports 3GPP-R6 viterbi decoding as specified in 3GPP TS 25.212, section 4.2.3.1.
  - – Fully programmable polynomials
  - – Programmable schemes for supporting various rates/puncturing cases (e.g. 1/2, 1/3).
  - – Support for zero tailing.
  - – Support for tail-bitting with multiple-iteration or WAVA* approaches.
  - – 8-bit soft symbol inputs with Hard or Soft decision outputs.
  — FFT/IFFT and DFT/IDFT processing
  - – Variable lengths FFT/IFFT processing of lengths 128, 256, 512, 1024 and 2048.
  - – Variable lengths DFT/IDFT processing of the form $2^k \cdot 3^m \cdot 5^n \cdot 12$, up to 1536 points.
  - – Mixed radix implementation using R2, R3, R4, R5 and R8 building blocks.
  - – 16-bit I, 16-bit Q input, output and twiddles resolutions.
  - – Input and output I/Q samples are interleaved in memory.
  - – Internal twiddles memory.
- Chip-level arbitration and switching system (CLASS)
  — A full fabric that arbitrates between the MAPLE-B initiator buses, Serial RapidIO controllers, PCI controller initiator bus to the M2 memory, DDR SDRAM controller, MAPLE-B target bus, PCI target bus and the device configuration control and status registers (CCSRs).
  — High bandwidth.
  — Non-blocking allows parallel accesses from multiple initiators to multiple targets.
  — Fully pipelined.
  — Low latency.
  — Per target arbitration highly optimized to the target characteristics using prioritized round-robin arbitration.
  — Reduces data flow bottlenecks and enables high-bandwidth internal data transfers.
- 512 Kbyte M2 low-latency memory for critical data and temporary data buffering. Accessible from all CLASS masters via four interleaved ports.
  — Runs at up to 400 MHz.
  — Four address-interleaved banks.

- — 64-bit wide port per bank.
- — Up to four simultaneously accesses.
- DDR Controller
  - — Up to 166 MHz clock rate (333 MHz data rate).
  - — 16/32-bit DDR SDRAM data bus.
  - — Supported memory includes 64 Mbit to 4 Gbit DDR2 devices with x8/x16 data ports (no direct x4 support).
  - — DDR SDRAM chip configurations up to 512 Mbyte, including:
    - – Up to two physical banks (chip selects), each independently addressable.
    - – 32/40-bit SDRAM data bus and 16/24-bit SDRAM data bus for DDR and DDR2.
  - — Up to two memory chip selects with each chip select independently addressable.
  - — Four or eight sub-banks per chip select.
  - — DDR SDRAM timing parameters are fully programmable.
  - — Data mask (DM) signal and read-modify-write (RMW) for writing less than 4 bytes.
  - — Open page management (up to four open pages).
  - — Double-bit error detection and single-bit error correction (ECC).
  - — Sleep power management.
- Serial RapidIO Subsystem
  - — Two serial RapidIO ports supporting 1x/4x operation up to 3.125 Gbaud, each containing a RapidIO messaging unit and a RapidIO DMA unit.
  - — Each 1x/4x serial RapidIO endpoint operates at 1.25/2.5/3.125 Gbaud and complies with the following parts of Specification 1.2 of the RapidIO trade association interconnect specification:
    - – Part I (input and output logical specifications)
    - – Part II (message passing logical specification)
    - – Part III (common transport specification)
    - – Part VI (physical layer 1x LP-serial specification)
    - – Part VIII (error management extension specification)
  - — Each serial RapidIO port supports read, write, messages, doorbells, and maintenance accesses:
    - – Small and large transport information field only
    - – All priorities flow
  - — Each RapidIO Messaging Unit supports:
    - – Two outbound message queues
    - – Two inbound message queues
    - – One outbound doorbell queue
    - – One inbound doorbell queue
    - – One inbound port-write queue
  - — Each RapidIO DMA unit supports:
    - – Four high-speed/high-bandwidth channels accessible by local and remote masters
    - – Basic DMA operation modes (direct, simple chaining)
    - – Extended DMA operation modes (advanced chaining and stride capability)
    - – Programmable bandwidth control between channels
    - – Up to 256 bytes for DMA sub-block transfers to maximize performance over the RapidIO interface

- – Three priority levels supported for source and destination transactions
- PCI
  - — Designed to be compliant with the PCI specification revision 2.2 per the voltage specifications in the *MSBA8100 Technical Data* sheet
  - — 33 MHz and 66 MHz
  - — 32-bit PCI interface
  - — PCI 3.3V compatible
  - — Accesses to all PCI address spaces
  - — PCI-to-system and system-to-PCI streaming
- Clocks
  - — Three input clocks:
    - – Global input clock.
    - – Two differential input clocks (one per each serial RapidIO PLL).
  - — Four PLLs:
    - – System PLL
    - – DDR PLL
    - – Two Serial RapidIO PLLs.
  - — Clock ratios selected during reset via reset configuration pins.
- General-purpose input/output (GPIO) ports:
  - — 4 GPIO ports
  - — All ports are bidirectional
  - — All ports have open-drain output capability
- JTAG. Test Access Port (TAP) and Boundary Scan Architecture designed to comply with **IEEE** Std. 1149.1™.
- Reduced power dissipation
  - — Very low power CMOS design
  - — Low-power standby modes
  - — Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
- Technology: The MSBA8100 device is manufactured using CMOS 90 nm SOI technology.

2 Developer Environment

Freescale supplies a set of development tools for the MSBA8100 device to develop 3G-LTE and WiMAX systems.

2.1 Tools

The MSBA8100 device tool components include:

- *Development Board.* A board with the MSBA8100 device connected to two 16-bit DDR memories. The MSBA8100 also connects to an MSC8144 DSP via the 4x serial RapidIO interface and to an MPC8560 via the PCI. The board also includes an AMC connector to allow connection to another board over the 4x serial RapidIO interface.
- *Device Drivers*. Drivers with SmartDSP OS for MSC814x to configure and control the MSBA8100 device.
- *Implementation Examples*. A set of examples for different hardware and software configurations implementing the transmit/receive functions of the different processing engines: Turbo, Viterbi, FFT, and DFT through the underlying PCI and serial RapidIO physical interfaces.

2.2 Application Software

Freescale offers a broad range of DSP applications through its third-party application software partners; these applications target IP telephony, telephony modem, wireless and multimedia transcoding, and wireless base stations. Applications and software modules are listed in **Table 1**.

Table 1. Application Software Modules

Application	Modules
Baseband	WiMAX solution supporting Wave 1 features with future extension to Wave 2 and beyond.
	3G-LTE evolving kernels library.
	Optimized FFT kernels, including matrix multiplication, and so forth.
Device Drivers and Example Code	MAPLE-B driver, DMA driver, serial RapidIO driver, TDM driver, Ethernet driver, UART driver, memory allocation, and interrupt handling.
StarCore Libraries	Rich set of StarCore software libraries, including: Math (Part 1 and 2), Signal, Complex vector, Control function, Frequency domain, Filter, Common, Image Processing, Communication, and Matrix.

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