

Features

- I_{off} supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16245T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162245T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162H245T Features:

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors

Functional Description

These 16-bit transceivers are designed for use in bidirectional synchronous communication between two buses, where high speed and low power are required. With the exception of the CY74FCT16245T, these devices can be operated either as two independent octals or a single 16-bit transceiver. Direction of data flow is controlled by (DIR), the Output Enable (\overline{OE}) transfers data when LOW and isolates the buses when HIGH.

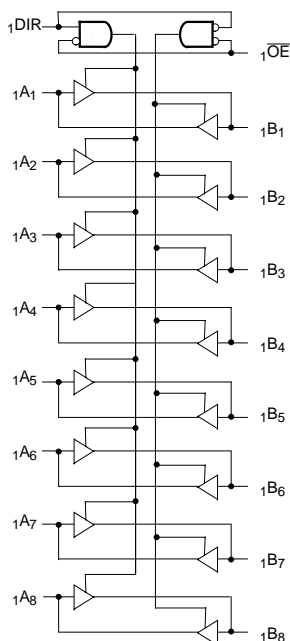
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16245T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

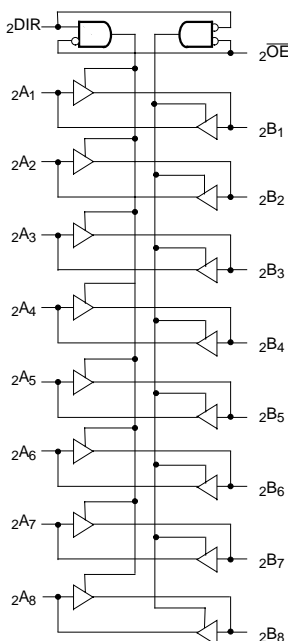
The CY74FCT162245T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162245T is ideal for driving transmission lines.

The CY74FCT162H245T is a 24-mA balanced output part that has bus hold on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Logic Block Diagrams CY74FCT16245T, CY74FCT162245T, CY74FCT162H245T



FCT16245-1



FCT16245-2

Pin Configuration

SSOP/TSSOP Top View

| | | | |
|------|----|----|-----|
| 1DIR | 1 | 48 | 1OE |
| 1B1 | 2 | 47 | 1A1 |
| 1B2 | 3 | 46 | 1A2 |
| GND | 4 | 45 | GND |
| 1B3 | 5 | 44 | 1A3 |
| 1B4 | 6 | 43 | 1A4 |
| VCC | 7 | 42 | VCC |
| 1B5 | 8 | 41 | 1A5 |
| 1B6 | 9 | 40 | 1A6 |
| GND | 10 | 39 | GND |
| 1B7 | 11 | 38 | 1A7 |
| 1B8 | 12 | 37 | 1A8 |
| 2B1 | 13 | 36 | 2A1 |
| 2B2 | 14 | 35 | 2A2 |
| GND | 15 | 34 | GND |
| 2B3 | 16 | 33 | 2A3 |
| 2B4 | 17 | 32 | 2A4 |
| VCC | 18 | 31 | VCC |
| 2B5 | 19 | 30 | 2A5 |
| 2B6 | 20 | 29 | 2A6 |
| GND | 21 | 28 | GND |
| 2B7 | 22 | 27 | 2A7 |
| 2B8 | 23 | 26 | 2A8 |
| 2DIR | 24 | 25 | 2OE |

FCT16245-3

Pin Description

| Name | Description |
|------|---|
| OE | Three-State Output Enable Inputs (Active LOW) |
| DIR | Direction Control |
| A | Inputs or Three-State Outputs ^[1] |
| B | Inputs or Three-State Outputs ^[1] |

Function Table^[2]

| Inputs | | Outputs |
|--------|-----|---------------------|
| OE | DIR | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature Com'l -55°C to +125°C

Ambient Temperature with

Power Applied..... Com'l -55°C to +125°C

DC Input Voltage -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current

(Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage..... >2001V
(per MIL-STD-883, Method 3015)

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Industrial | -40°C to +85°C | 5V ± 10% |

Notes:

- On CY74FCT162H245T these pins have bus hold.
- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ. ^[5] | Max. | Unit |
|--|---|---|--|---------------------|------|------|
| V _{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V _{IL} | Input LOW Voltage | | | | 0.8 | V |
| V _H | Input Hysteresis ^[6] | | | 100 | | mV |
| V _{IK} | Input Clamp Diode Voltage | V _{CC} =Min., I _{IN} =-18 mA | | -0.7 | -1.2 | V |
| I _{IH} | Input HIGH Current | Standard Bus Hold | V _{CC} =Max., V _I =V _{CC} | | ±1 | μA |
| | | | | | ±100 | |
| I _{IL} | Input LOW Current | Standard Bus Hold | V _{CC} =Max., V _I =GND | | ±1 | μA |
| | | | | | ±100 | μA |
| I _{BBH} I _{BBL} | Bus Hold Sustain Current on Bus Hold Input ^[7] | V _{CC} =Min. V _I =2.0V V _I =0.8V | -50 +50 | | | μA |
| I _{BHHO} I _{BHLO} | Bus Hold Overdrive Current on Bus Hold Input ^[7] | V _{CC} =Max., V _I =1.5V | | | TBD | mA |
| I _{OZH} | High Impedance Output Current (Three-State Output pins) | V _{CC} =Max., V _{OUT} =2.7V | | | ±1 | μA |
| I _{OZL} | High Impedance Output Current (Three-State Output pins) | V _{CC} =Max., V _{OUT} =0.5V | | | ±1 | μA |
| I _{OS} | Short Circuit Current ^[8] | V _{CC} =Max., V _{OUT} =GND | -80 | -140 | -200 | mA |
| I _O | Output Drive Current ^[8] | V _{CC} =Max., V _{OUT} =2.5V | -50 | | -180 | mA |
| I _{OFF} | Power-Off Disable | V _{CC} =0V, V _{OUT} ≤4.5V ^[9] | | | ±1 | μA |

Output Drive Characteristics for CY74FCT16245T

| Parameter | Description | Test Conditions | Min. | Typ. ^[5] | Max. | Unit |
|-----------------|---------------------|--|------|---------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-3 mA | 2.5 | 3.5 | | V |
| | | V _{CC} =Min., I _{OH} =-15 mA | 2.4 | 3.5 | | V |
| | | V _{CC} =Min., I _{OH} =-32 mA | 2.0 | 3.0 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =64 mA | | 0.2 | 0.55 | V |

Output Drive Characteristics for CY74FCT162245T, CY74FCT162H245T

| Parameter | Description | Test Conditions | Min. | Typ. ^[5] | Max. | Unit |
|------------------|------------------------------------|---|------|---------------------|------|------|
| I _{ODL} | Output LOW Current ^[8] | V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V | 60 | 115 | 150 | mA |
| I _{ODH} | Output HIGH Current ^[8] | V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V | -60 | -115 | -150 | mA |
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-24 mA | 2.4 | 3.3 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =24 mA | | 0.3 | 0.55 | V |

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is specified but not tested.
7. Pins with bus hold are described in Pin Description.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
9. Tested at +25°C.

Capacitance^[6] (T_A = +25°C, f = 1.0 MHz)

| Parameter | Description | Test Conditions | Typ. ^[5] | Max. | Unit |
|------------------|--------------------|-----------------------|---------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6.0 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 5.5 | 8.0 | pF |

Power Supply Characteristics

| Parameter | Description | Test Conditions | | Typ. ^[5] | Max. | Unit |
|-----------------|--|--|---|---------------------|----------------------|--------------------|
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$ | $V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ | 5 | 500 | μA |
| ΔI_{CC} | Quiescent Power Supply Current (TTL inputs HIGH) | $V_{CC} = \text{Max.}$ | $V_{IN} = 3.4V^{[10]}$ | 0.5 | 1.5 | mA |
| I_{CCD} | Dynamic Power Supply Current ^[11] | $V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $OE = \overline{DIR} = \text{GND}$ | $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$ | 60 | 100 | $\mu A/\text{MHz}$ |
| I_C | Total Power Supply Current ^[12] | $V_{CC} = \text{Max.}$, $f_1 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $OE = \overline{DIR} = \text{GND}$ | $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$ | 0.6 | 1.5 | mA |
| | | | $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ | 0.9 | 2.3 | mA |
| | | $V_{CC} = \text{Max.}$, $f_1 = 2.5 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $OE = \overline{DIR} = \text{GND}$ | $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$ | 2.4 | 4.5 ^[13] | mA |
| | | | $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ | 6.4 | 16.5 ^[13] | mA |

Notes:

10. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[14]

| Parameter | Description | 74FCT16245T 74FCT162245T | | 74FCT16245AT 74FCT162245AT 74FCT162H245AT | | Unit | Fig. No. ^[15] |
|--------------------------------------|--|-----------------------------|------|---|------|------|-----------------------------|
| | | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output A to B, B to A | 1.5 | 7.0 | 1.5 | 4.5 | ns | 1, 3 |
| t _{PZH} t _{PZL} | Output Enable Time OE to A or B | 1.5 | 9.5 | 1.5 | 6.2 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time OE to A or B | 1.5 | 7.5 | 1.5 | 5.0 | ns | 1, 7, 8 |
| t _{PZH} t _{PZL} | Output Enable Time DIR to A or B | 1.5 | 9.5 | 1.5 | 6.2 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time DIR to A or B | 1.5 | 7.5 | 1.5 | 5.0 | ns | 1, 7, 8 |
| t _{SK(O)} | Output Skew ^[16] | | 0.5 | | 0.5 | ns | — |

| Parameter | Description | 74FCT16245CT 74FCT162245CT 74FCT162H245CT | | Unit | Fig. No. ^[15] |
|--------------------------------------|--|---|------|------|-----------------------------|
| | | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output A to B, B to A | 1.5 | 4.1 | ns | 1, 3 |
| t _{PZH} t _{PZL} | Output Enable Time OE to A or B | 1.5 | 5.8 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time OE to A or B | 1.5 | 4.8 | ns | 1, 7, 8 |
| t _{PZH} t _{PZL} | Output Enable Time DIR to A or B | 1.5 | 5.8 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time DIR to A or B | 1.5 | 4.8 | ns | 1, 7, 8 |
| t _{SK(O)} | Output Skew ^[16] | | 0.5 | ns | — |

Note:

14. Minimum limits are specified but not tested on Propagation Delays.

15. See "Parameter Measurement Information" in the General Information section.

16. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16245

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---------------|------------------------|-----------------|-------------------------|--------------------|
| 4.1 | CY74FCT16245CTPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16245CTPVC/PVCT | O48 | 48-Lead (300-Mil) SSOP | |
| 4.5 | CY74FCT16245ATPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16245ATPVC/PVCT | O48 | 48-Lead (300-Mil) SSOP | |
| 7.0 | CY74FCT16245TPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16245TPVC/PVCT | O48 | 48-Lead (300-Mil) SSOP | |

Ordering Information CY74FCT162245

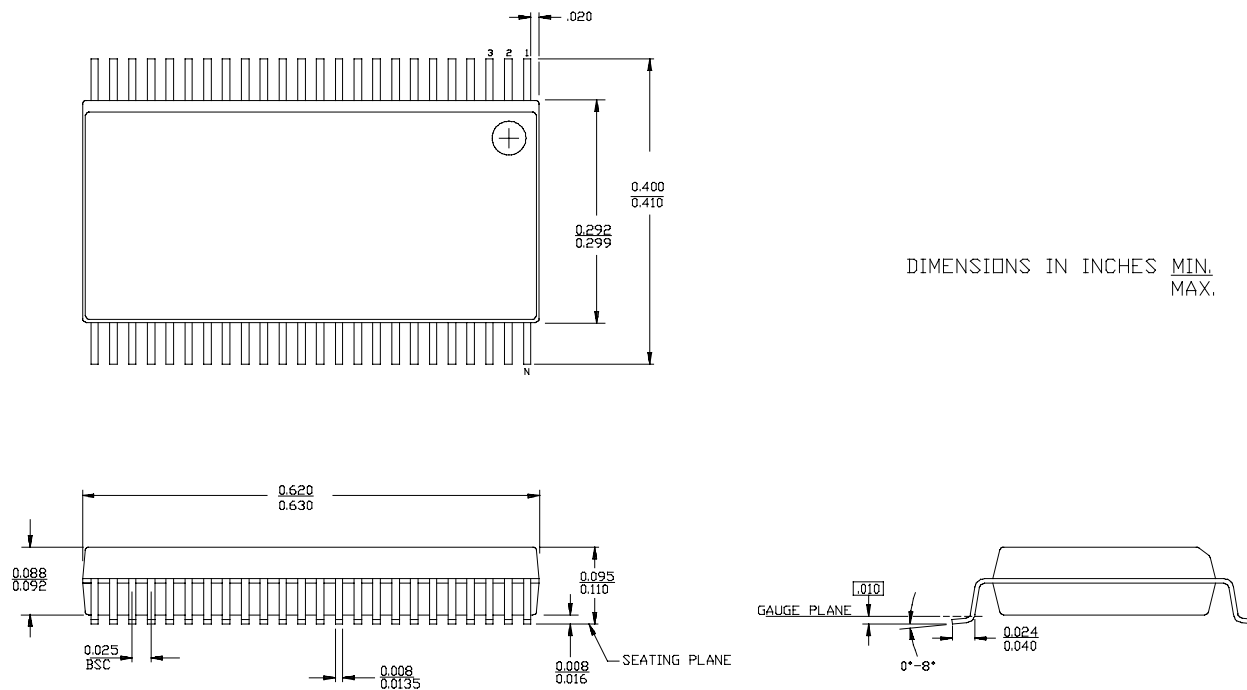
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|------------------------|--------------|-------------------------|-----------------|
| 4.1 | CY74FCT162245CTPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162245CTPVC | O48 | 48-Lead (300-Mil) SSOP | |
| | 74FCT162245CTPVCT | O48 | 48-Lead (300-Mil) SSOP | |
| 4.5 | 74FCT162245ATPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162245ATPVC | O48 | 48-Lead (300-Mil) SSOP | |
| | 74FCT162245ATPVCT | O48 | 48-Lead (300-Mil) SSOP | |
| 7.0 | CY74FCT162245TPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162245TPVC/PVCT | O48 | 48-Lead (300-Mil) SSOP | |

Ordering Information CY74FCT162H245

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------------|--------------|-------------------------|-----------------|
| 4.1 | 74FCT162H245CTPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162H245CTPVC | O48 | 48-Lead (300-Mil) SSOP | |
| | 74FCT162H245CTPVCT | O48 | 48-Lead (300-Mil) SSOP | |
| 4.5 | 74FCT162H245ATPACT | Z48 | 48-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162H245ATPVC | O48 | 48-Lead (300-Mil) SSOP | |
| | 74FCT162H245ATPVCT | O48 | 48-Lead (300-Mil) SSOP | |

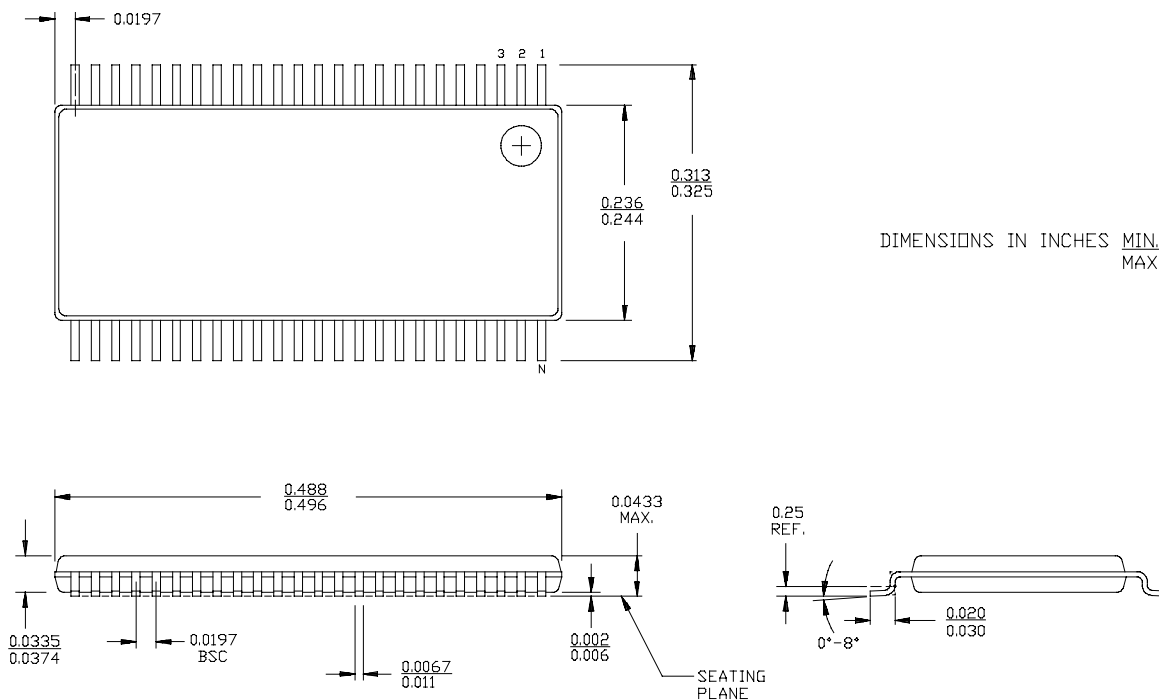
Package Diagrams

48-Lead Shrunk Small Outline Package O48



Package Diagrams

48-Lead Thin Shrunk Small Outline Package Z48



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