Numbers in parenthesis denote pin numbers for F package (Case 650).

FUNCTIONS AND CHARACTERISTICS (continued)

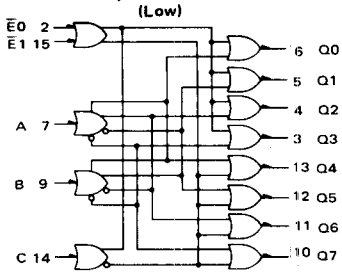
Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Universal Decade Counter	MC10137	MC10537	f = 150 MHz	625	620,650
Bi-Quinary Counter	MC10138	–	f = 150 MHz	370	620
64-Bit Random Access Memory (90 Ω)	MCM10140	–	t_{Access} = 15 (max)	420	620,690
Four-Bit Universal Shift Register	MC10141	MC10541	f = 200 MHz	425	620,648,650
64-Bit Random Access Memory (50 Ω)	MCM10142	–	t_{Access} = 10 (max)	420	620
8 x 2 Multiport Register File (RAM)	MCM10143	–	t_{Access} = 10	610	623
256-Bit Random Access Memory	MCM10144	–	t_{Access} = 30 (max)	420	620,690
64-Bit Register File (RAM)	MCM10145	–	t_{Access} = 10	625	620
128-Bit Random Access Memory	MCM10147	–	t_{Access} = 12 (max)	420	620
64-Bit Random Access Memory (50 Ω)	MCM10148	–	t_{Access} = 15 (max)	420	620
1024-Bit Programmable Read Only Memory	MCM10150	–	t_{Access} = 20	–	690
Quad Latch	MC10153	–	4.0	310	620
12-Bit Parity Generator-Checker	MC10160	MC10560	5.0	320	620,648,650
Binary to 1-8 Decoder (Low)	MC10161	MC10561	4.0	315	620,648,650
Binary to 1-8 Decoder (High)	MC10162	MC10562	4.0	315	620,648,650
Error Detection-Correction Circuit	MC10163	–	5.0	520	620
8-Line Multiplexer	MC10164	MC10564	3.0	310	620,648,650
8-Input Priority Encoder	MC10165	–	7.0	545	620,648
5-Bit Magnitude Comparator	MC10166	–	6.0	440	620
Quad Latch	MC10168	–	3.0	310	620
Dual Binary To 1-4 Decoder (Low)	MC10171	MC10571	4.0	325	620,648,650
Dual Binary To 1-4 Decoder (High)	MC10172	MC10572	4.0	325	620,648,650
Quad 2-Input Multiplexer/Latch	MC10173	–	2.5	275	620,648
Dual 4 To 1 Multiplexer	MC10174	MC10574	3.5	305	620,650
Quint Latch	MC10175	MC10575	2.5	400	620
Hex "D" Master-Slave Flip-Flop	MC10176	–	f = 250 MHz	460	620
Triple MECL to NMOS Translator	MC10177	–	–	1.0 W	620
Binary Counter	MC10178	–	f = 150 MHz	370	620
Look-Ahead Carry Block	MC10179	MC10579	3.0 (Cn,P) 4.0 (G)	300	620,648,650
Dual High Speed Adder/Subtractor	MC10180	MC10580	4.5	360	620,648,650
4-Bit Arithmetic Logic Unit/Function Generator	MC10181	MC10581	See Logic Diag.	600	623,649,652
2-Bit Arithmetic Logic Unit/Function Generator	MC10182	–	See Logic Diag.	575	620
Error Detection-Correction Circuit	MC10193	–	7.5	520	620
Hex Inverter/Buffer	MC10195	–	2.0	200	620
Hex "AND" Gate	MC10197	–	2.8	200	620
High Speed Dual 3-Input 3-Output OR Gate	MC10210	–	1.5	160	620
High Speed Dual 3-Input 3-Output NOR Gate	MC10211	–	1.5	160	620
High Speed Dual 3-Input 3-Output OR/NOR Gate	MC10212	–	1.5	160	620
High Speed Triple Line Receiver	MC10216	MC10616	1.8	100	620,648,650
High Speed Dual Type D Master-Slave Flip-Flop	MC10231	MC10631	f = 225 MHz	270	620,648,650
High Speed 2 x 1 Bit Array Multiplier Block	MC10287	–	–	400	620

① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*Load Power not included

DECODERS

MC10161
MC10561
Binary To 1-8 Decoder
(Low)



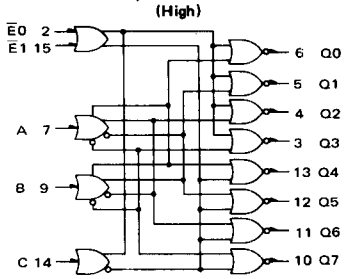
TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
Ē1	Ē0	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Φ	Φ	Φ	Φ	H	H	H	H	H	H	H	H

Φ = Don't Care

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

MC10162
MC10562
Binary To 1-8 Decoder
(High)



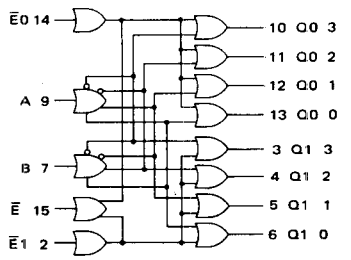
TRUTH TABLE

INPUTS					OUTPUTS							
Ē0	Ē1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	Φ	Φ	Φ	Φ	L	L	L	L	L	L	L	L
Φ	H	Φ	Φ	Φ	L	L	L	L	L	L	L	L

Φ = Don't Care

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

MC10171
Dual Binary To 1-4 Decoder
(Low)



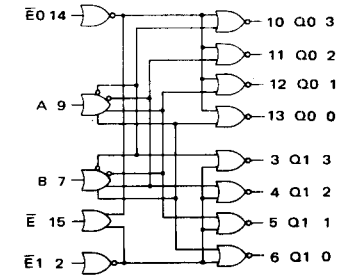
TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
Ē	Ē0	Ē1	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	H	L	H	L	H	H	H	L	H	H
L	L	L	L	H	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	H	Φ	Φ	Φ	H	H	H	H	L	H	H	H
H	Φ	Φ	Φ	Φ	H	H	H	H	H	H	H	H

Φ = Don't Care

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

MC10172
Dual Binary To 1-4 Decoder
(High)



TRUTH TABLE

Ē	Ē1	Ē0	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	H	L	L	H	L	L	L	H	L	L
L	H	H	L	H	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
H	H	Φ	Φ	Φ	L	L	L	L	L	L	L	L

Φ = Don't Care

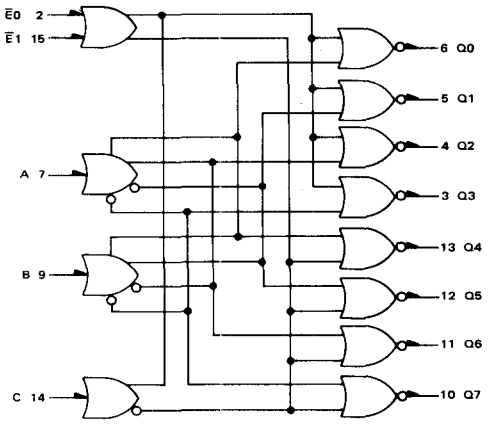
P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

BINARY TO 1-8 DECODER
(HIGH)

MC10162

The MC10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

POSITIVE LOGIC



P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E}0$	$\overline{E}1$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

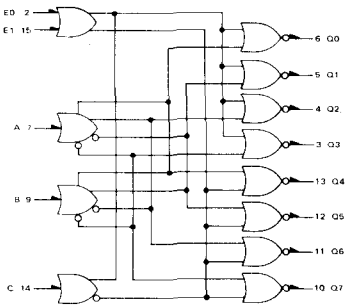
ϕ = Don't Care

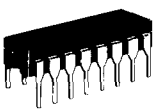
See General Information section for packaging.

3

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.



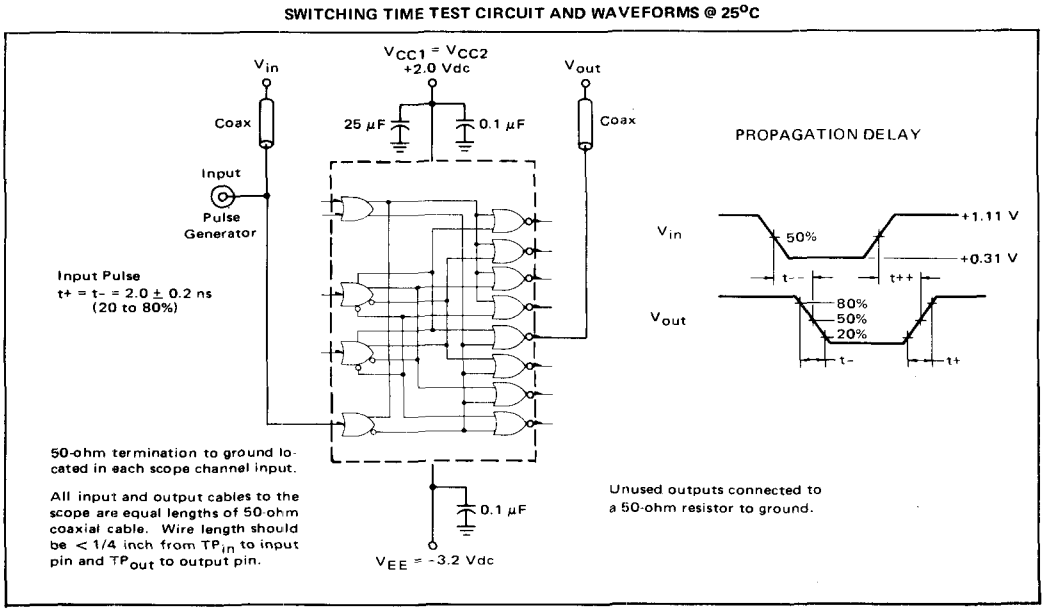


L SUFFIX
CERAMIC PACKAGE
CASE 620

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

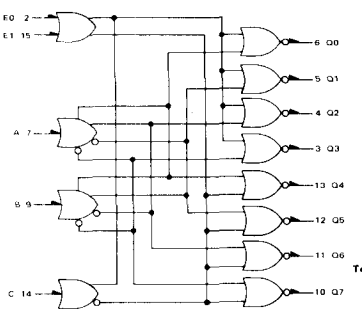
Characteristic	Symbol	Pin Under Test	MC10162L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8				61	76	–		mAdc		–	–	–	8	1,16
Input Current	I_{inH}	14		–			220			μAdc	14	–	–	–	8	1,16
	I_{inL}	14			0.5	–			–	μAdc		14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	2	–	–	–	8	1,16
		13	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080		-0.980			-0.910	–	Vdc		–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–		-1.630		-1.595	Vdc	–		2	–	8	1,16
		13		-1.655		–	-1.630		-1.595	Vdc			15	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	–	14	13	8	1,16
	t_{14-13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		–	–				
Rise Time (20% to 80%)	t_+	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				
Fall Time (20% to 80%)	t_-	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.



P SUFFIX
PLASTIC PACKAGE
CASE 648

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10162P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	-	-	-	61	76	-	-	mAdc	-	-	-	-	8	1,16
Input Current	I_{inH}	14	-	-	-	-	220	-	-	μAdc	14	-	-	-	8	1,16
	I_{inL}	14	-	-	0.5	-	-	-	-	μAdc	-	14	-	-	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	14	-	-	-	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	2	-	-	-	8	1,16
		13	-1.890	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	15	-	-	-	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	-	-0.980	-	-	-0.910	-	Vdc	-	-	14	-	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	2	-	8	1,16
		13	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	15	-	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	-	-	1.5	4.0	6.0	-	-	ns	-	-	14	13	8	1,16
	t_{14-13-}	13	-	-	1.5	4.0	6.0	-	-		-	-				
Rise Time (20% to 80%)	t_+	13	-	-	1.1	2.0	3.3				-	-				
Fall Time (20% to 80%)	t_-	13	-	-	1.1	2.0	3.3	-	-		-					

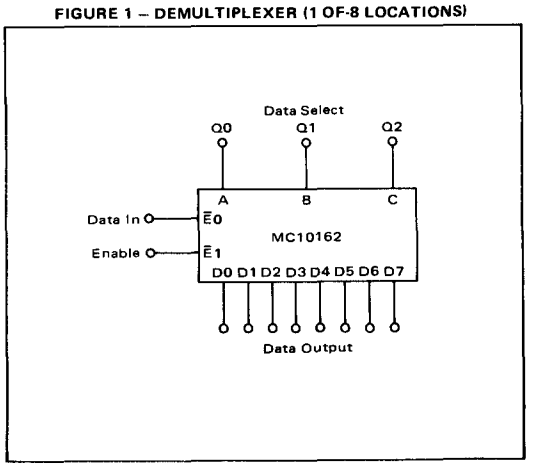
APPLICATION INFORMATION

The MC10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications as shown in Figure 1. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 2. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. Control information via twisted pair lines is sent through MC10101 gates to the MC10115 line receivers to provide select data to the multiplexer/demultiplexer units.

FIGURE 1 – DEMULTIPLEXER (1 OF-8 LOCATIONS)



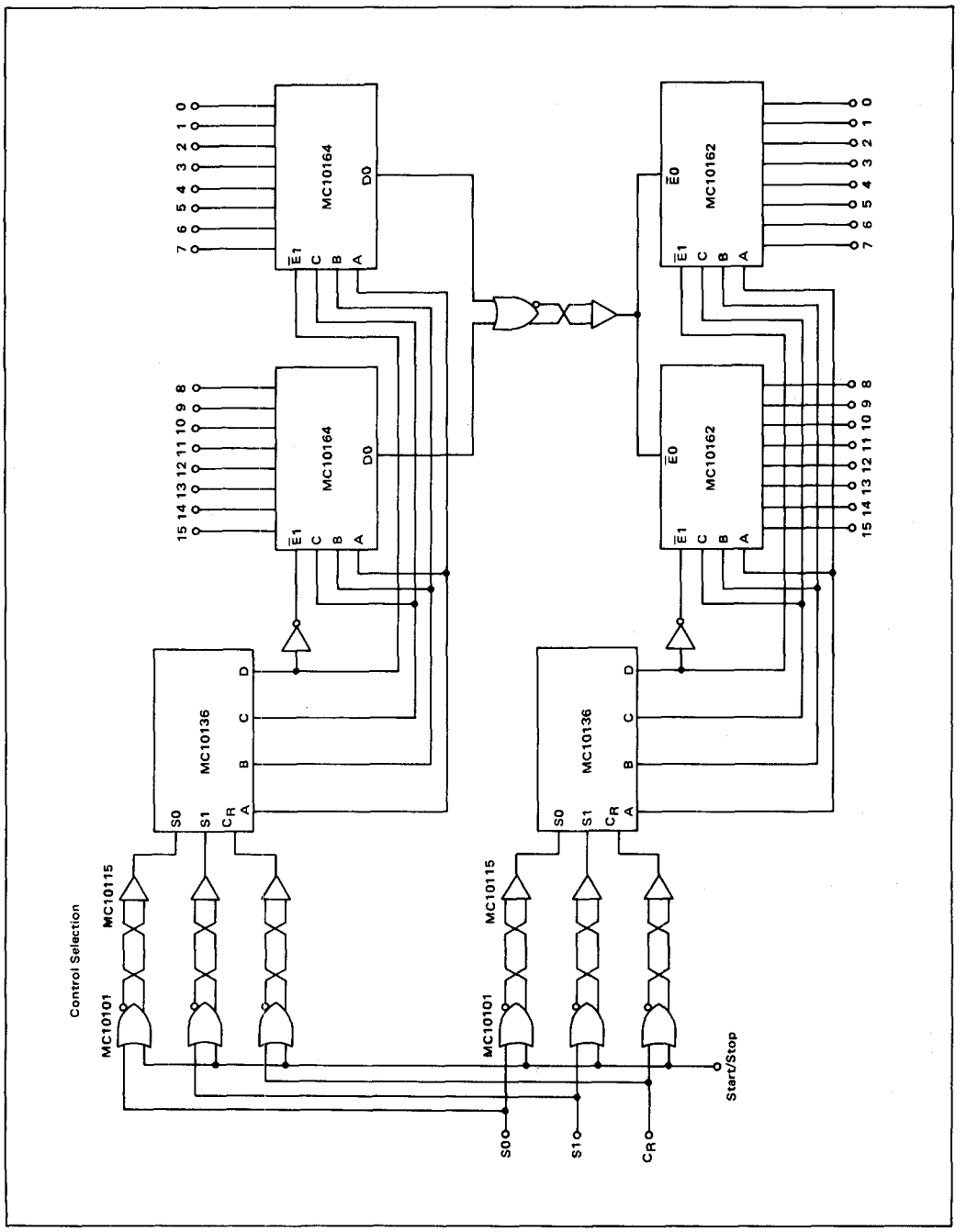


FIGURE 2 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER