

74F132

Quad 2-Input NAND Schmitt Trigger

General Description

The F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt Trigger followed by level shifting circuitry and a standard FAST™ output struc-

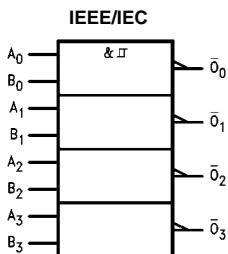
ture. The Schmitt Trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Code:

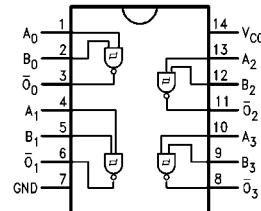
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F132SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| 74F132SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F132PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Function Table

| Inputs | | Outputs |
|--------|---|---------|
| A | B | O |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|---------------------------|-------------------|--------------------|---|
| A_n, B_n \bar{O}_n | Inputs Outputs | 1.0/1.0 50/33.3 | $20 \mu A/-0.6 mA$ $-1 mA/20 mA$ |

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Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|-------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V_{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC} = 0V$) | |
| Standard Output | -0.5V to V_{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated I_{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

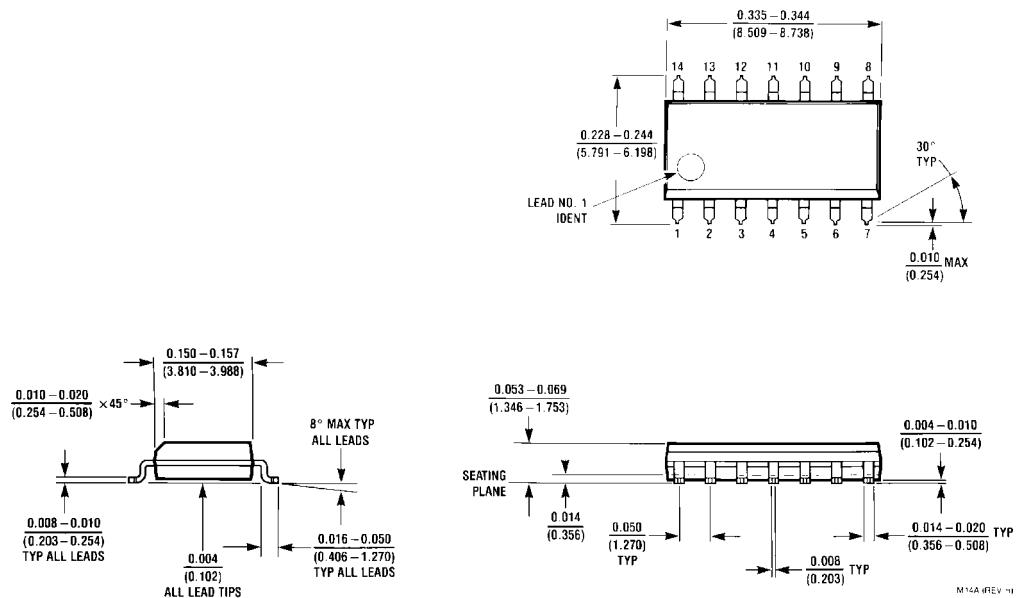
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V_{CC} | Conditions |
|--------------|-----------------------------------|--------------|-----|------|---------------|----------|---|
| V_{T+} | Positive-going Threshold | 1.5 | | 2.0 | V | 5.0 | |
| V_{T-} | Negative-going Threshold | 0.7 | | 1.1 | V | 5.0 | |
| ΔV_T | Hysteresis ($V_T^+ - V_T^-$) | 0.4 | | | V | 5.0 | |
| V_{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | $I_{IN} = -18 \text{ mA}$ |
| V_{OH} | Output HIGH Voltage | 10% V_{CC} | 2.5 | | V | Min | $I_{OH} = -1 \text{ mA}$ |
| | 5% V_{CC} | 2.7 | | | | | $I_{OH} = -1 \text{ mA}$ |
| V_{OL} | Output LOW Voltage | 10% V_{CC} | | 0.5 | V | Min | $I_{OL} = 20 \text{ mA}$ |
| I_{IH} | Input HIGH Current | | | 5.0 | μA | Max | $V_{IN} = 2.7V$ |
| I_{BVI} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | $V_{IN} = 7.0V$ |
| I_{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | $V_{OUT} = V_{CC}$ |
| I_{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | $I_{ID} = 1.9 \mu\text{A}$ All Other Pins Grounded |
| I_{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | $V_{OD} = 150 \text{ mV}$ All Other Pins Grounded |
| I_{IL} | Input LOW Current | | | -0.6 | mA | Max | $V_{IN} = 0.5V$ |
| I_{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | $V_{OUT} = 0V$ |
| I_{CCH} | Power Supply Current | | | 17.0 | mA | Max | $V_O = \text{HIGH}$ |
| I_{CCL} | Power Supply Current | | | 18.0 | mA | Max | $V_O = \text{LOW}$ |

AC Electrical Characteristics

| Symbol | Parameter | $T_A = +25^\circ\text{C}$ | | | $T_A = 0^\circ\text{C} \text{ to } +70^\circ\text{C}$ | | Units |
|-----------|--|---------------------------|-----|--------------|---|--------------|-------|
| | | Min | Typ | Max | Min | Max | |
| t_{PLH} | Propagation Delay A_n, B_n to \bar{O}_n | 4.0 5.0 | | 10.5 12.5 | 3.5 5.0 | 12.0 13.0 | ns |

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

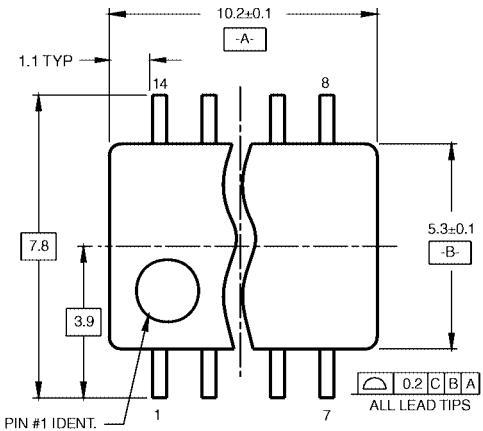
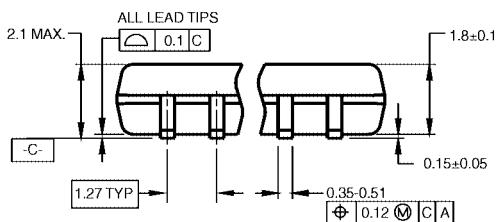


Diagram illustrating the layout of components on a printed circuit board. Components are labeled 14, 13, 9, 8, 1, 2, 6, and 7. Dimensions shown are 5.01 TYP, 9.27 TYP, 2.13 TYP, 1.27 TYP, and 0.6 TYP.

LAND PATTERN RECOMMENDATION

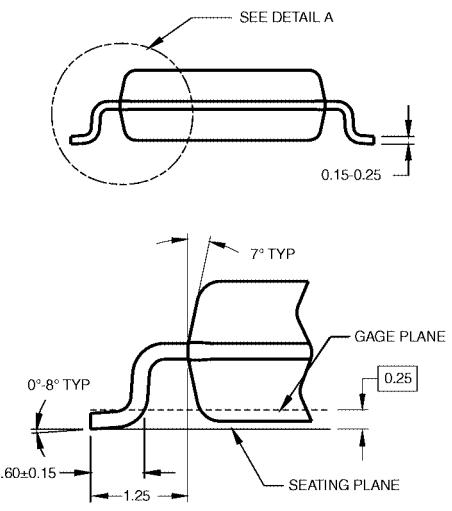


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

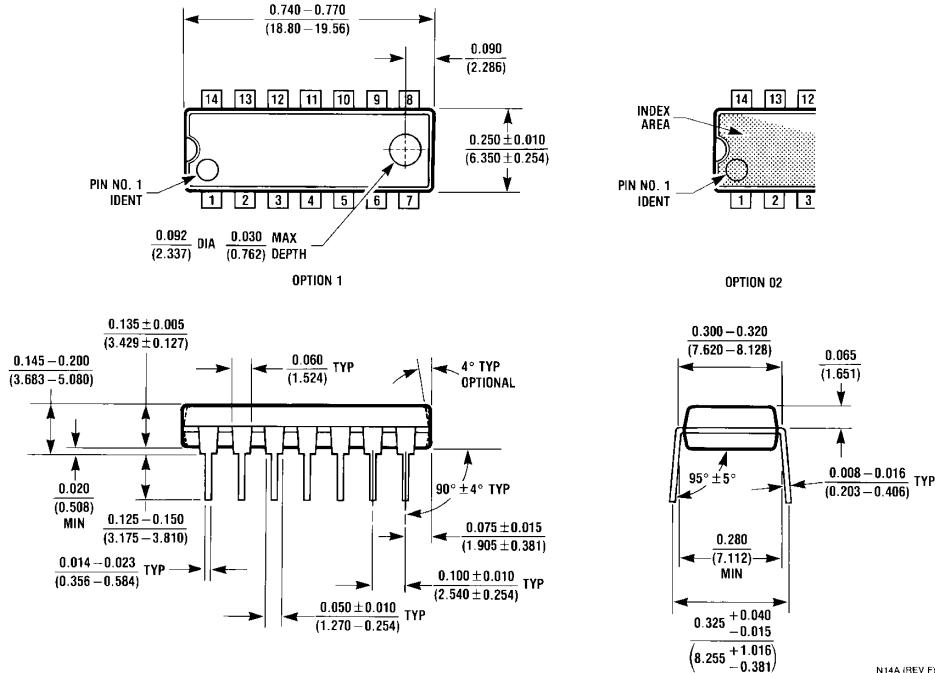
M14DRevB1



DETAIL A

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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