

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## Analog Multiplexers / Demultiplexers High-Performance Silicon-Gate CMOS

The MC74VHC4051, MC74VHC4052 and MC74VHC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The VHC4051, VHC4052 and VHC4053 are identical in pinout to the high-speed HC4051A, HC4052A and HC4053A, and the metal-gate MC14051B, MC14052B and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance ( $R_{on}$ ) is more linear over input voltage than  $R_{on}$  of metal-gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- Chip Complexity: VHC4051 — 184 FETs or 46 Equivalent Gates  
VHC4052 — 168 FETs or 42 Equivalent Gates  
VHC4053 — 156 FETs or 39 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



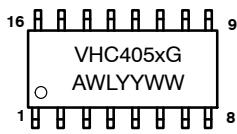
ON Semiconductor

<http://onsemi.com>

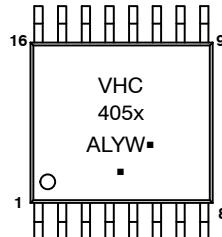
### MARKING DIAGRAMS



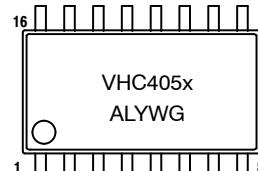
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC EIAJ-16  
M SUFFIX  
CASE 966



VHC405x = Specific Device Code  
(x = 1, 2 or 3)

A = Assembly Location

L, WL = Wafer Lot

Y, YY = Year

W, WW = Work Week

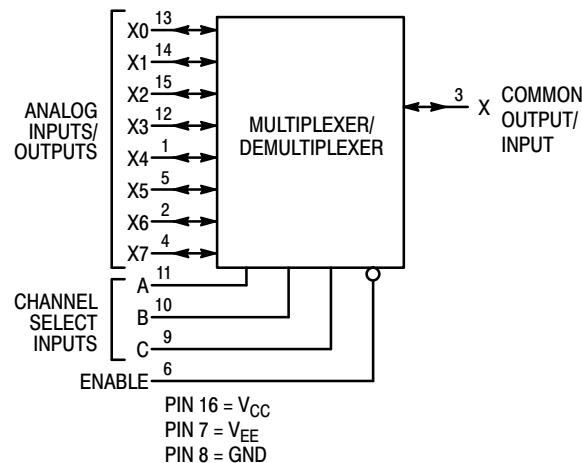
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

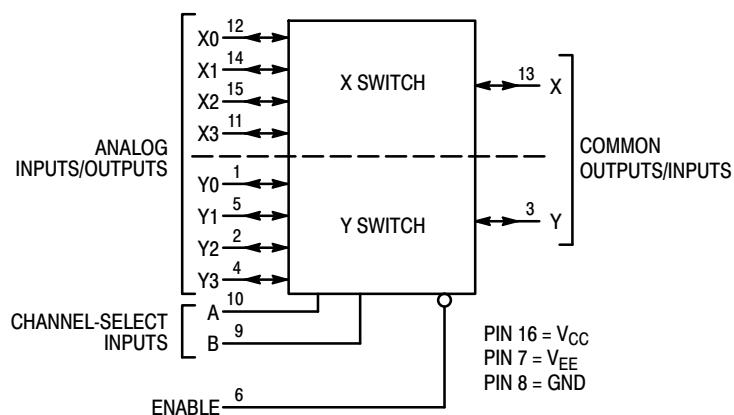
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

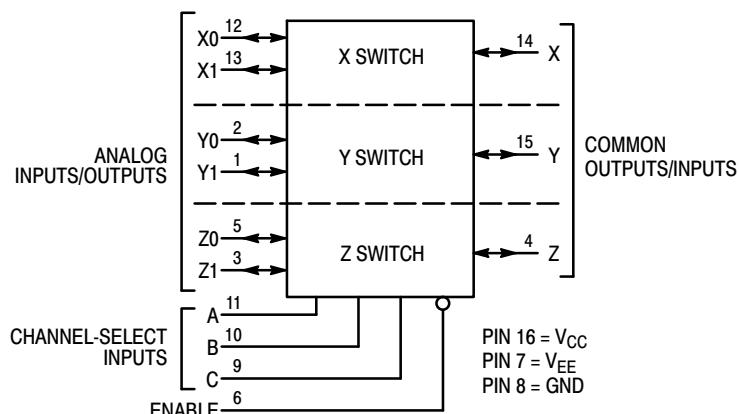
## MC74VHC4051, MC74VHC4052, MC74VHC4053



**MC74VHC4051**  
Single-Pole, 8-Position Plus Common Off



**MC74VHC4052**  
Double-Pole, 4-Position Plus Common Off



NOTE: This device allows independent control of each switch.  
Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

**MC74VHC4053**  
Triple Single-Pole, Double-Position Plus Common Off

**Figure 1. Logic Diagrams**

# MC74VHC4051, MC74VHC4052, MC74VHC4053

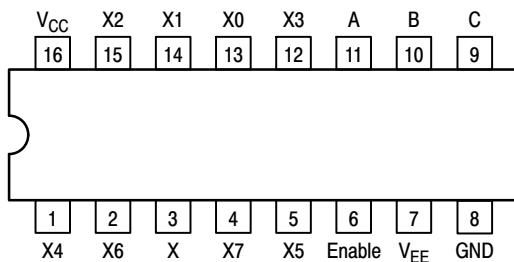


Figure 2. Pinout: MC74VHC4051 (Top View)

## FUNCTION TABLE – MC74VHC4051

Control Inputs			ON Channels
Enable	Select		
	C	B	A
L	L	L	X0
L	L	L	X1
L	L	H	X2
L	L	H	X3
L	H	L	X4
L	H	L	X5
L	H	H	X6
L	H	H	X7
H	X	X	X
			NONE

X = Don't Care

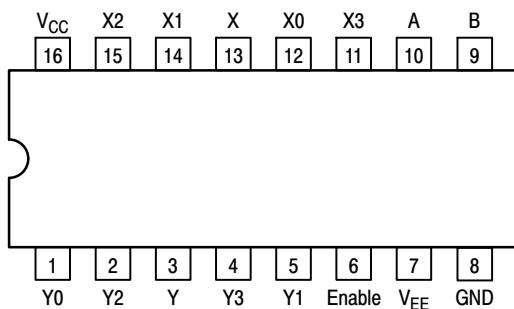


Figure 3. Pinout: MC74VHC4052 (Top View)

## FUNCTION TABLE – MC74VHC4052

Control Inputs			ON Channels
Enable	Select		
	B	A	
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

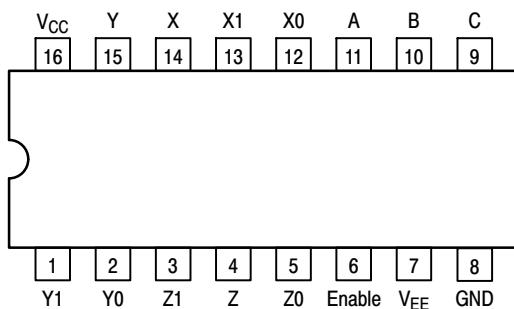


Figure 4. Pinout: MC74VHC4053 (Top View)

## FUNCTION TABLE – MC74VHC4053

Control Inputs			ON Channels
Enable	Select		
	C	B	A
L	L	L	Z0 Y0 X0
L	L	L	Z0 Y0 X1
L	L	H	Z0 Y1 X0
L	L	H	Z0 Y1 X1
L	H	L	Z1 Y0 X0
L	H	L	Z1 Y0 X1
L	H	H	Z1 Y1 X0
L	H	H	Z1 Y1 X1
H	X	X	X
			NONE

X = Don't Care

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	– 0.5 to + 7.0 – 0.5 to + 14.0	V
$V_{EE}$	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
$V_{IS}$	Analog Input Voltage	$V_{EE}$ – 0.5 to $V_{CC}$ + 0.5	V
$V_{in}$	Digital Input Voltage (Referenced to GND)	– 0.5 to $V_{CC}$ + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
$P_D$	Power Dissipation in Still Air SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature Range	– 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C  
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	2.0 2.0	6.0 12.0	V	
$V_{EE}$	Negative DC Supply Voltage, Output (Referenced to GND)	– 6.0	GND	V	
$V_{IS}$	Analog Input Voltage	$V_{EE}$	$V_{CC}$	V	
$V_{in}$	Digital Input Voltage (Referenced to GND)	GND	$V_{CC}$	V	
$V_{IO}^*$	Static or Dynamic Voltage Across Switch		1.2	V	
$T_A$	Operating Temperature Range, All Package Types	– 55	+ 125	°C	
$t_r, t_f$	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 3.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0 0	1000 800 500 400	ns

\*For voltage drops across switch greater than 1.2V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

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## DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$ , Except Where Noted

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
$V_{IL}$	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
$I_{in}$	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0$ V	6.0	± 0.1	± 1.0	± 1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$ $V_{IO} = 0$ V $V_{EE} = -6.0$ V	6.0 6.0	1 4	10 40	40 80	μA

## DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	$V_{CC}$ V	$V_{EE}$ V	Guaranteed Limit			Unit
					-55 to 25°C	≤ 85°C	≤ 125°C	
$R_{on}$	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IS} = V_{CC}$ to $V_{EE}$ $I_S \leq 2.0$ mA (Figures 5 through 11)	3.0 4.5 4.5 6.0	0.0 0.0 -4.5 -6.0	200 160 120 100	240 200 150 125	320 280 170 140	Ω
		$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IS} = V_{CC}$ or $V_{EE}$ (Endpoints) $I_S \leq 2.0$ mA (Figures 5 through 11)	3.0 4.5 4.5 6.0	0.0 0.0 -4.5 -6.0	150 110 90 80	180 140 120 100	230 190 140 115	
$\Delta R_{on}$	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IS} = 1/2 (V_{CC} - V_{EE})$ $I_S \leq 2.0$ mA	3.0 4.5 4.5 6.0	0.0 0.0 -4.5 -6.0	40 20 10 10	50 25 15 12	80 40 18 14	Ω
$I_{off}$	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{IO} = V_{CC} - V_{EE}$ Switch Off (Figure 12)	6.0	-6.0	0.1	0.5	1.0	μA
		Maximum Off-Channel VHC4051 Leakage Current, VHC4052 Common Channel VHC4053	6.0 6.0 6.0	-6.0 -6.0 -6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
$I_{on}$	Maximum On-Channel VHC4051 Leakage Current, VHC4052 Channel-to-Channel VHC4053	$V_{in} = V_{IL}$ or $V_{IH}$ Switch-to-Switch = $V_{CC} - V_{EE}$ ; (Figure 14)	6.0 6.0 6.0	-6.0 -6.0 -6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μA

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AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit		
			-55 to 25°C	≤85°C	≤125°C			
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Channel-Select to Analog Output (Figures 18, 19)	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figures 20, 21)	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable to Analog Output (Figures 22, 23)	2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns		
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable to Analog Output (Figures 22, 23)	2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns		
C <sub>in</sub>	Maximum Input Capacitance, Channel-Select or Enable Inputs		10	10	10	pF		
C <sub>I/O</sub>	Maximum Capacitance (All Switches Off)	Analog I/O Common O/I: VHC4051 VHC4052 VHC4053 Feedthrough	35	35	35	pF		
			130	130	130			
			80	80	80			
			50	50	50			
C <sub>PD</sub>			1.0	1.0	1.0	pF		
			45	80	45			

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Limit*			Unit
					25°C			
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 15)	$f_{in} = 1\text{MHz}$ Sine Wave; Adjust $f_{in}$ Voltage to Obtain 0dBm at $V_{OS}$ ; Increase $f_{in}$ Frequency Until dB Meter Reads -3dB; $R_L = 50\Omega$ , $C_L = 10\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	'51 80 80	'52 95 95	'53 120 120	MHz
—	Off-Channel Feedthrough Isolation (Figure 16)	$f_{in} = \text{Sine Wave}$ ; Adjust $f_{in}$ Voltage to Obtain 0dBm at $V_{IS}$ $f_{in} = 10\text{kHz}$ , $R_L = 600\Omega$ , $C_L = 50\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50			dB
		$f_{in} = 1.0\text{MHz}$ , $R_L = 50\Omega$ , $C_L = 10\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	-40			
—	Feedthrough Noise. Channel-Select Input to Common I/O (Figure 17)	$V_{in} \leq 1\text{MHz}$ Square Wave ( $t_r = t_f = 6\text{ns}$ ); Adjust $R_L$ at Setup so that $I_S = 0\text{A}$ ; Enable = GND $R_L = 600\Omega$ , $C_L = 50\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	25			mV <sub>PP</sub>
		$R_L = 10\text{k}\Omega$ , $C_L = 10\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	35			
—	Crosstalk Between Any Two Switches (Figure 24) (Test does not apply to VHC4051)	$f_{in} = \text{Sine Wave}$ ; Adjust $f_{in}$ Voltage to Obtain 0dBm at $V_{IS}$ $f_{in} = 10\text{kHz}$ , $R_L = 600\Omega$ , $C_L = 50\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50			dB
		$f_{in} = 1.0\text{MHz}$ , $R_L = 50\Omega$ , $C_L = 10\text{pF}$	2.25 4.50 6.00	-2.25 -4.50 -6.00	-60			
THD	Total Harmonic Distortion (Figure 26)	$f_{in} = 1\text{kHz}$ , $R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ $THD = THD_{measured} - THD_{source}$ $V_{IS} = 4.0\text{V}_{PP}$ sine wave $V_{IS} = 8.0\text{V}_{PP}$ sine wave $V_{IS} = 11.0\text{V}_{PP}$ sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10			%

\*Limits not tested. Determined by design and verified by qualification.

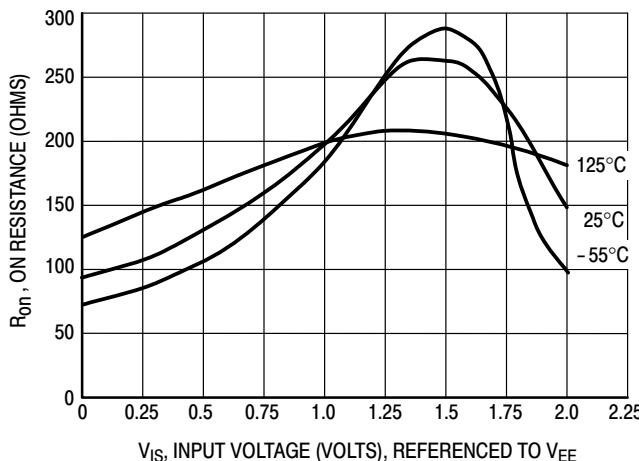


Figure 5. Typical On Resistance,  $V_{CC} - V_{EE} = 2.0\text{ V}$

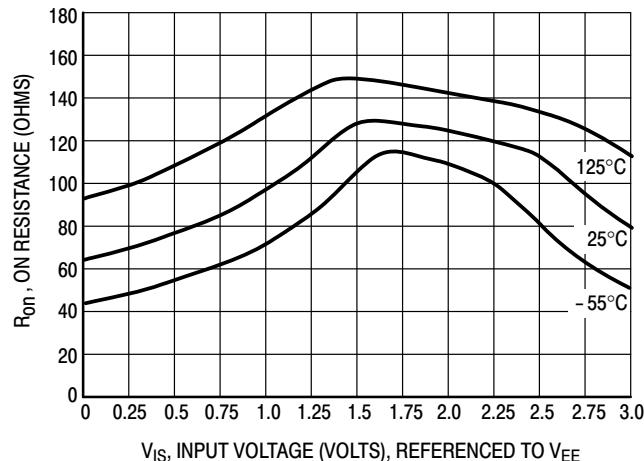


Figure 6. Typical On Resistance,  $V_{CC} - V_{EE} = 3.0\text{ V}$

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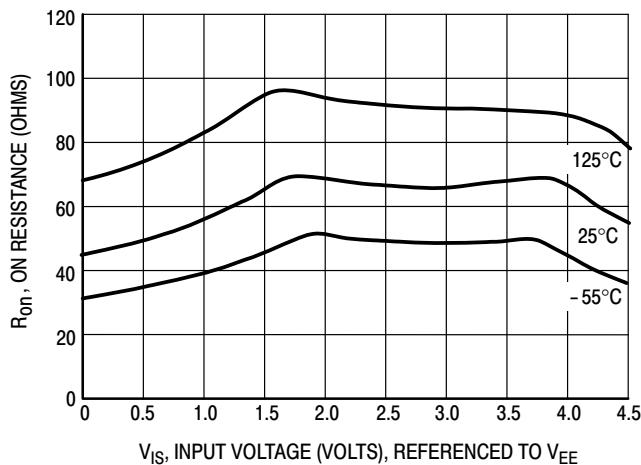


Figure 7. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5$  V

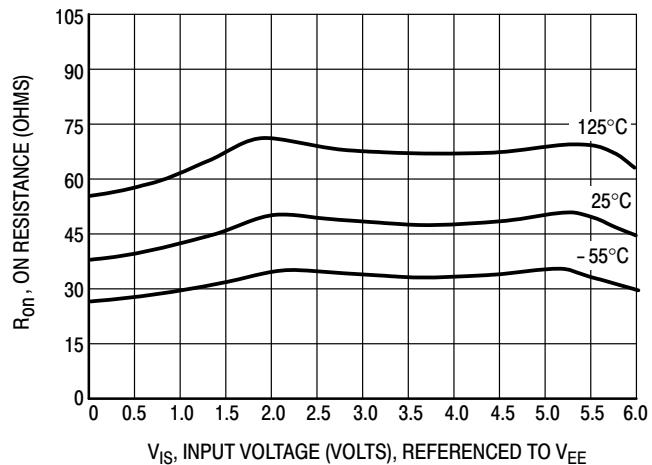


Figure 8. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0$  V

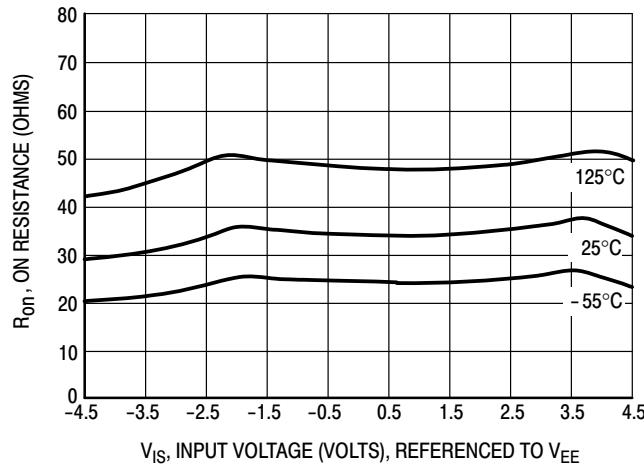


Figure 9. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0$  V

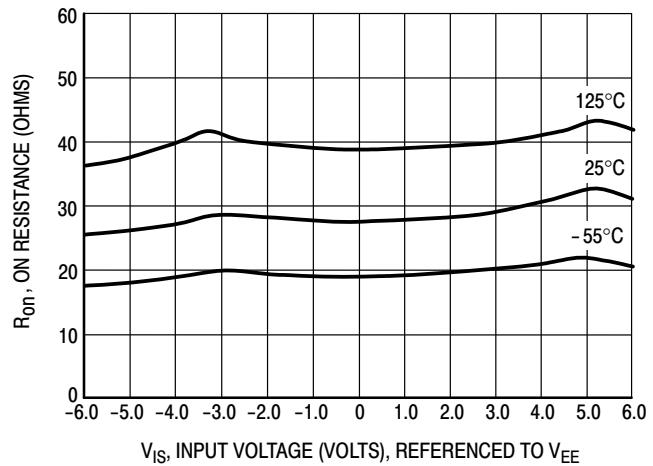


Figure 10. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0$  V

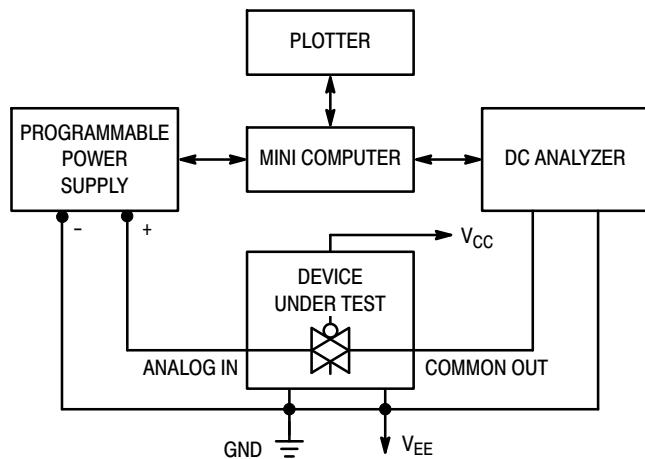


Figure 11. On Resistance Test Set-Up

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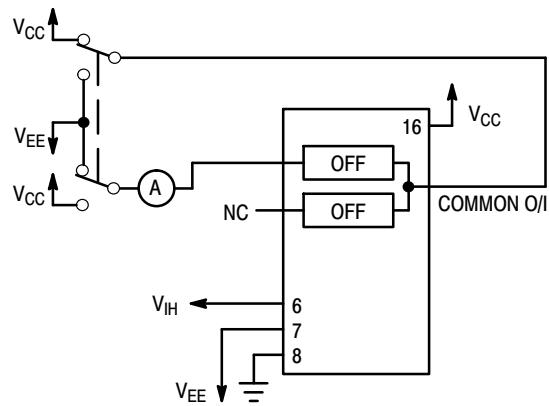


Figure 12. Maximum Off Channel Leakage Current,  
Any One Channel, Test Set-Up

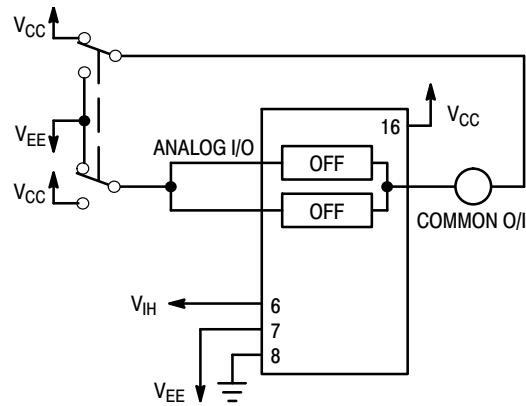


Figure 13. Maximum Off Channel Leakage Current,  
Common Channel, Test Set-Up

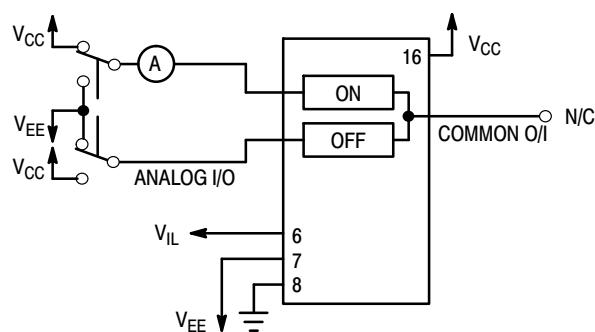


Figure 14. Maximum On Channel Leakage Current,  
Channel to Channel, Test Set-Up

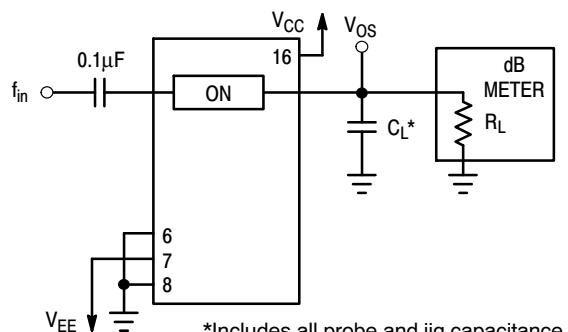


Figure 15. Maximum On Channel Bandwidth,  
Test Set-Up

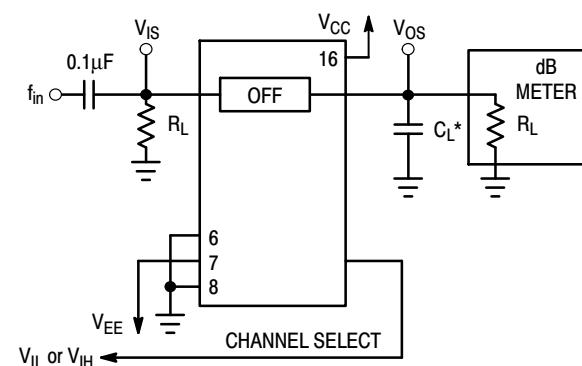


Figure 16. Off Channel Feedthrough Isolation,  
Test Set-Up

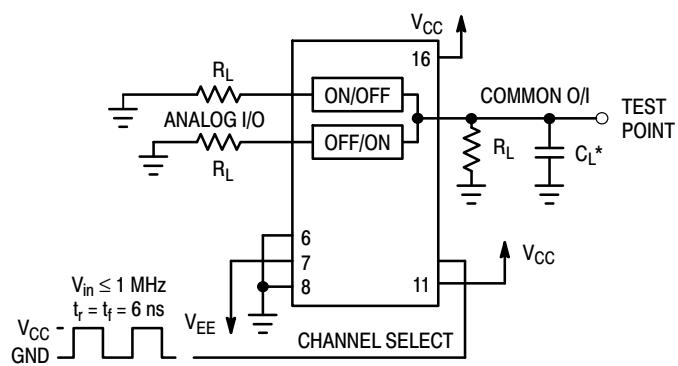


Figure 17. Feedthrough Noise, Channel Select to  
Common Out, Test Set-Up

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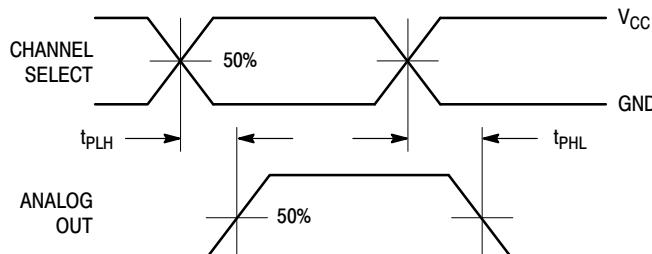
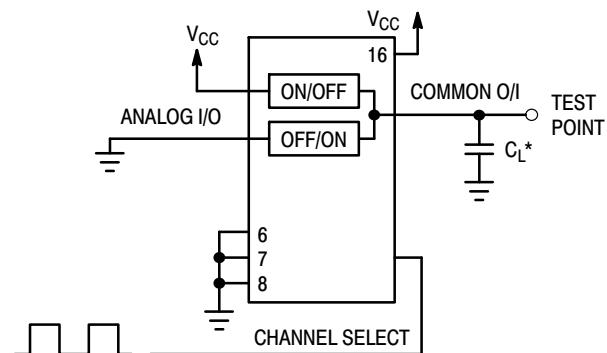


Figure 18. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance

Figure 19. Propagation Delay, Test Set-Up Channel Select to Analog Out

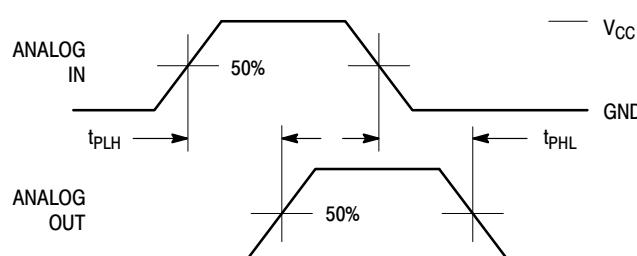
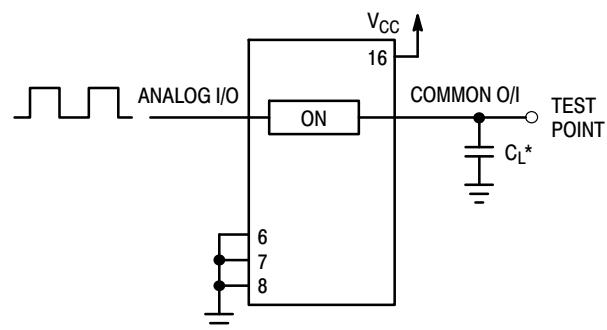


Figure 20. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance

Figure 21. Propagation Delay, Test Set-Up Analog In to Analog Out

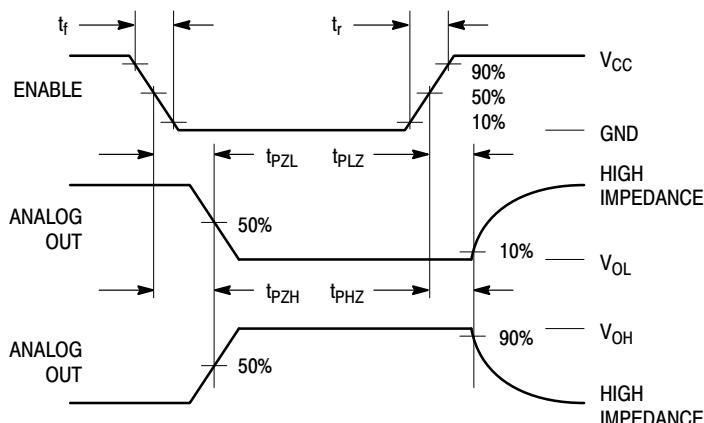


Figure 22. Propagation Delays, Enable to Analog Out

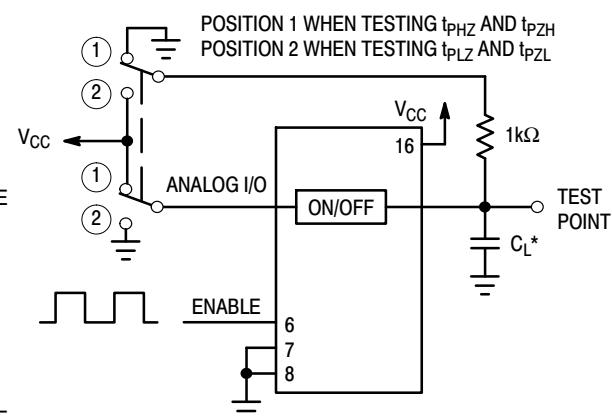
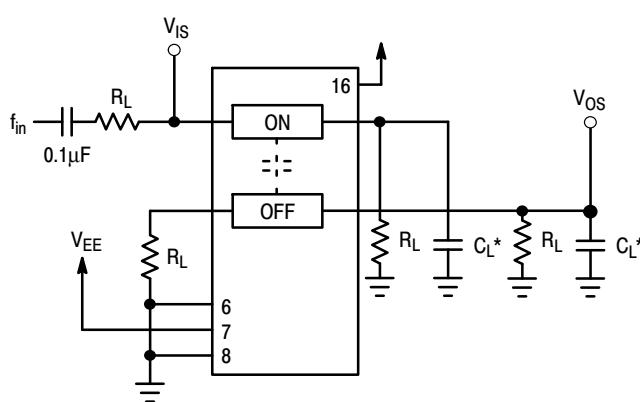
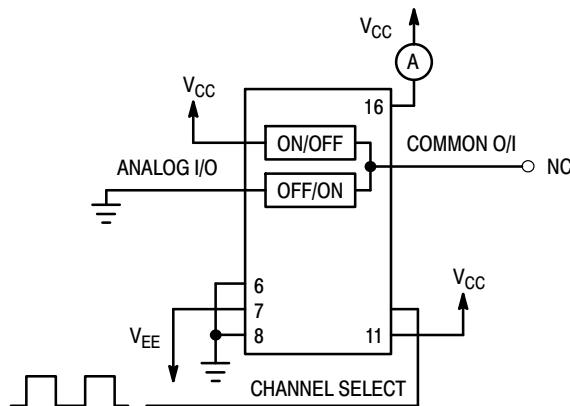


Figure 23. Propagation Delay, Test Set-Up Enable to Analog Out

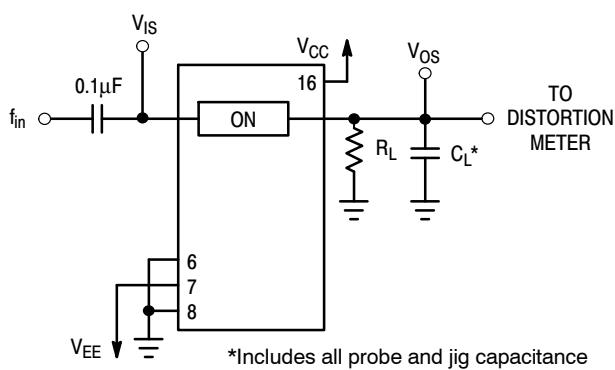


\*Includes all probe and jig capacitance

**Figure 24. Crosstalk Between Any Two Switches, Test Set-Up**

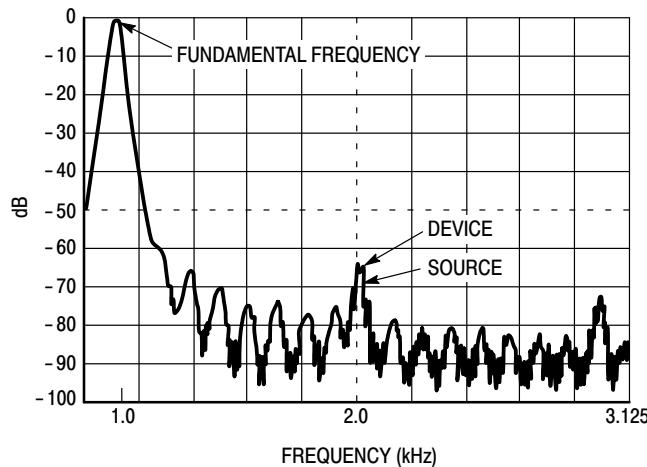


**Figure 25. Power Dissipation Capacitance, Test Set-Up**



\*Includes all probe and jig capacitance

**Figure 26. Total Harmonic Distortion, Test Set-Up**



**Figure 27. Plot, Harmonic Distortion**

## APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V<sub>CC</sub> or GND logic levels. V<sub>CC</sub> being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ V_{EE} &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages V<sub>CC</sub> and V<sub>EE</sub>. The positive peak analog voltage should not exceed V<sub>CC</sub>. Similarly, the negative peak analog voltage should not go below V<sub>EE</sub>. In this example, the difference between V<sub>CC</sub> and V<sub>EE</sub> is ten volts. Therefore, using the configuration of Figure 28, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V<sub>CC</sub> or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - GND &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - GND &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ \text{and } V_{EE} &\leq GND \end{aligned}$$

When voltage transients above V<sub>CC</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external Germanium or Schottky diodes (D<sub>x</sub>) are recommended as shown in Figure 29. These diodes should be able to absorb the maximum anticipated current surges during clipping.

## MC74VHC4051, MC74VHC4052, MC74VHC4053

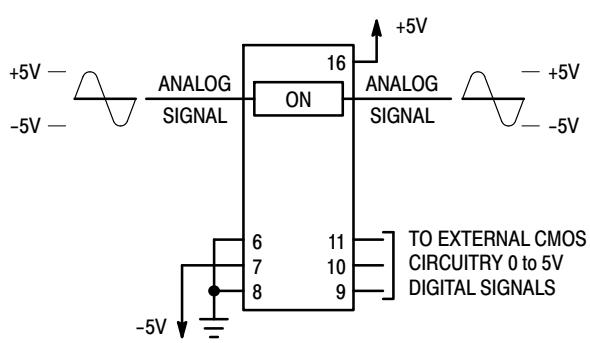


Figure 28. Application Example

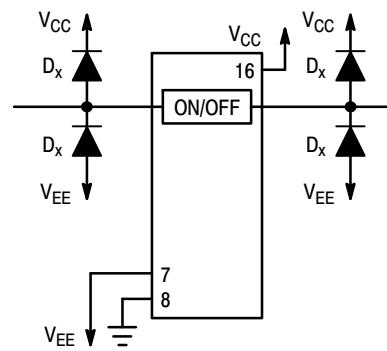
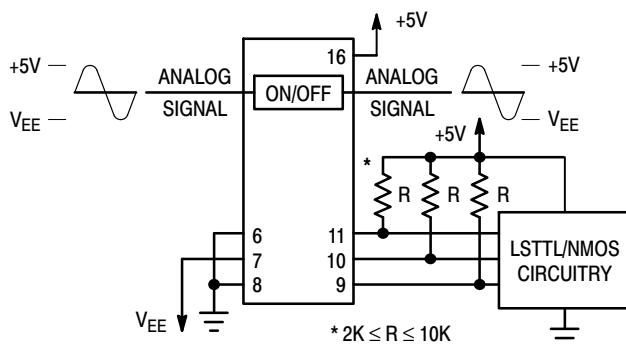
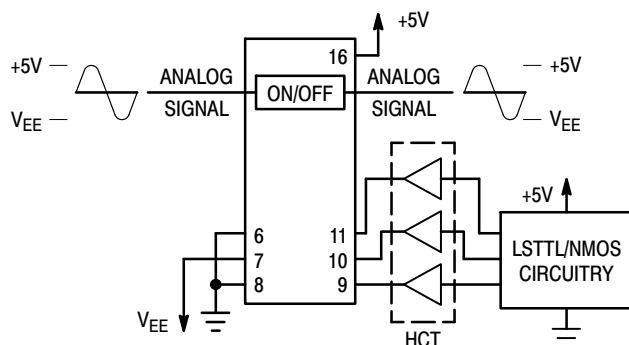


Figure 29. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 30. Interfacing LSTTL/NMOS to CMOS Inputs

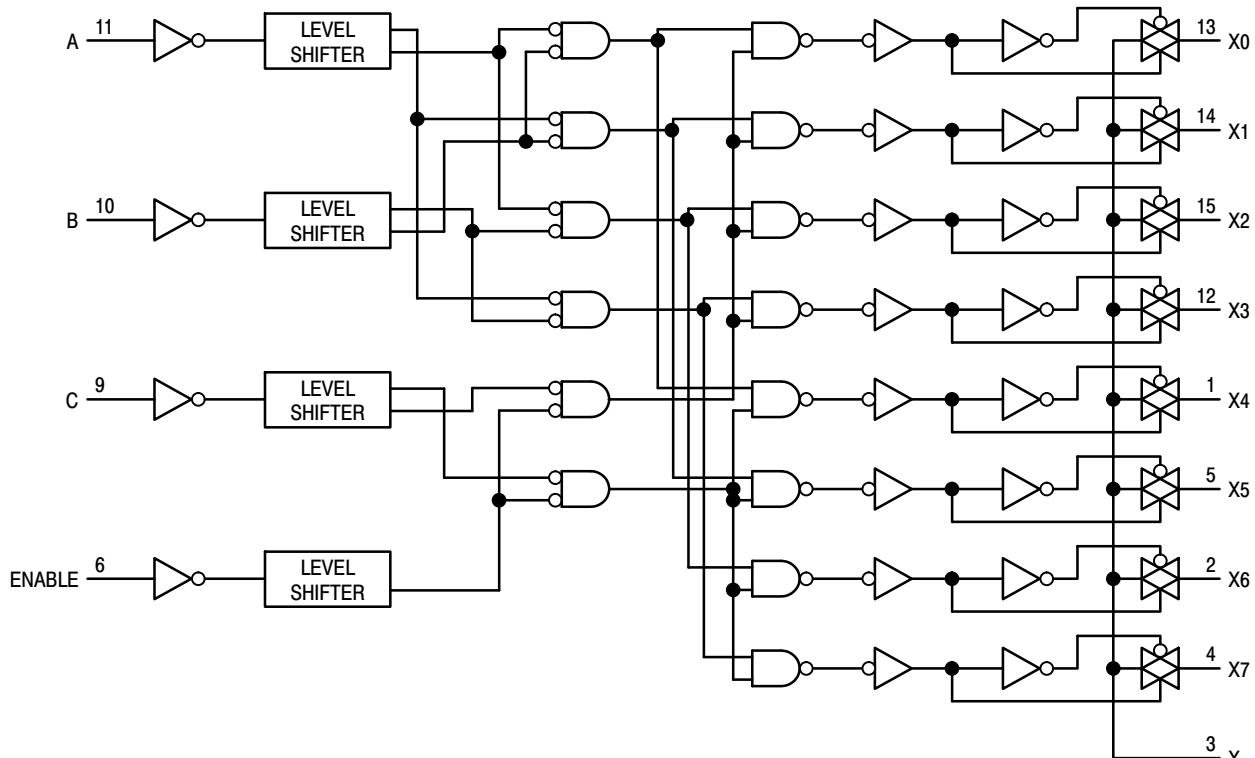


Figure 31. Function Diagram, VHC4051

## MC74VHC4051, MC74VHC4052, MC74VHC4053

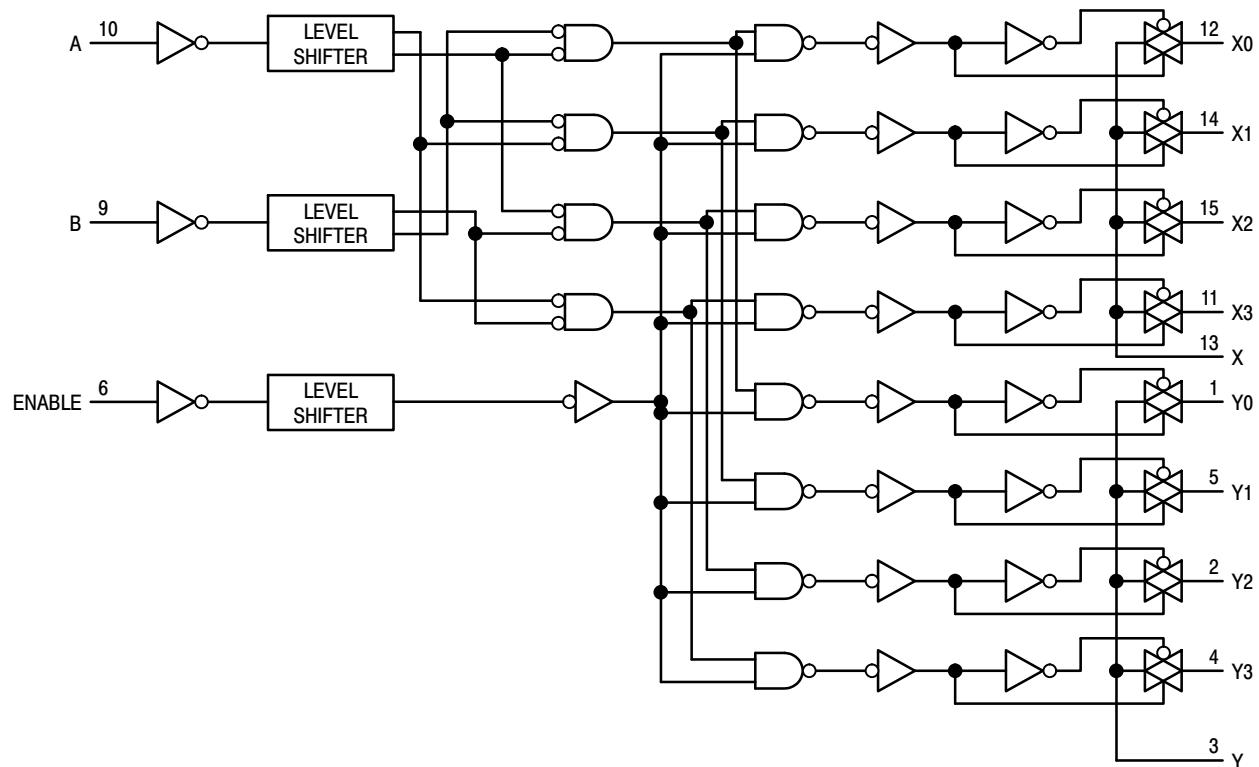


Figure 33. Function Diagram, VHC4052

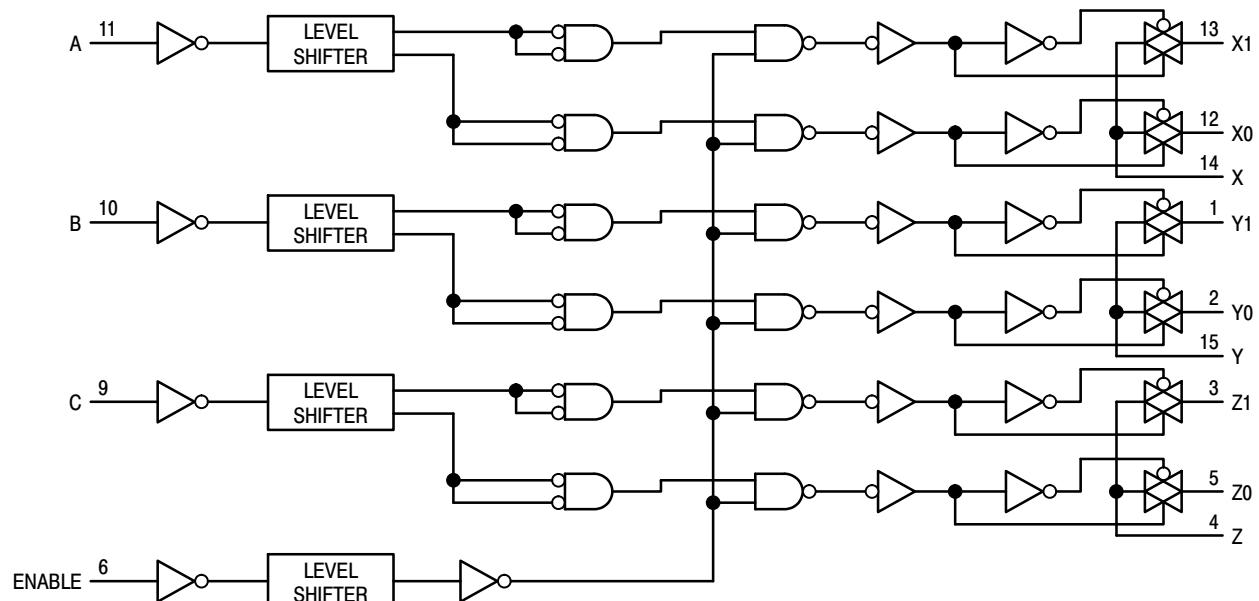


Figure 32. Function Diagram, VHC4053

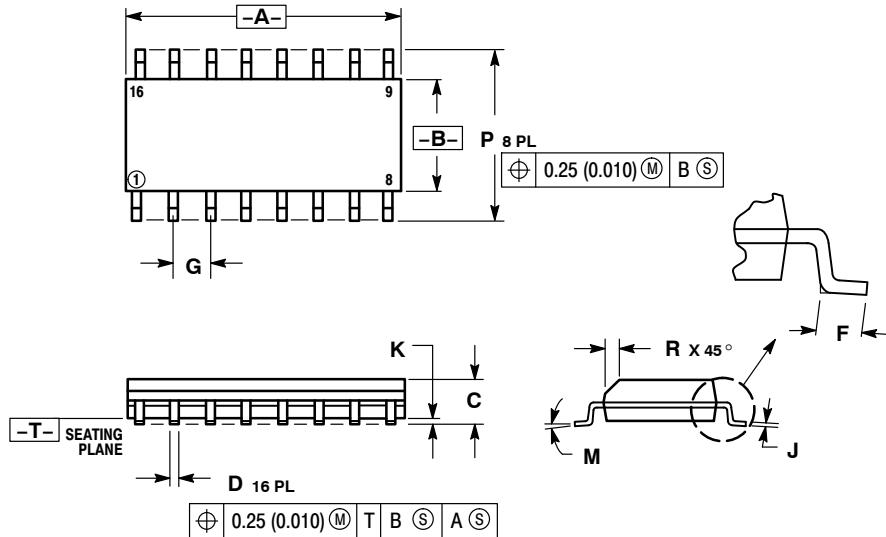
## MC74VHC4051, MC74VHC4052, MC74VHC4053

### ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74VHC4051DR2G	SOIC-16	2500 Units / Tape & Reel
MC74VHC4051DTR2G	TSSOP-16	2500 Units / Tape & Reel
MC74VHC4052DR2G	SOIC-16	2500 Units / Tape & Reel
MC74VHC4052DTR2G	TSSOP-16	2500 Units / Tape & Reel
MC74VHC4053DR2G	SOIC-16	2500 Units / Tape & Reel
MC74VHC4053DTR2G	TSSOP-16	2500 Units / Tape & Reel
MC74VHC4051MG	SOEIAJ-16	50 Units / Rail
MC74VHC4052MG	SOEIAJ-16	50 Units / Rail
MC74VHC4052MELG	SOEIAJ-16	2000 Units / Reel
MC74VHC4053MG	SOEIAJ-16	50 Units / Rail

PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

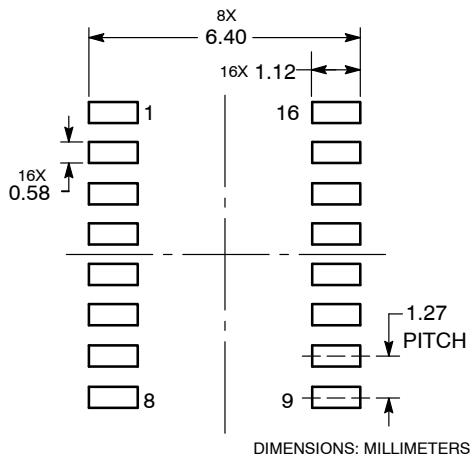


NOTES:

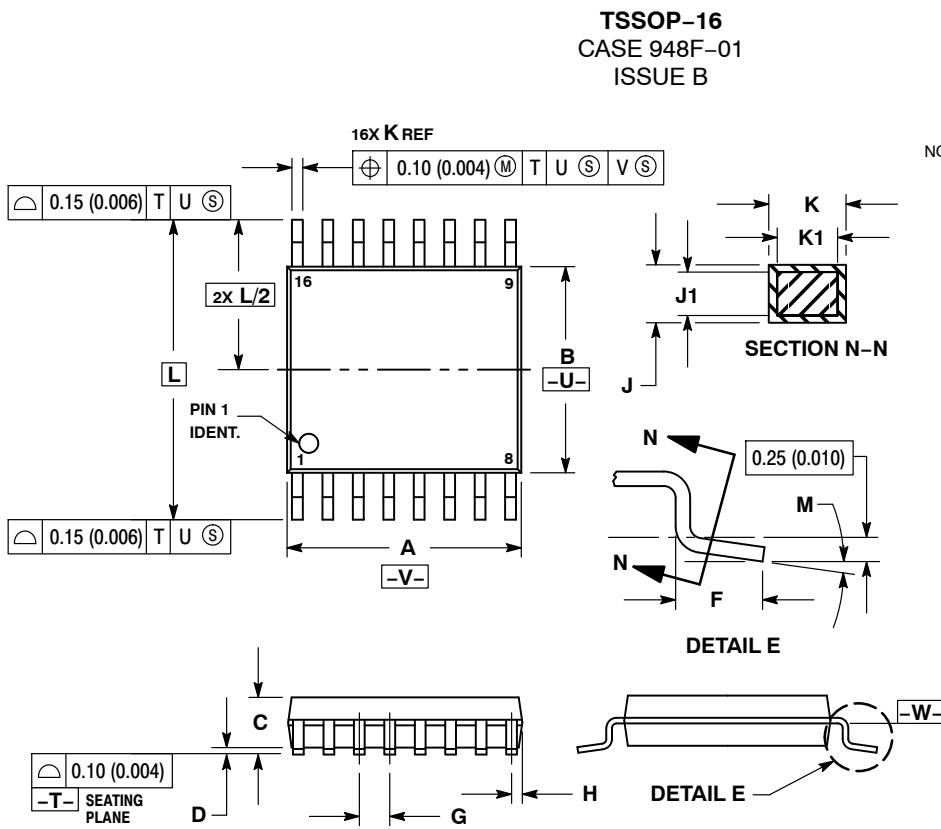
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

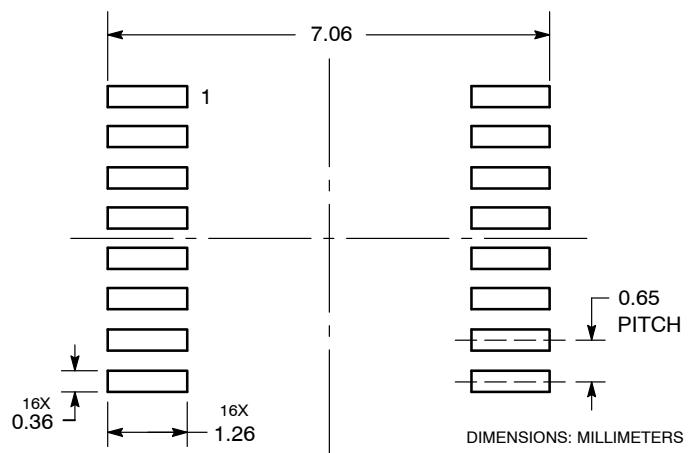


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

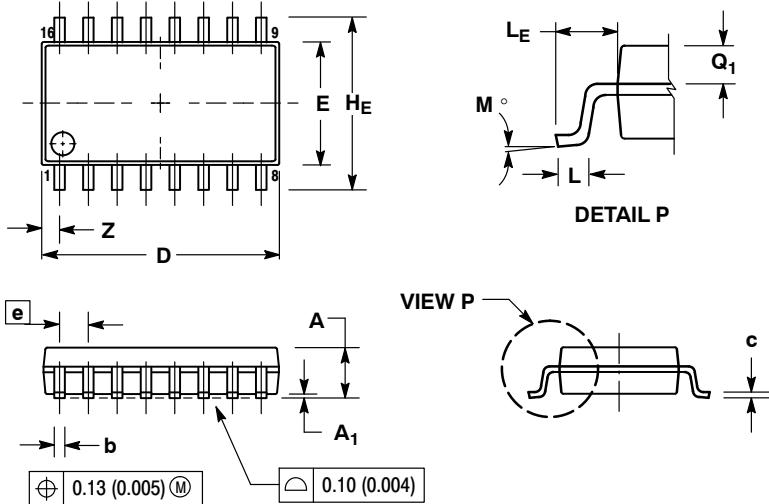
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



## PACKAGE DIMENSIONS

SOEIAJ-16  
CASE 966-01  
ISSUE A



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC	1.27 BSC	0.050 BSC	0.050 BSC
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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