CY29947

2.5V or 3.3V, 200-MHz, 1:9 Clock Distribution Buffer

Features

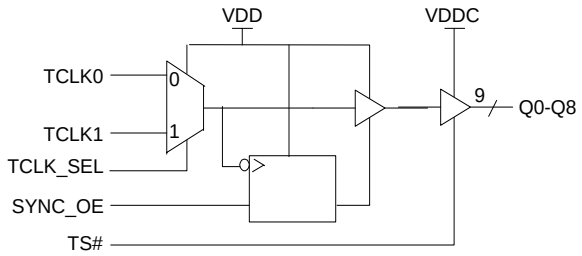
- **2.5V or 3.3V operation**
- **200-MHz clock support**
- **LVCMOS-/LVTTL-compatible inputs**
- **9 clock outputs: drive up to 18 clock lines**
- **Synchronous Output Enable**
- **Output three-state control**
- **250 ps max. output-to-output skew**
- **Pin compatible with MPC947, MPC9447**
- **Available in Industrial and Commercial temp. range**
- **32-pin TQFP package**

Description

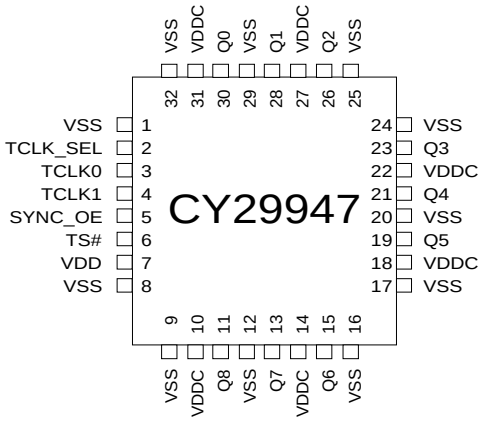
The CY29947 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible clock inputs. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The 9 outputs are LVCMOS or LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines.For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:18. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the CY29947 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The CY29947 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
3	TCLK0		I, PU	**Test Clock Input**
4	TCLK1		I, PU	**Test Clock Input**
2	TCLK_SEL		I, PU	**Test Clock Select Input**. When LOW, TCLK0 is selected. When asserted HIGH, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q(8:0)	VDDC	O	**Clock Outputs**
5	SYNC_OE		I, PU	**Output Enable Input**. When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	**Three-state Control Input**. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 27, 31	VDDC			**3.3V or 2.5V Power Supply for Output Clock Buffers**
7	VDD			**3.3V or 2.5V Power Supply**
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	VSS			**Common Ground**

Note:
1. PD = internal pull-down, PU = internal pull-up.

Output Enable/Disable

The CY29947 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in *Figure 1*.

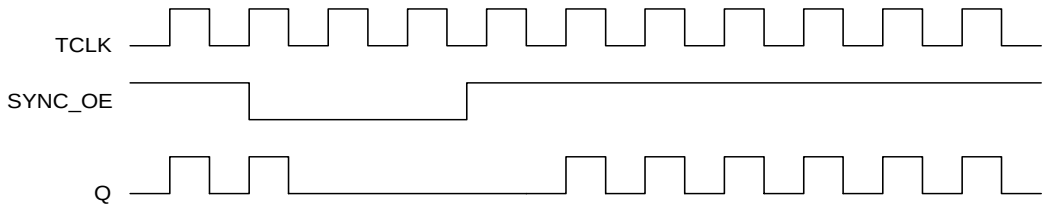


Figure 1. SYNC_OE Timing Diagram

Maximum Ratings [2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: ..... –65°C to + 150°C
Operating Temperature: ..... –40°C to +85°C
Maximum ESD protection 2kV
Maximum Power Supply: 5.5V
Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, Over the specified temperature range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[3]				–100	µA
I_{IH}	Input High Current[3]				10	µA
V_{OL}	Output Low Voltage[4]	I_{OL} = 20 mA			0.4	V
V_{OH}	Output High Voltage[4]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5			V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF		120		mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF		200		
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF		85		
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF		140		
Zout	Output Impedance	V_{DD} = 3.3V	12	15	18	Ω
		V_{DD} = 2.5V	14	18	22	
C_{in}	Input Capacitance			4		pF

Notes:
2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters[5]**:** $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, Over the specified temperature range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[6]	V_{DD} = 3.3V			200	MHz
		V_{DD} = 2.5V			170	
Tpd	TCLK To Q Delay[6]	V_{DD} = 3.3V	4.75		9.25	ns
		V_{DD} = 2.5V	6.50		10.50	
FoutDC	Output Duty Cycle[6, 7]	Measured at $V_{DD}/2$	45		55	%
tpZL, tpZH	Output Enable Time (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[6, 8]			150	250	ps
Tskew(pp)	Part-to-Part Skew[9]				2.0	ns
Ts	Set-up Time[6, 10]	SYNC_OE to TCLK	0.0			ps
Th	Hold Time[6, 10]	TCLK to SYNC_OE	1.0			ps
Tr/Tf	Output Clocks Rise/Fall Time[8]	0.8V to 2.0V, V_{DD} = 3.3V	0.20		1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.20		1.3	

Notes:

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. 50% input duty cycle.
8. See *Figure 2*.
9. Part-to-Part skew at a given temperature and voltage.
10. Set-up and hold times are relative to the falling edge of the input clock

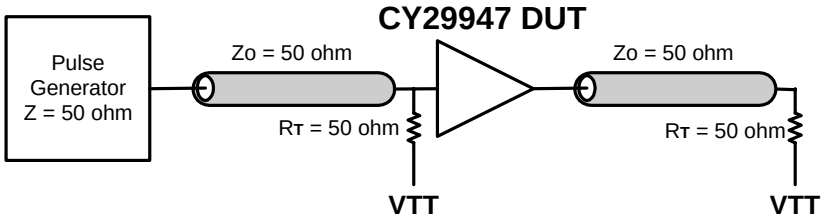


Figure 2. LVCMOS_CLK CY29947 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

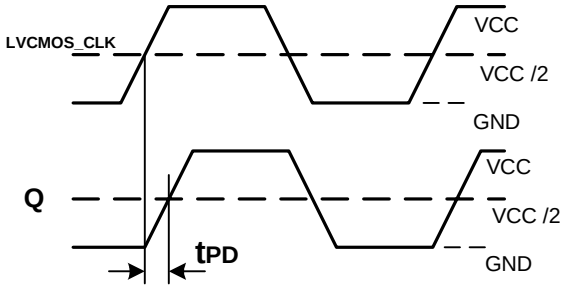


Figure 3. LVCMOS Propagation Delay (TPD) Test Reference

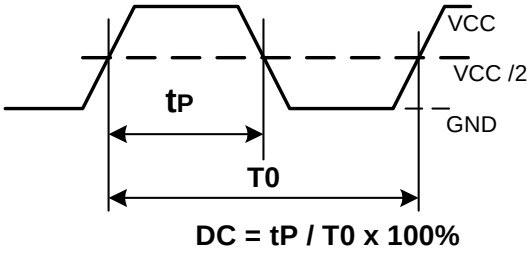


Figure 4. Output Duty Cycle (FoutDC)

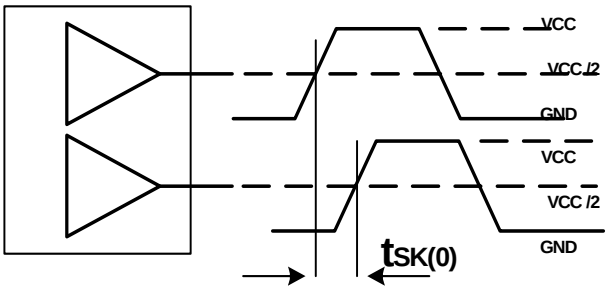


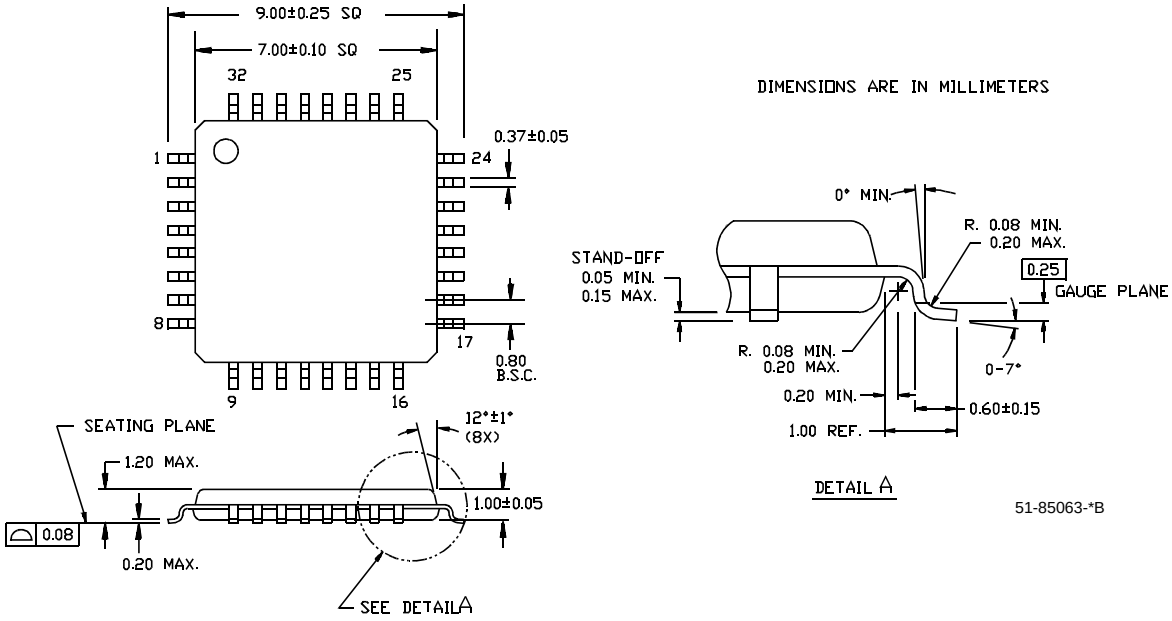
Figure 5. Output-to-Output Skew tsk(0).

Ordering Information

Part Number	Package Type	Production Flow
CY29947AI	32 Pin TQFP	Industrial, –40°C to +85°C
CY29947AIT	32 Pin TQFP - Tape and Reel	Industrial, –40°C to +85°C
CY29947AC	32 Pin TQFP	Commercial, 0°C to +70°C
CY29947ACT	32 Pin TQFP - Tape and Reel	Commercial, 0°C to +70°C

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32



Revision History

Document Title: CY29947 2.5V or 3.3V, 200-MHz, 1:9 Clock Distribution Buffer Document Number: 38-07287				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111098	02/07/02	BRK	New data sheet
*A	116781	08/14/02	HWT	Added Commercial Temperature Range in the ordering information
*B	118462	09/09/02	HWT	Corrected the Package Drawing and Dimension in page 6 from 32 LQFP to 32 TQFP
*C	122879	12/22/02	RBI	Added power up requirements to Maximum Ratings