# DATA SHEET

## 74F109

## Positive J-$\overline{K}$ positive edge-triggered flip-flops

Product specification

1990 Oct 23

IC15 Data Handbook

Philips
Semiconductors

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# Postive J-$\overline{K}$ positive edge-triggered flip-flops 74F109

## FEATURE

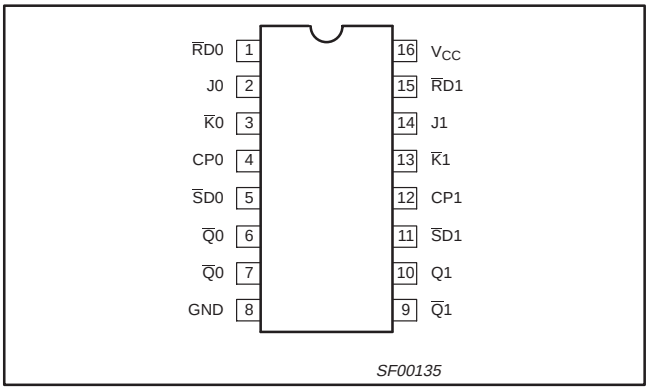
- Industrial temperature range available (–40°C to +85°C)

## DESCRIPTION

The 74F109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input. The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

| TYPE | TYPICAL $f_{max}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F109 | 125MHz | 12.3mA |

## PIN CONFIGURATION




SF00135

## ORDERING INFORMATION

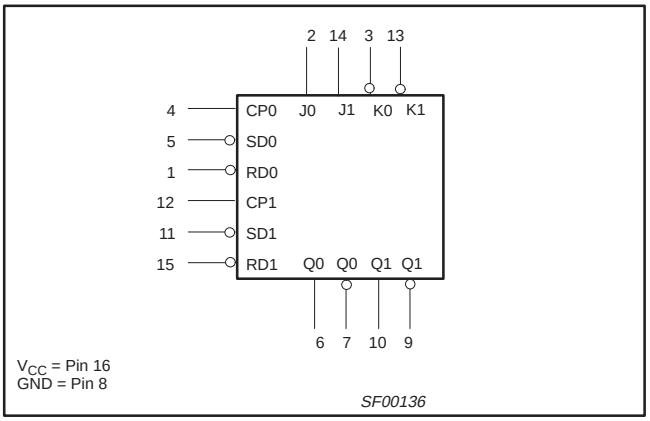
| DESCRIPTION | ORDER CODE | | PKG DWG # |
|---|---|---|---|
| | COMMERCIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = 0°C to +70°C | INDUSTRIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = –40°C to +85°C | |
| 16-pin plastic DIP | N74F109N | I74F109N | SOT38-4 |
| 16-pin plastic SO | N74F109D | I74F109D | SOT109-1 |

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| J0, J1 | J inputs | 1.0/1.0 | 20µA/0.6mA |
| $\overline{K}$0, $\overline{K}$1 | K inputs | 1.0/1.0 | 20µA/0.6mA |
| CP0, CP1 | Clock inputs (active rising edge) | 1.0/1.0 | 20µA/0.6mA |
| $\overline{SD}$0, $\overline{SD}$1 | Set inputs (active Low) | 1.0/3.0 | 20µA/1.8mA |
| $\overline{RD}$0, $\overline{RD}$1 | Reset inputs (active Low) | 1.0/3.0 | 20µA/1.8mA |
| Q0, Q1, $\overline{Q}$0, $\overline{Q}$1 | Data outputs | 50/33 | 1.0mA/20mA |

**NOTE:** One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL

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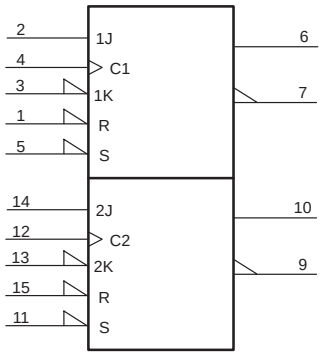
## IEC/IEEE SYMBOL

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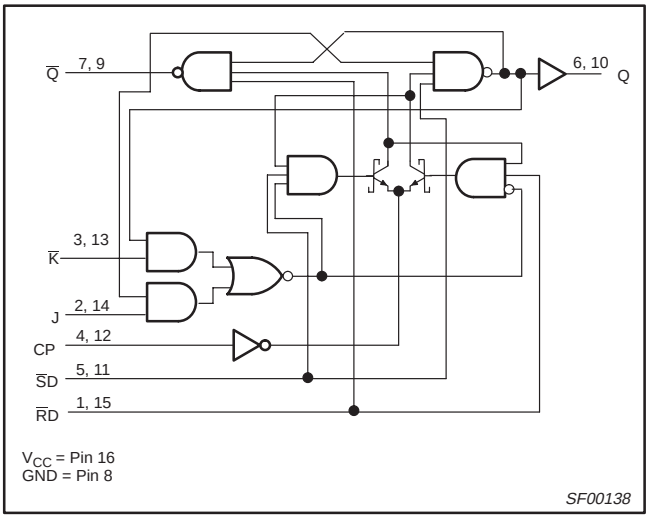
## LOGIC DIAGRAM




## FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|---|
| $\overline{SD}$ | $\overline{RD}$ | CP | J | $\overline{K}$ | Q | $\overline{Q}$ | |
| L | H | X | X | X | H | L | Asynchronous set |
| H | L | X | X | X | L | H | Asynchronous reset |
| L | L | X | X | X | H | H | Undetermined* |
| H | H | ↕ | X | X | q | $\overline{q}$ | Hold |
| H | H | ↑ | h | l | $\overline{q}$ | q | Toggle |
| H | H | ↑ | h | h | H | L | Load "1" (set) |
| H | H | ↑ | l | l | L | H | Load "0" (reset) |
| H | H | ↑ | l | h | q | $\overline{q}$ | Hold 'no change" |

**NOTES:**
H = High-voltage level
h = High-voltage level one setup time prior to low-to-high clock transition
L = Low-voltage level
l = Low-voltage level one setup time prior to low-to-high clock transition
q = Lower case indicate the state of the referenced output prior to the low-to-high clock transition
X = Don't care
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition
* = Both outputs will be high if both $\overline{SD}$ and $\overline{RD}$ go low simultaneously

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | | –0.5 to +7.0 | V |
| $I_{IN}$ | Input current | | –30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | | –0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | | 40 | mA |
| $T_{amb}$ | Operating free-air temperature range | Commercial range | 0 to +70 | °C |
| | | Industrial range | –40 to +85 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{IN}$ | High-level input voltage | | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | | –1 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | mA |
| $T_{amb}$ | Operating free-air temperature range | Commercial range | 0 | | +70 | °C |
| | | Industrial range | –40 | | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS[1] | | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP[2] | MAX | |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OH}$ = MAX | ±10%$V_{CC}$ | 2.5 | | | V |
| | | | | | ±5%$V_{CC}$ | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = MAX | ±10%$V_{CC}$ | | 0.30 | 0.50 | V |
| | | | | | ±5%$V_{CC}$ | | 0.30 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | | –0.73 | –1.2 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 7.0V | | | | | 100 | µA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | | 20 | µA |
| $I_{IL}$ | Low-level input current | J, $\overline{K}$, CPn | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | | | –0.6 | mA |
| | | $\overline{S}$Dn, $\overline{R}$Dn | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | | | –1.8 | mA |
| $I_{OS}$ | Short-circuit output current[3] | | $V_{CC}$ = MAX | | | -60 | | –150 | mA |
| $I_{CC}$ | Supply current[4] (total) | | $V_{CC}$ = MAX | | | | 12.3 | 17 | mA |

**NOTES:**

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = 25°C.
3. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.
4. Measure $I_{CC}$ with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

## AC ELECTRICAL CHARACTERISTICS

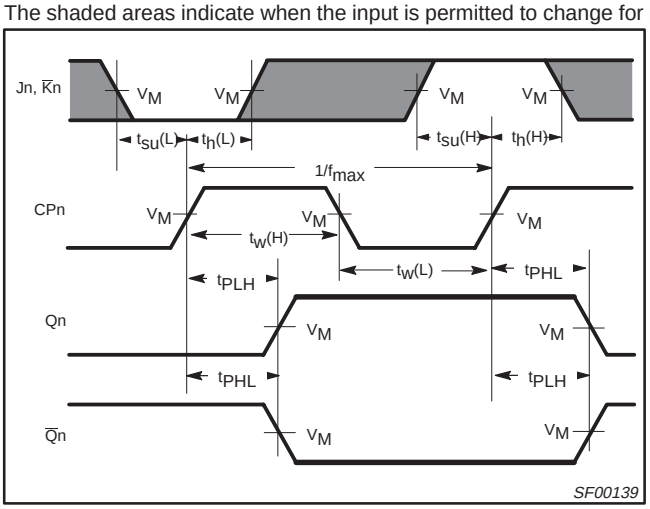
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = +5.0V $T_{amb}$ = +25°C $C_L$ = 50pF $R_L$ = 500Ω | | | $V_{CC}$ = +5.0V ± 10% $T_{amb}$ = 0°C to +70°C $C_L$ = 50pF $R_L$ = 500Ω | | $V_{CC}$ = +5.0V ± 10% $T_{amb}$ = –40°C to +85°C $C_L$ = 50pF $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{MAX}$ | Maximum clock frequency | Waveform 1 | 90 | 125 | | 90 | | 90 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CPn to Qn or $\overline{Q}$n | Waveform 1 | 3.8<br>4.4 | 5.3<br>6.2 | 7.0<br>8.0 | 3.8<br>4.4 | 8.0<br>9.2 | 3.8<br>4.4 | 9.0<br>9.2 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{S}$Dn, $\overline{R}$D to Qn or $\overline{Q}$n | Waveform 2, 3 | 3.2<br>3.5 | 5.2<br>7.0 | 7.0<br>9.0 | 3.2<br>3.5 | 8.0<br>10.5 | 2.8<br>3.5 | 9.0<br>10.5 | ns |

## AC SETUP REQUIREMENTS

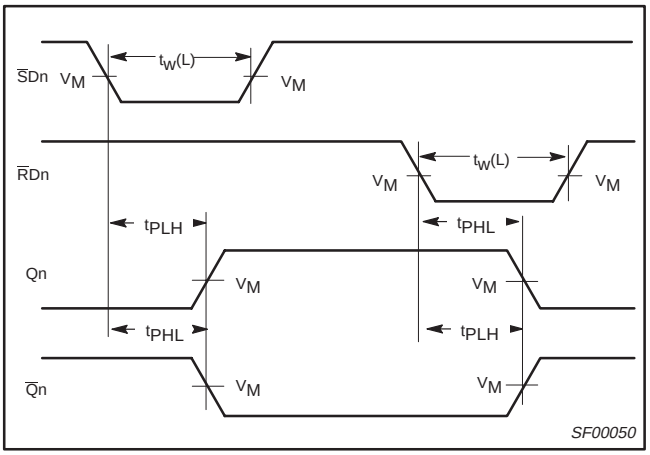
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = +5.0V $T_{amb}$ = +25°C $C_L$ = 50pF $R_L$ = 500Ω | | | $V_{CC}$ = +5.0V ± 10% $T_{amb}$ = 0°C to +70°C $C_L$ = 50pF $R_L$ = 500Ω | | $V_{CC}$ = +5.0V ± 10% $T_{amb}$ = –40°C to +85°C $C_L$ = 50pF $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{su}$ (H)<br>$t_{su}$(L) | Setup time, high or low<br>Dn to CPn | Waveform 1 | 3.0<br>3.0 | | | 3.0<br>3.0 | | 3.0<br>3.0 | | ns |
| $t_h$ (H)<br>$t_h$ (L) | Hold time, high or low<br>Dn to CPn | Waveform 1 | 1.0<br>1.0 | | | 1.0<br>1.0 | | 1.0<br>1.0 | | ns |
| $t_w$ (H)<br>$t_w$ (L) | CP pulse width,<br>high or low | Waveform 1 | 4.0<br>5.0 | | | 4.0<br>5.0 | | 4.0<br>5.0 | | ns |
| $t_w$ (L) | $\overline{S}$Dn or $\overline{R}$Dn pulse width,<br>low | Waveform 2 | 4.0 | | | 4.0 | | 4.0 | | ns |
| $t_{rec}$ | Recovery time<br>$\overline{S}$Dn or $\overline{R}$Dn to CP | Waveform 3 | 2.0 | | | 2.0 | | 2.0 | | ns |

## AC WAVEFORMS

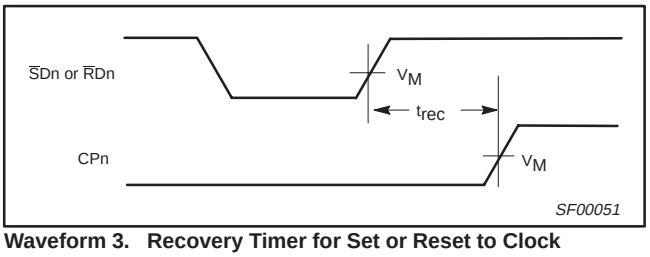
For all waveforms, $V_M$ = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.




**Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width,and Maximum Clock Frequency**

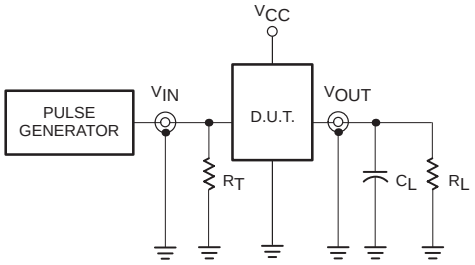



**Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width**

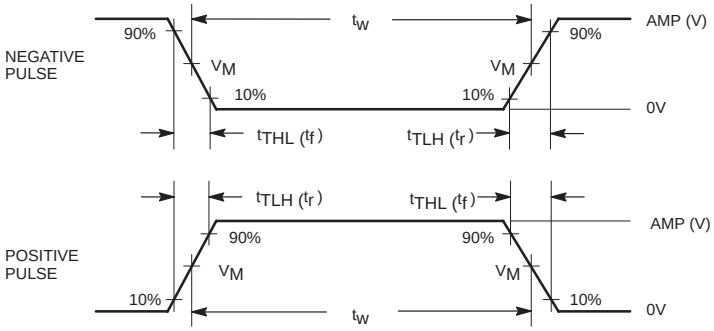



**Waveform 3. Recovery Timer for Set or Reset to Clock**

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for Totem-Pole Outputs**




**DEFINITIONS:**

$R_L$ = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

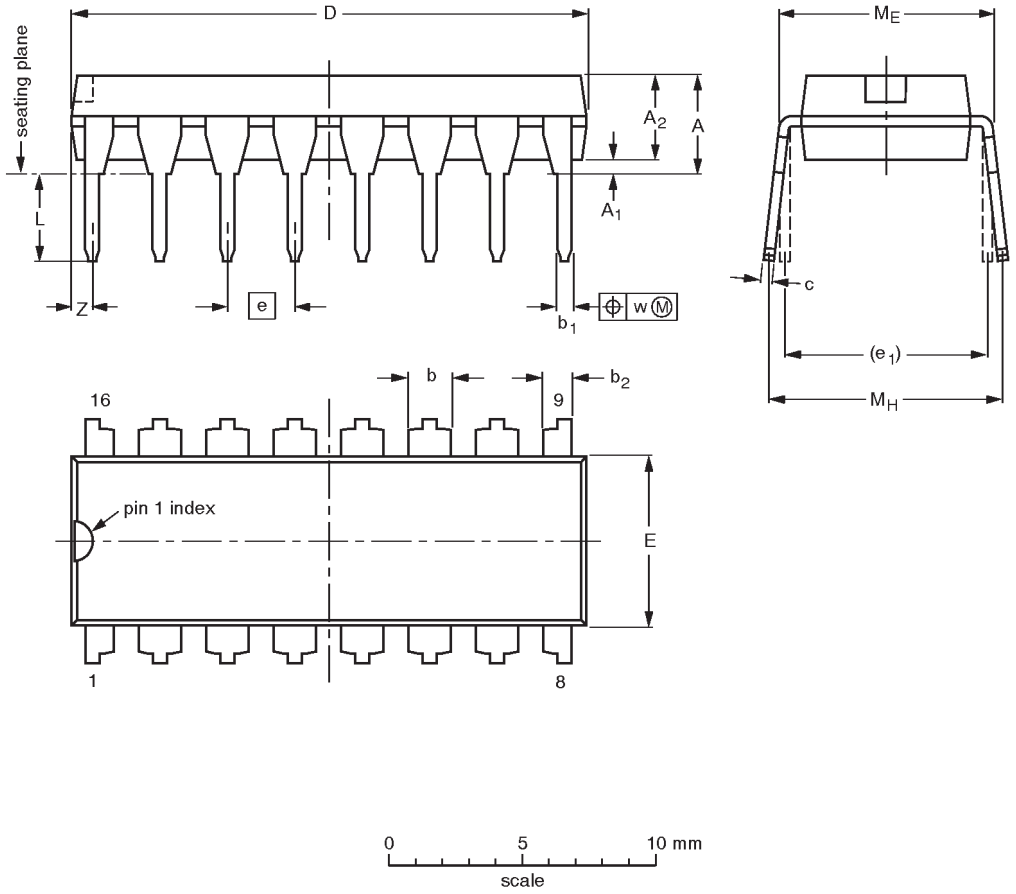
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

**Input Pulse Definition**

| family | INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|---|
| | amplitude | $V_M$ | rep. rate | $t_w$ | $t_{TLH}$ | $t_{THL}$ |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

*SF00006*

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

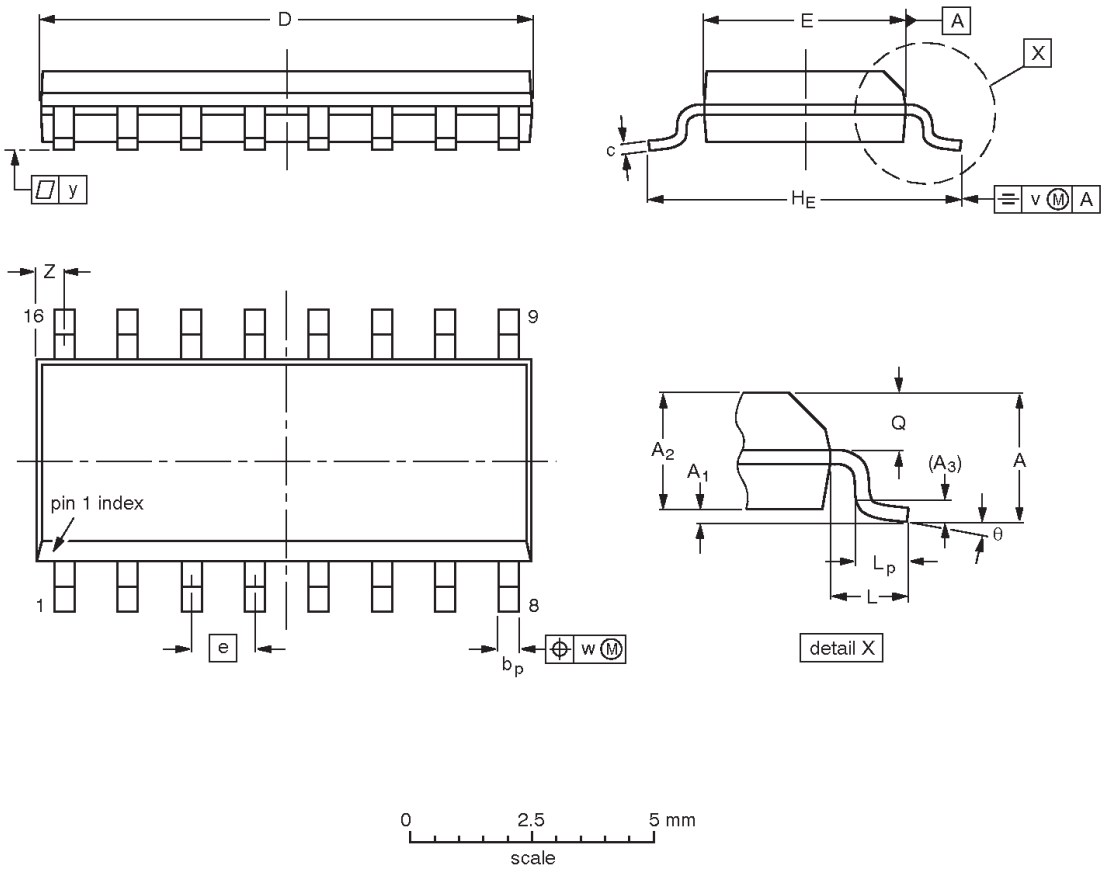
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.030 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-4 | | | | | | ~~92-11-17~~<br>95-01-14 |

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | ~~95-01-23~~<br>97-05-22 |

**NOTES**

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code Date of release: 10-98

Document order number: 9397-750-05069

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