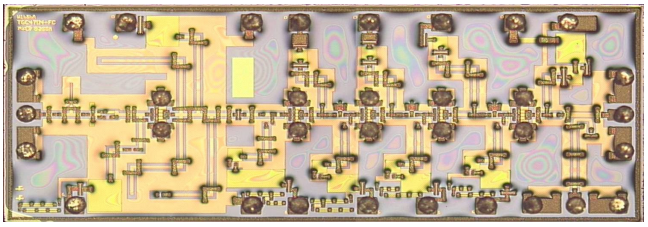
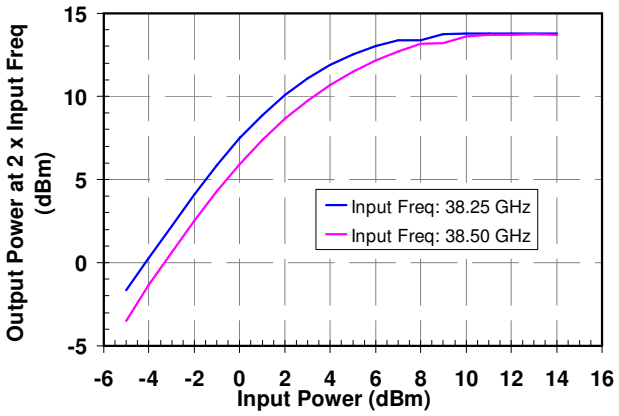
TGC4704-FC

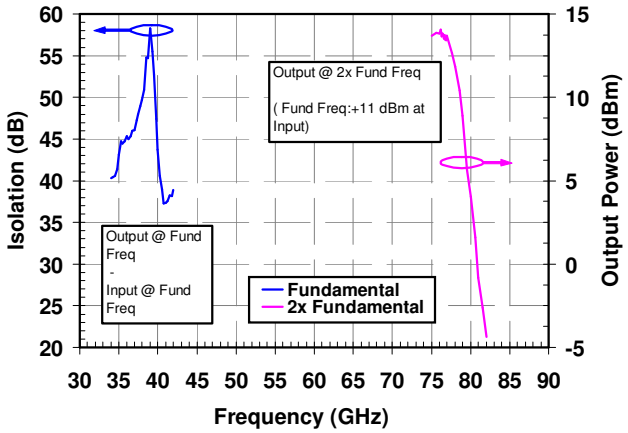
38 to 77 GHz Doubler and Medium Power Amplifier



Measured Performance

Bias conditions: Vd = 4.0 V, Vg1 = -0.4 V, Vg2= 0.2 V,
Idq = 180 mA Typical





Key Features

- RF Output Frequency Range: 76–77 GHz
- Input Frequency Range: 38.0–38.5 GHz
- Two outputs – Out1 (Main) and Out2 (12 dB coupled from Out1)
- 14 dBm saturated Output Power
- 5 dB Conversion Gain
- 50 dB Input Frequency Isolation at output
- Input Return Loss > 8 dB
- Output Return Loss > 10 dB
- Bias: Vd = 3.75 V, Idq = 180 mA, Vg1 = -0.4 V Vg2 = +0.2 V Typical
- Technology: 0.13 um pHEMT with front-side Cu/Sn pillars
- Chip Dimensions: 3.38 x 1.37 x 0.38 mm

Primary Applications

- Automotive Radar
- E-Band Communication

Product Description

The TriQuint TGC4704-FC is a flip-chip frequency doubler. It combines an output medium power amplifier and a frequency doubler at frequencies in the automotive radar frequency band. The TGC4704-FC is designed using TriQuint's proven 0.13 µm pHEMT process and front-side Cu / Sn pillar technology for simplified assembly and low interconnect inductance. Die reliability is enhanced by using TriQuint's BCB polymeric passivation process.

The TGC4704-FC typically provides 14 dBm saturated output power with 5 dB conversion gain.

Lead-free and RoHS compliant.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	5.5 V	
Vd	Drain Voltage	4.0 V	
Vg	Gate Voltage Range	-1 to + 0.45 V	
Id	Drain Current	330 mA	
Ig	Gate Current Range	-0.5 to +3.0 mA	
Pin	Input Continuous Wave Power	16 dBm	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value
Vd	Drain Voltage	3.75 V
Idq	Drain Current, No RF signal at Input	180 mA
Id	Drain Current, RF signal at Input	240 mA
Vg1	Multiplier Stage Gate Voltage	-0.4 V
Vg2a thru Vg2d	Amplifier Stages Gate Voltage	+0.2 V

1/ See electrical schematic diagram for bias instructions.

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Table III
RF Characterization Table

Bias: Vd = 3.75 V V, Idq = 180 mA, Vg1 = -0.4 V, Vg2 = +0.2 V Typical

SYMBOL	PARAMETER	TEST CONDITIONS	MINIMUM	NOMINAL	UNITS
IRL	Input Return Loss	Fin = 38.0 – 38.5 GHz		8	dB
ORL	Output Return Loss	Fin = 76.0 – 77.0 GHz		10	dB
Pout	Output Power (Pin = 8 dBm)	Fin = 38.5 GHz Fout = 77 GHz	11.5	12.5	dBm
Pout	Output Power (Pin = 10 dBm)	Fin = 38.5 GHz Fout = 77 GHz	13.0	14.0	dBm
Isol	Isolation	Fin = 38.0 – 38.5 GHz Fout = 38.0 – 38.5 GHz		50	dB

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Table IV
Power Dissipation and Thermal Properties

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 128.8 °C	Pd = 1.2 W Tchannel = 150 °C Tm = 2.4E+7 Hrs	1/ 2/ 3/
Thermal Resistance, θjc	Vd = 4.0 V Vg1 = -0.4 V Vg2 = +0.2 V Id = 0.240 A Pd = 0.960 W Tbaseplate = 85 °C	θjc = 17.7 (°C/W) Tchannel = 102 °C Tm = 9.8E+9 Hrs	3/
Mounting Temperature		Refer to Solder Reflow Profiles (pp 12)	
Storage Temperature		-65 to 150 °C	

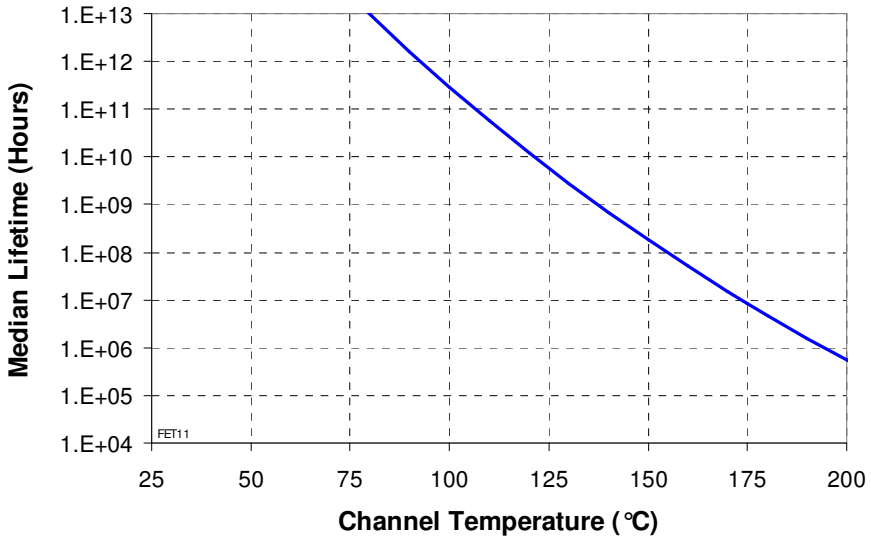
1/ For a median life of 2.4E+7 hours, Power Dissipation is limited to

$$Pd(max) = (150\ °C - Tbase\ °C)/\theta jc.$$

2/ Channel operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

3/ For this flip-chip die, the baseplate is a plane between the Cu/Sn pillars and the test board. For the TGC4704-FC, the critical pillars for thermal power dissipation are 24 thru 33. (See Mechanical Drawing.)

Median Lifetime (Tm) vs Channel Temperature



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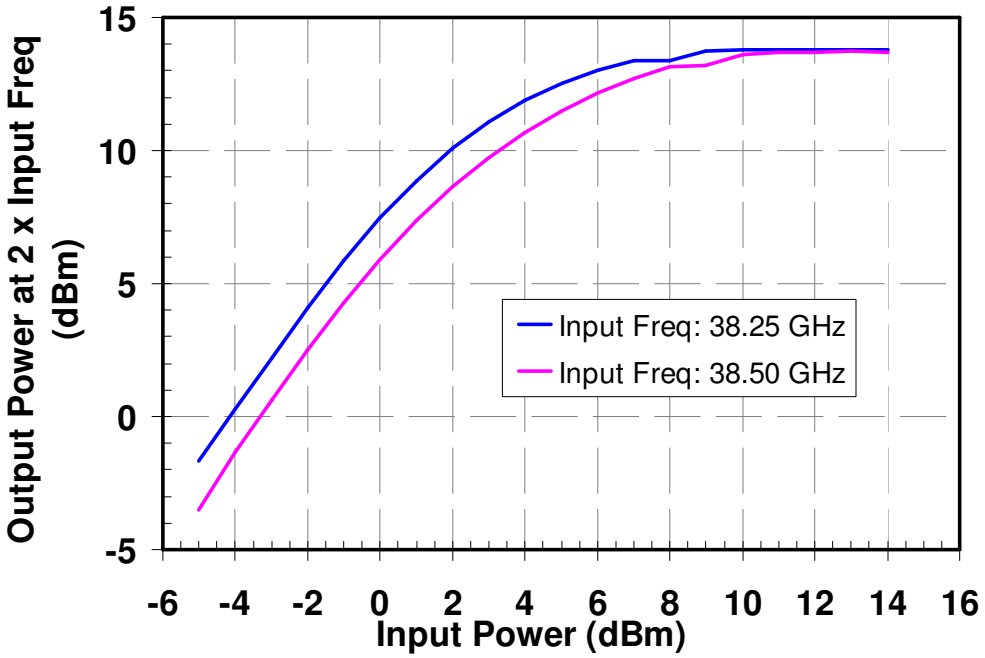
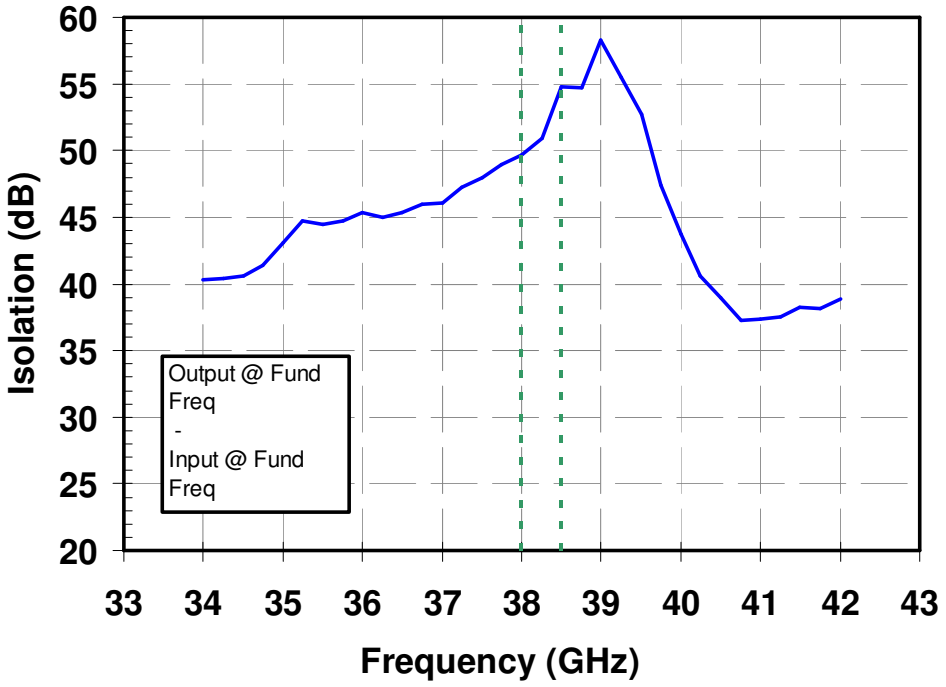
Measured Data on Flipped Die on Carrier Board

Bias: Vd = 4.0 V, Idq = 180 mA, Vg1 = -0.4 V, Vg2 = +0.2 V Typical





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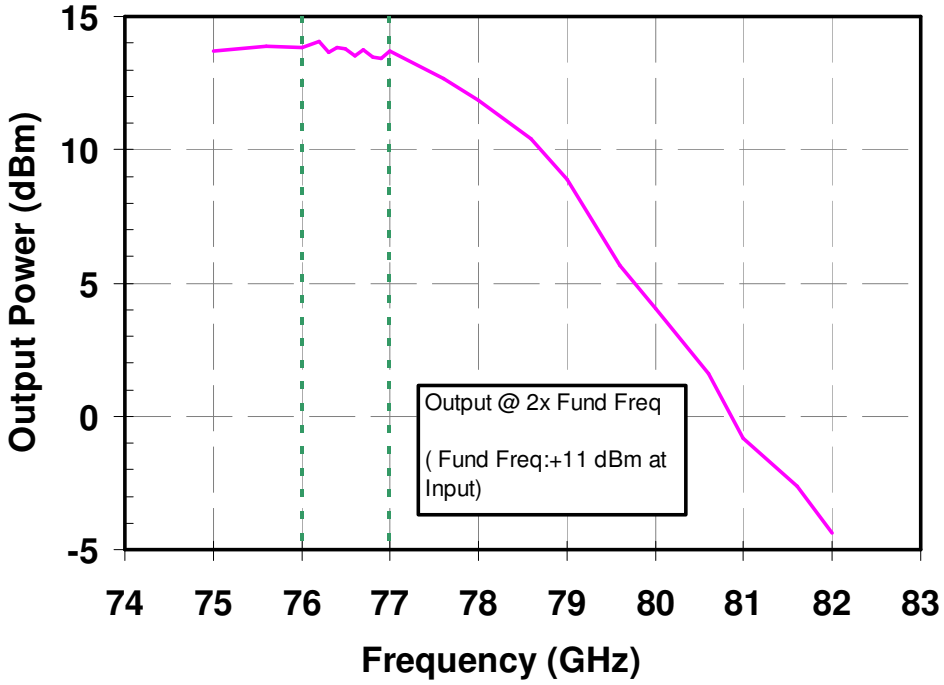

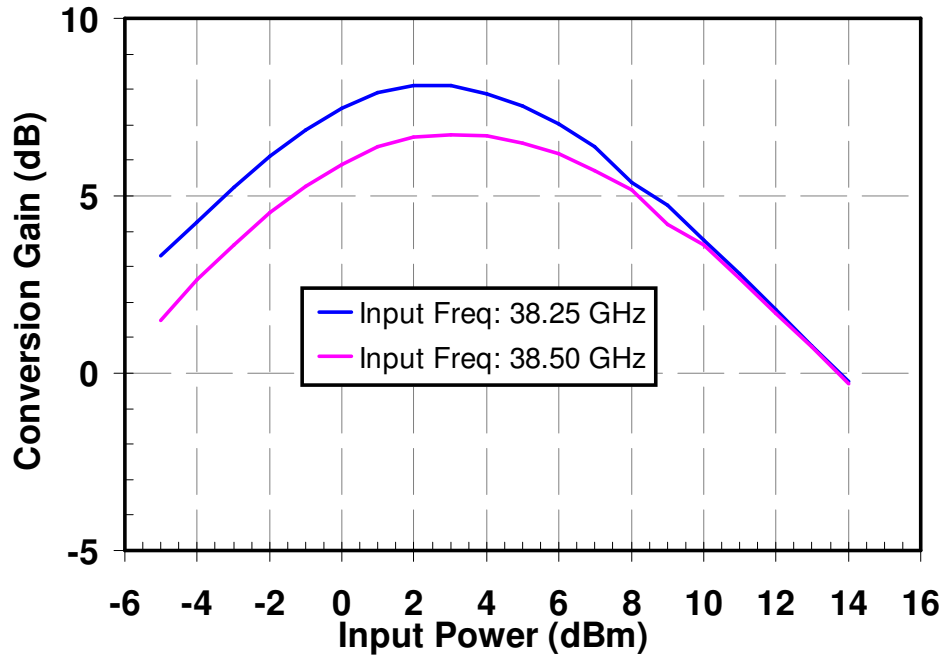

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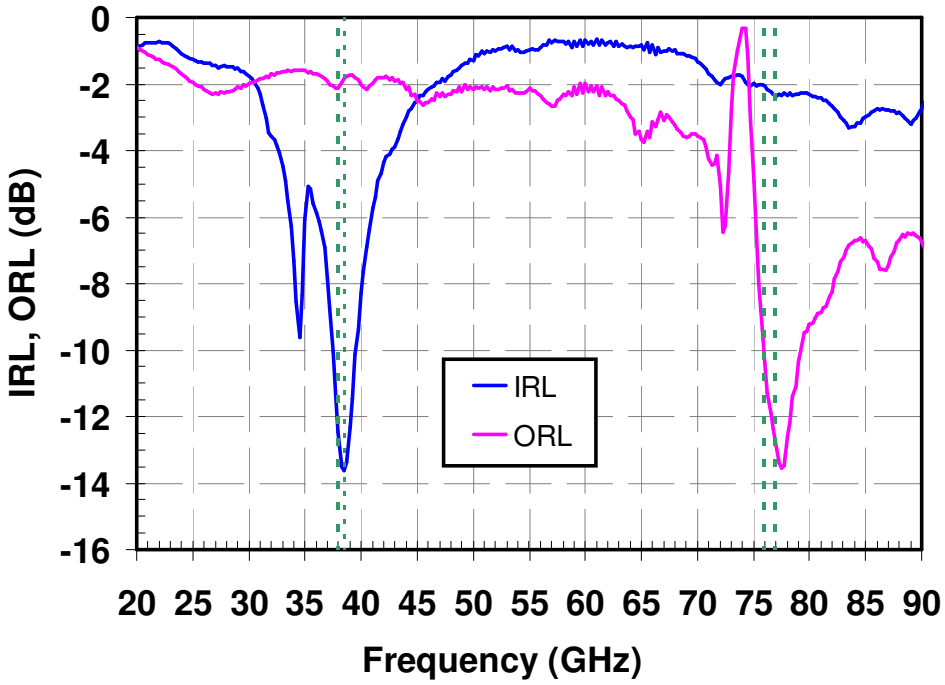

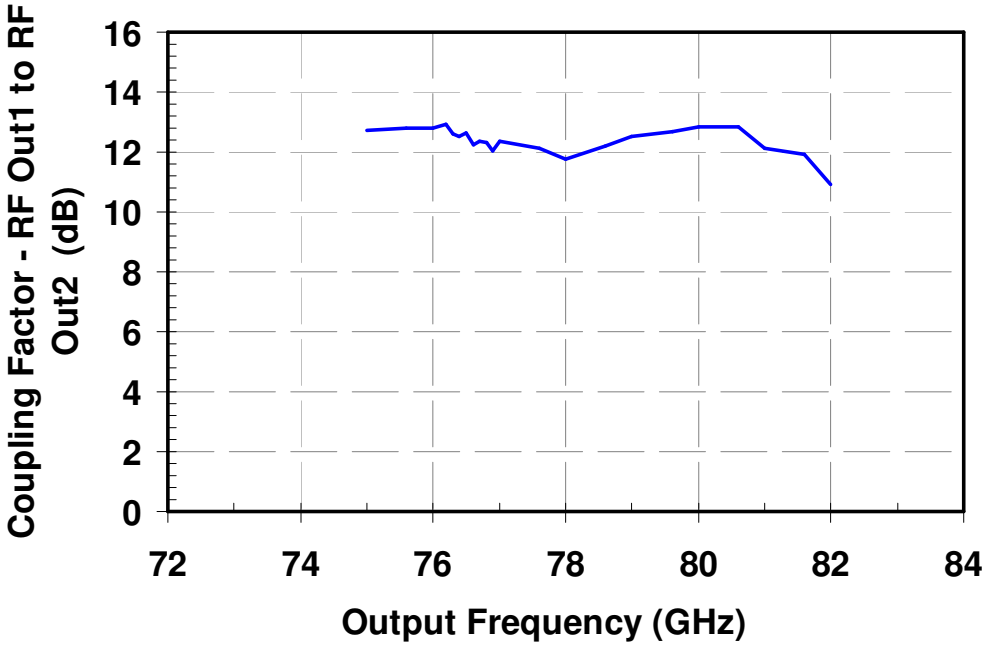

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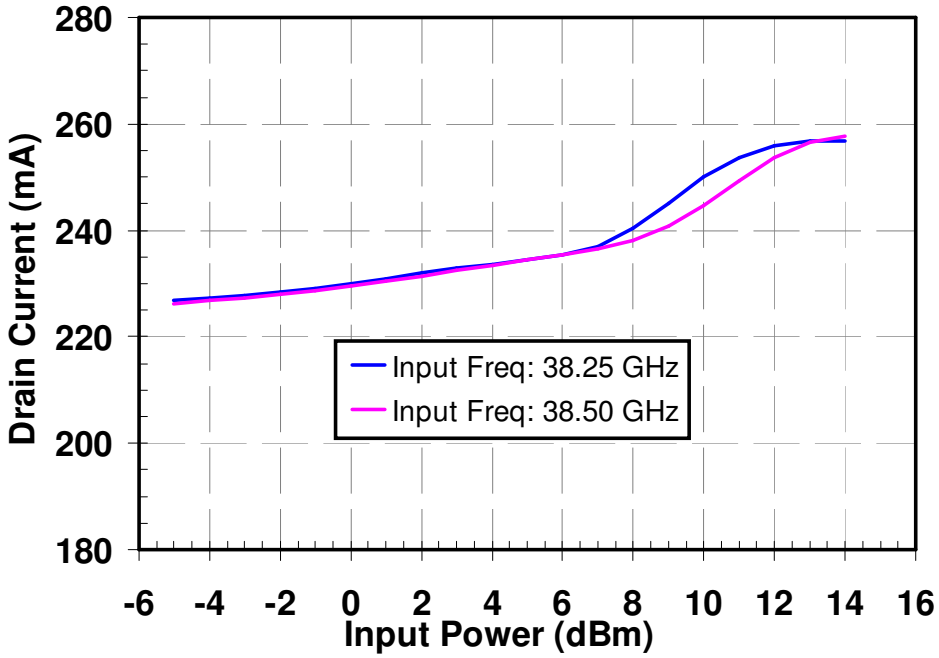

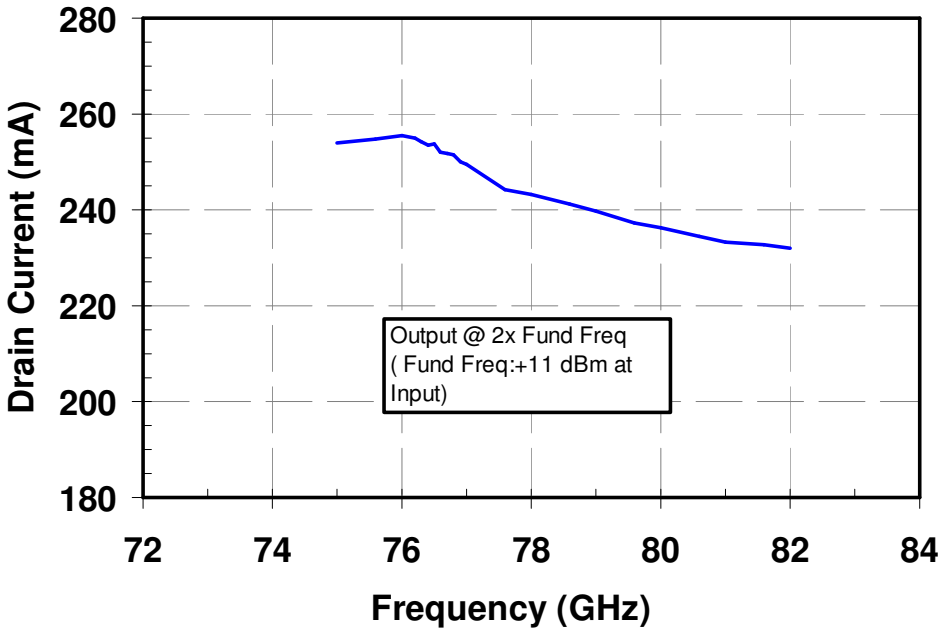

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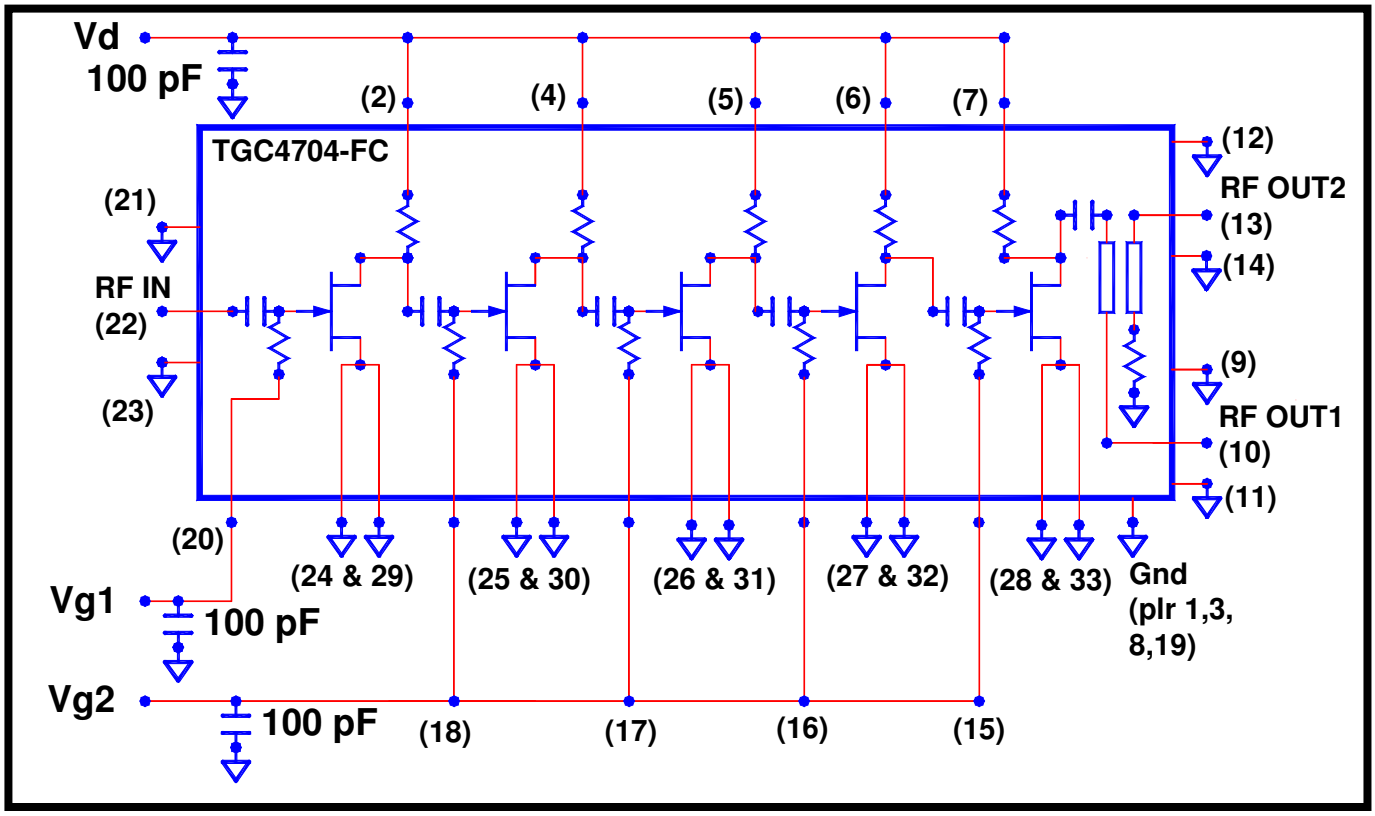
Electrical Schematic



Bias Procedures

Bias-up Procedure

Vg1, Vg2 set to -0.4 V

Vd set to +3.75 V

Adjust Vg2 ONLY more positive until Id is 180 mA
(Vg ~ +0.2 V)

Apply RF signal to input
Id will be ~240 mA

Bias-down Procedure

Turn off RF signal to input

Reduce Vg1,2 to -0.4 V. Ensure Id ~ 0 mA

Turn Vd to 0 V

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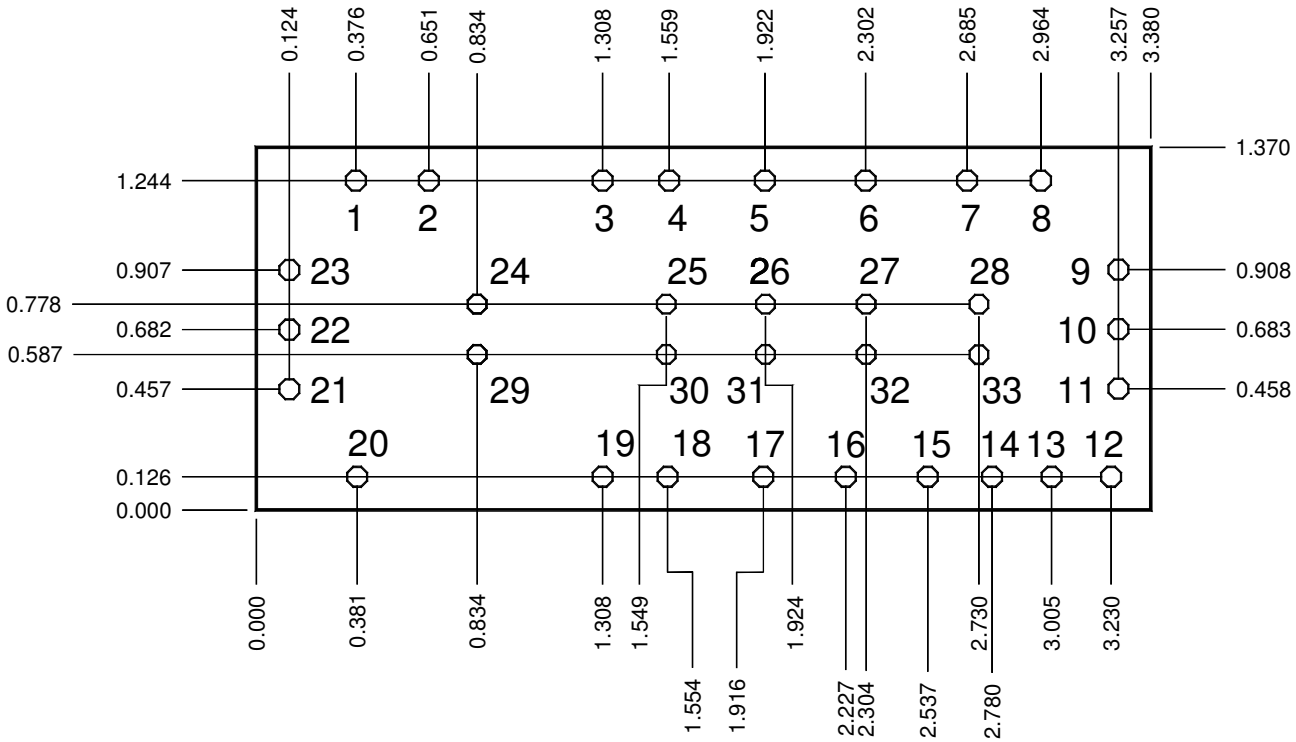
TGC4704-FC

Mechanical Drawing

Drawing is for chip face-up



Units: millimeters Thickness: 0.380

Die x, y size tolerance +/- 0.050

Chip edge to pillar dimensions are shown to center of pillar

Pillar #22	RF In	0.075 Ø
Pillar #10	RF Out1 (Main)	0.075 Ø
Pillar #13	RF Out2 (Coupled)	0.075 Ø
Pillar #9, 11, 12, 14, 21, 23	RF CPW Ground	0.075 Ø
Pillar #20	Vg1	0.075 Ø
Pillar #18	Vg2a	0.075 Ø
Pillar #17	Vg2b	0.075 Ø
Pillar #16	Vg2c	0.075 Ø

Pillar #15	Vg2d	0.075 Ø
Pillar #2	Vd1	0.075 Ø
Pillar #4	Vd2a	0.075 Ø
Pillar #5	Vd2b	0.075 Ø
Pillar #6	Vd2c	0.075 Ø
Pillar #7	Vd2d	0.075 Ø
Pillar #1,3 8,19, 24 thru 33	DC Ground	0.075 Ø

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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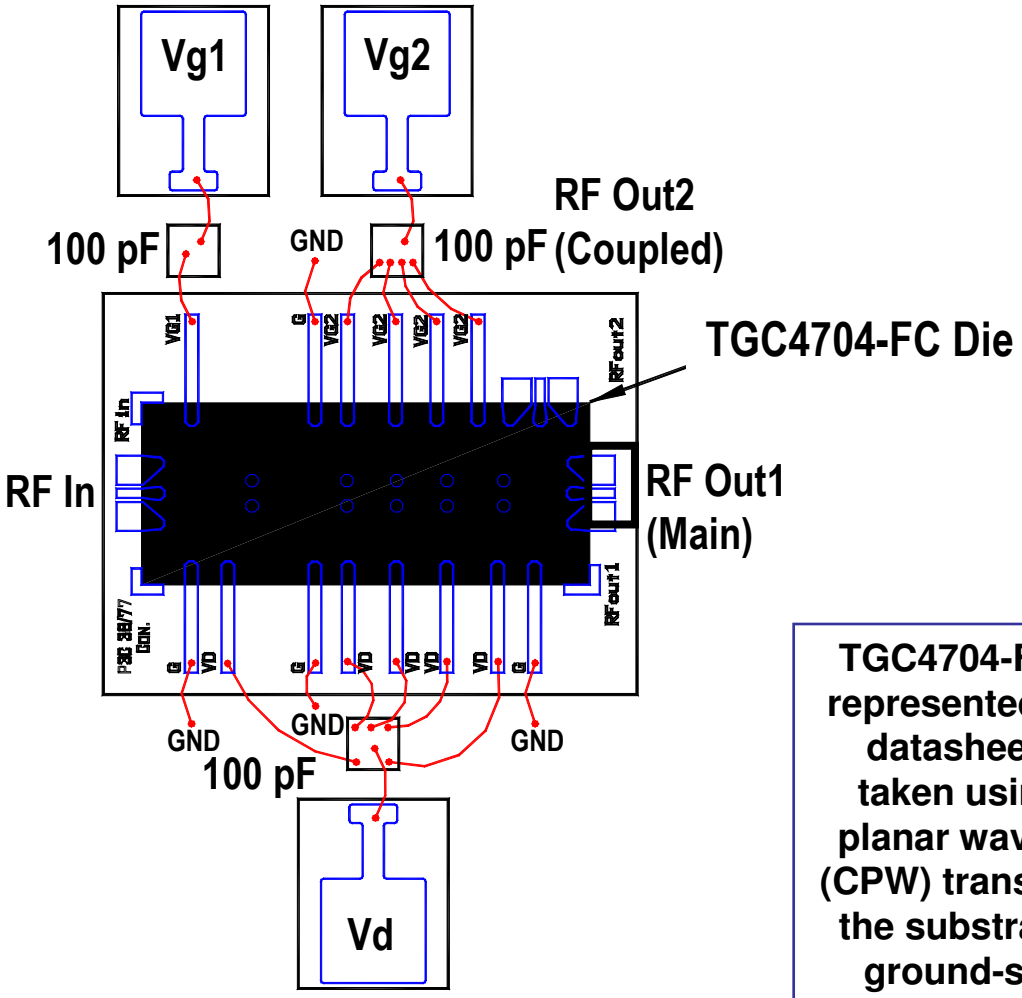
Recommended Assembly Diagram



TGC4704-FC data represented in this datasheet was taken using co-planar waveguide (CPW) transition on the substrate and ground-signal-ground probes

Die is flip-chip soldered to a 15 mil thick alumina test substrate

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Assembly Notes

Component placement and die attach assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- Cu pillars on die are 65 um tall with a 22 um tall Sn solder cap.
- Recommended board metallization is evaporated TiW followed by nickel/gold at pillar attach interface. Ni is the adhesion layer for the solder and the gold keeps the Ni from oxidizing. The Au should be kept to a minimum to avoid embrittlement; suggested Au / Sn mass ratio must not exceed 8%.
- Au metallization is not recommended on traces due to solder wicking and consumption concerns. If Au traces are used, a physical solder barrier must be applied or designed into the pad area of the board. The barrier must be sufficient to keep the solder from undercutting the barrier.

Reflow process assembly notes:

- Minimum alloying temperatures 245 ^{0}C.
- Repeating reflow cycles is not recommended due to Sn consumption on the first reflow cycle.
- An alloy station or conveyor furnace with an inert atmosphere such as N2 should be used.
- Dip copper pillars in “no-clean flip chip” flux prior to solder attach. Suggest using a high temperature flux. Avoid exposing entire die to flux.
- If screen printing flux, use small apertures and minimize volume of flux applied.
- Coefficient of thermal expansion matching between the MMIC and the substrate/board is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.
- Suggested reflow will depend on board material and density.

Typical Reflow Profiles for TriQuint Cu / Sn Pillars

Process	Sn Reflow
Ramp-up Rate	3 ^{0}C/sec
Flux Activation Time and Temperature	60 – 120 sec @ 140 – 160 ^{0}C
Time above Melting Point (245 ^{0}C)	60 – 150 sec
Max Peak Temperature	300 ^{0}C
Time within 5 ^{0}C of Peak Temperature	10 – 20 sec
Ramp-down Rate	4 – 6 ^{0}C/sec

Ordering Information

Part	Package Style
TGC4704-FC	GaAs MMIC Die

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